Integration Design of Chip and Package for Cost-Effective High-Speed Applications

Nansen Chen, Hongchin Lin, Nan-Cheng Chen, Roger Wu, Tomson Chou, and Herbie Chien

Abstract – **Low cost is the trend for consumer electronics. However, the challenges of the LCD-TV processor using cost-effective two-layer ball grid array (BGA) packages suffer from serious crosstalk and return loss due to lack of a solid plane to suppress the coupling effect and control the trace impedance. Two types of two-layer BGA packages were measured and simulated using a 3D full-wave electromagnetic field solver and an EM-based 3D parasitic extractor to analyze their speed limitations and power coupling between the signals and the power net. The results indicated the signal coupling is the dominant factor for insertion loss. Thus, the design guidelines and specifications using two-layer BGA packages are proposed for development of the next generation processors.**

I. Introduction

Many reports have indicated the LCD TV is the fastest growing product in TFT LCD applications. The trend of LCD TV includes the larger panel, higher resolution, and lower cost. In addition to the panel, the most important component in the LCD TV is the processor. The processor drives an external DDR SDRAM that is used for the text and graphic generations, or MPEG buffer. Therefore, the speed of the memory interface influences the LCD-TV performance. Most of LCD-TV processors were encapsulated using the higher cost four-layer ball grid array (BGA) packages to preserve the signal quality at the high-speed memory interface. However, the two-layer BGA package embedded with the plating lines may be considered for low cost requirement. In this paper, two types of two-layer packages were adopted and evaluated. A 3D full-wave electromagnetic field solver and an EM-based 3D parasitic extractor were used to analyze their S-parameters and power inductance for package design. Finally, the design guidelines and S-parameters specifications of two-layer BAG package are suggested for the future product development.

Nansen Chen and Hongchin Lin are with the Department of Electrical Engineering, National Chung-Hsing University, Taichung, Taiwan, E-mail: nansen@seed.net.tw, hclin@dragon.nchu.edu.tw; Nan-Cheng Chen, Roger Wu, Tomson Chou, and Herbie Chien are with MediaTek Inc., Taiwan, E-mail: Charles_Chen@mtk.com.tw

II. BGA Package Layouts

The two kinds of two-layer BGA packages, AT02 and AT05, were used to encapsulate the LCD-TV processors. The detailed package parameters are given in Table I. Fig. 1 shows parts of the high-speed signals and power/ground net layouts including DQ0-15, DQS0-1, DQM0, DVDD2 (power net), and DVSS (ground net). The major difference between the two layouts is two solder-ball rows in AT05 and four solder-ball rows in AT02. The larger trace span is found in AT05 due to less ball rows. Some traces in AT02 were designed in the form of serpentine that servers as a delay line.

III. Testing Results and Simulation Methods

Both of the packages including the processor were tested on the PCB. The testing results indicated the speed limitations for AT02 and AT05 are 378 Mbps and 332 Mbp, respectively. However, the goal of data speed for AT02 is 400 Mbps, which is the maximum data speed of DDR SDRAM. In the following sections, both of the package layouts are investigated using S-parameter simulations. Good trace layouts are preserved as reusable layouts for the future package design.

For wideband digital signals, S-parameters contain the effects of reflection or transmission of power for any network [1]. Thus, S-parameters are useful to determine the power scattering effect and power receiving performance between signal ports, such as the coupling relationship between the signals and the power net. A test load of 50 Ω was used to measure the rising time (T_r, 20%–80%) of 0.214 ns for the DQ signal at the load terminal. The 3-dB bandwidth (F_{3dB}) was calculated by $0.35/T_r \approx 1.6$ GHz. Ansoft HFSS was utilized to extract their S-parameters up to 3 GHz based on the package geometry and material given in Table I. The extended bandwidths are evaluated for higher speed, or smaller T_r up to 125 ns. Both ends of gold wire and solder-ball for signals or DVDD2 were assigned to lumped ports terminated to 50 Ω. DVSS was connected to the ideal ground, which is 0.381 mm below the package.

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IV. Evaluation of Electrical Characteristics

A. Signal Loss and Coupling effects

The drawback of two-layer BGA package is lack of a solid ground plane under the signal traces to control trace impedance and suppress the crosstalk. Larger insertion loss will be expected because of larger return loss and crosstalk. Fig. 2 shows the insertion losses for DQ0-15 of AT02 and AT05. From the rise time T_r measurement giving the 3-dB frequency of 1.6 GHz, we can observe that for frequency lower than 1.6 GHz the insertion loss of AT02 is less than that of AT05 due to the more serious loss of DQ11 and DQ12 in AT05. Note that if these two traces are failed, the chip can not work correctly. It is also worth noting that for DQ 8 and DQ9 on AT02, resonance may be occurred at 2.5 GHz, which means the signal quality will be poor if their bit rates increase significantly. The largest insertion loss occurred at DQ12 in AT05 is caused by the significant coupling between DQ11 and DQ12 as shown in Fig. 3. Comparison of return loss and near-end coupling for both packages is given in Fig. 5. The neighbor coupling in DQ11-12 dominates the performance in insertion loss, while return loss does not. Therefore, well control of signal coupling will be the major challenge for high-speed signals using the two-layer BGA package. For example, the interlacing layout of AT05 DQ2 illustrated in Fig. 4 gives the neighbor couplings less than –20dB, which is not shown in this paper due to limitation of paper space.

B. Power Inductance and Coupling

Ansoft Maxwell 3-D Quick Parameter Extractor was used to extract DVDD2 inductance. The simulated inductance values are 1.16nH and 3.20 nH for AT05 and AT02, respectively. Thus, the power net supplied to high-speed signals in both packages cannot be assumed as ideal reference plane. The power inductance induces the power drop and simultaneous switching noise (SSN), called power noise. When the power noise occurs, the signal traces will induce the noise coupling. Fig. 6 shows the DVDD2 coupling to the DQ lines. The power coupling is not as serious as expected due to the thick BT core (0.4 mm). Although the coupling magnitudes for frequencies lower than 1.6 GHz are insignificant, the trend of power coupling is increasing when the data speed increases or the data rise time decreases. If the non-ideal power net beneath the high-speed traces is removed, the noise coupling will be reduced.

V. Layout Guidelines and Specifications

The goal to reuse the two-layer BGA package embedded with the plating lines for the future LCD-TV processor is to ensure minimum insertion loss. To achieve this goal, well control of signal coupling or crosstalk becomes the critical issue. Some suggestions for the two-layer substrate layout are as follows.

- Interlace the high-speed traces between the top and bottom layers.
- Reduce the length of parallel traces, including the plating line, which can reduce the crosstalk saturation [2].
- Insert the ground wire paralleled with the signal trace, if possible, which can reduce the signal parasitic parameters and coupling effects.
- Move the signal as far away as possible from the power net (DVDD2) on the same layer.
- For many high-speed I/Os on the package, use three or four rows of I/O balls to reduce the routing span in the package.
- Carefully design the power nets, such as DVDD2, supplied to the high-speed signals to reduce the inductance. For instance, layout DVDD2 toward the inner balls to shorten the electrical path.
- Avoid the high-speed I/O pads at the chip corner that can reduce the length of bondwire and trace routing in the package.

Ref. [3] demonstrates another S-parameters analysis for high-speed applications using the leadframe packages. With the analysis and the guidelines given above as well as Ref. [3], the package specifications of signal loss and coupling on DDR SDRAM interface could be defined in Table II. The smaller signal rise time is, the tighter loss budget is.

VI. Conclusion

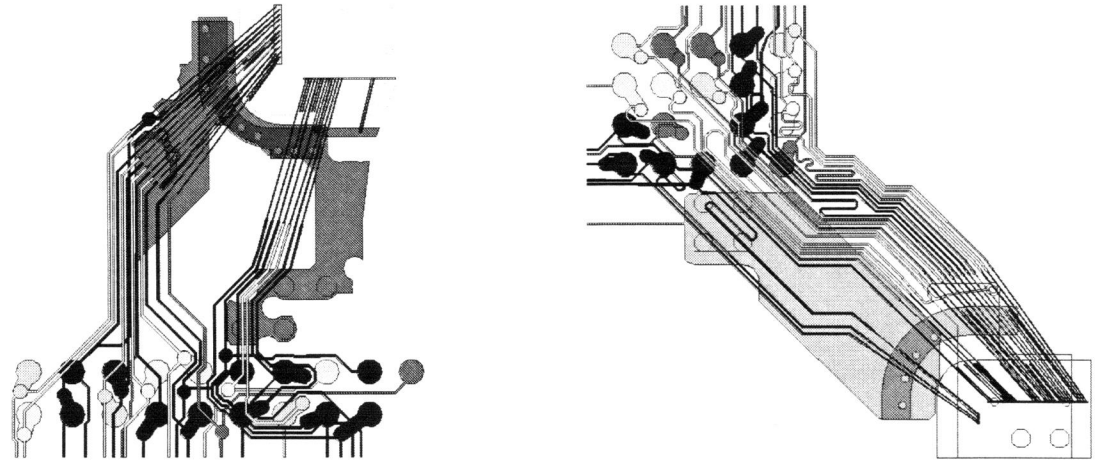
Lower cost two-layer BGA package could be achieved for high-speed applications, such as the LCD-TV processors. This paper demonstrates the frequency domain analysis of two types of two-layer BGA packages for the high-speed memory interface. Well control of signal coupling is the major challenge when the two-layer BGA package embedded with the plating lines is used. The package design guidelines and specifications are presented for the future product development. The future work will be verification of the package specifications followed by the guidelines.

References

[1] T. C. Edwards and M. B. Steer, *Foundations of Interconnect and Microstrip Design*, 3rd ed., New York: John Wiley & Sons, 2000, pp. 457–470.

[2] D.N. de Araujo, M. Cases, N. Pham, and E. Matoglu, "Co-design optimization of laminate substrates for high speed applications," *IEEE 54th Electronic Components and Technology Conference*, pp. 1776-1783, Jun. 2004.

[3] N. Chen and H. Lin, "Design and evaluation of chip on heat sink quad flat package (COHS-QFP) for consumer electronics," *iMAPS-Taiwan 2005 Technical Symposium*, pp. 260-264, Jun. 2005.



(a) (b)

Fig. 1. Two types of two-layer BGA package layout (a) AT05 (DQ0-15) and (b) AT02 (DQ0-15).

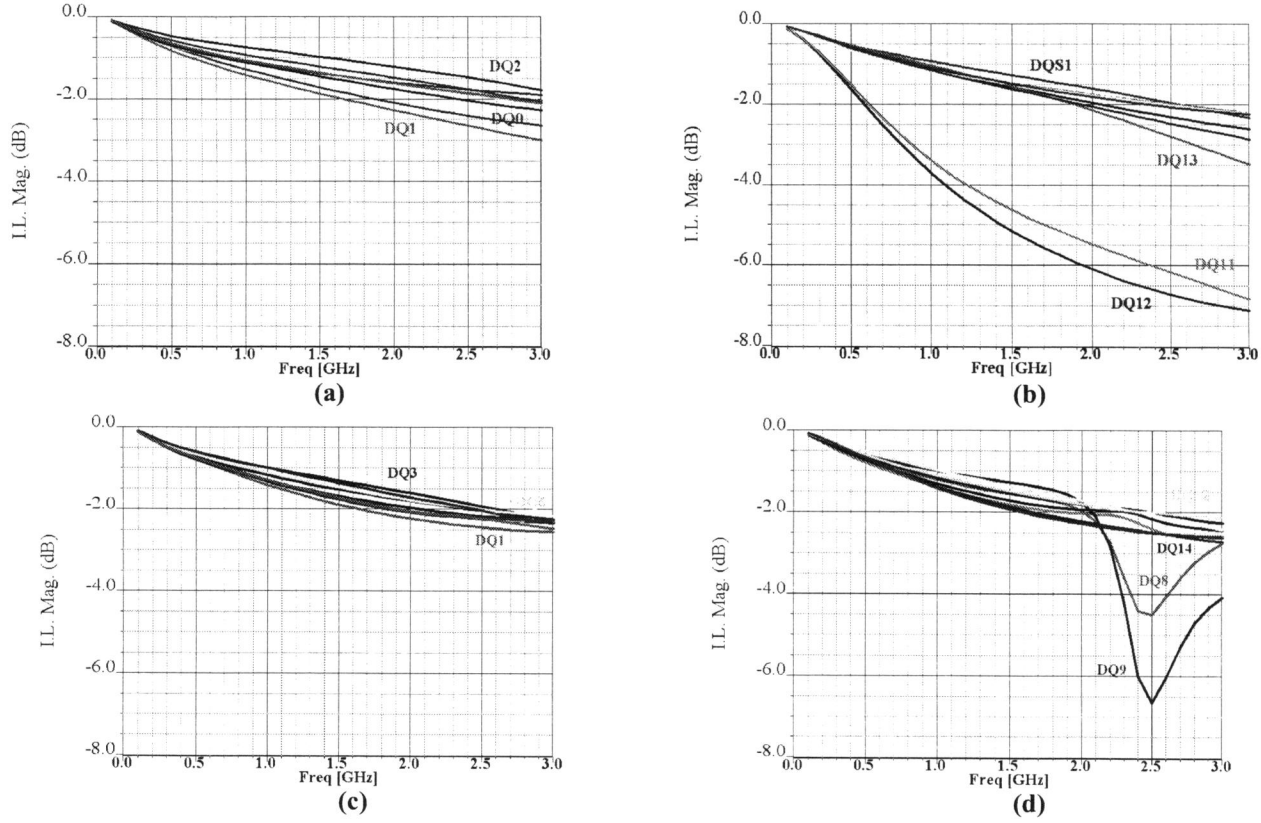


Fig. 2. Insertion loss (a) AT05: DQ0-7, (b) AT05: DQ8-15, (c) AT02: DQ0-7, and (d) AT02: DQ8-15.

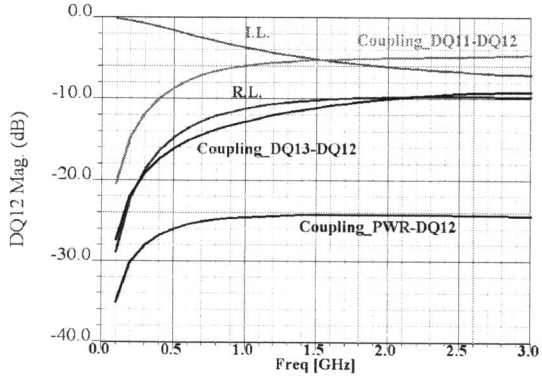


Fig. 3. S-parameters magnitude of AT05 DQ12.

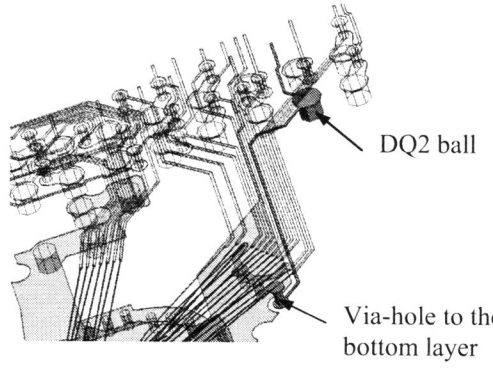


Fig. 4. The interlacing layout of AT05 DQ2 with the most portion of copper on the bottom layer and the most portions of neighboring traces on the top layer.

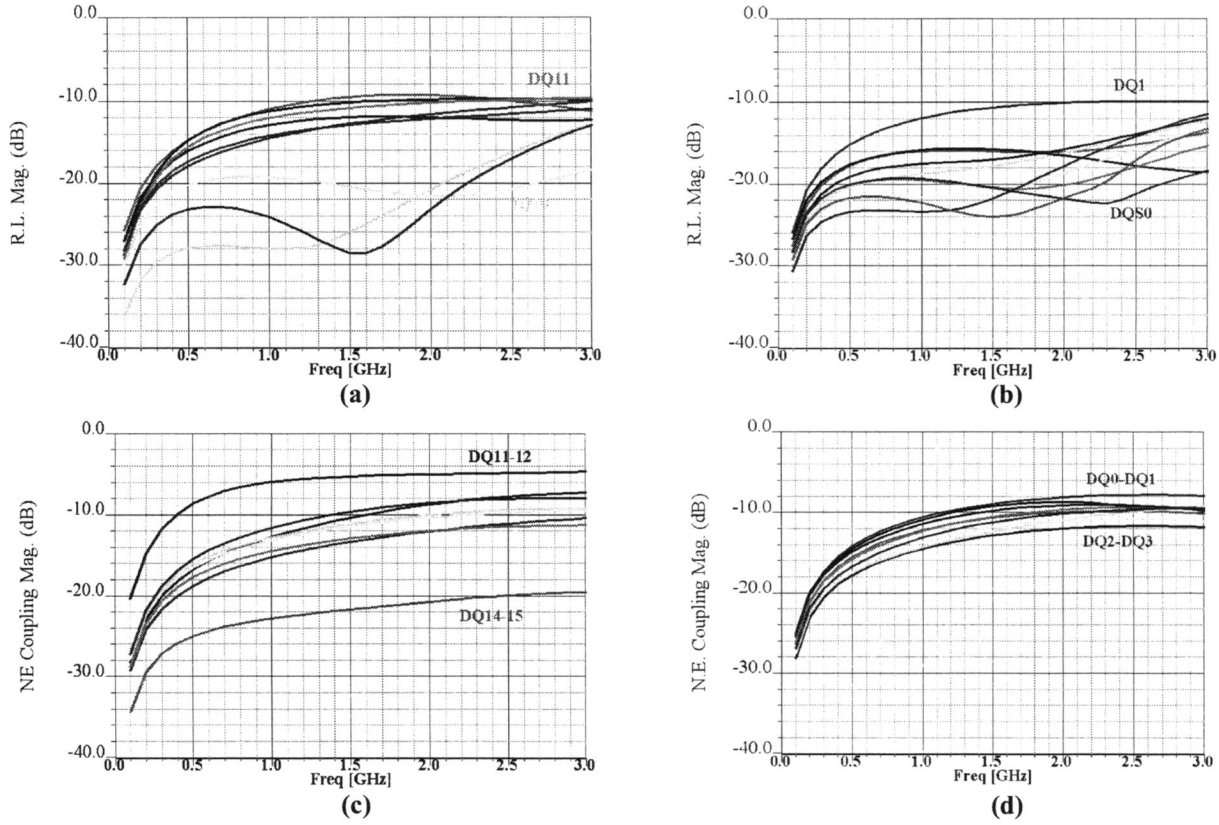


Fig. 5. Return loss (a) AT05: DQ8-15, (b) AT02: DQ0-7, and near-end coupling (c) AT05: DQ8-15, (d) AT02: DQ0-7.

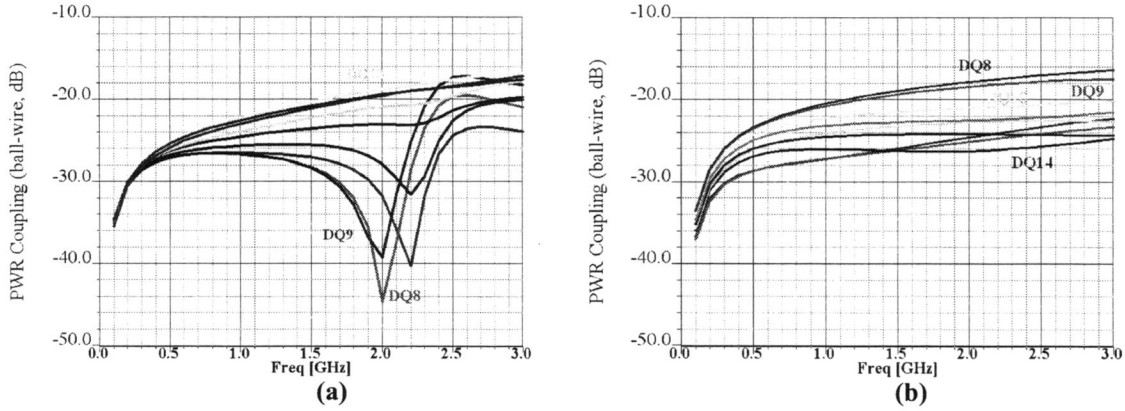


Fig. 6. Power (DVDD2 balls) coupling to signal wires (a) AT02: DQ8-15 and (b) AT05: DQ8-15.

TABLE I
DETAILED PACKAGE PARAMETERS

Code no.	AT02	AT05
Package size (LxWxH, mm)	27 x 27 x 2.2	
Ball count/pitch	388 / 1.0-mm	
Trace width/thickness	50/27 μm	55/27 μm
Mold thickness	1.17 mm (D_k = 4.0, D_f = 0.01)	
BT core thickness	0.4 mm (D_k = 4.2, D_f = 0.012)	
Solder-mask thickness	40 μm (D_k = 4.0, D_f = 0.028)	
Gold-wire diameter	0.8 mil	0.9 mil
Chip-pad pitch	60 μm	72 μm
Via-hole diameter	0.2 mm	
Metal conductivity (σ)	Copper: 5.8 x 10^7 /Ω-m Gold: 4.1 x 10^7 /Ω-m	
DVDD2 balls/wires	4/10	8/17

TABLE II
PACKAGE SPECIFICATIONS FOR SIGNAL LOSS AND COUPLING

Item	Max. Specification
Insertion loss	−3 dB
Average NE coupling	−10 dB
Return loss	−10 dB
Power coupling	−17 dB