A Low-Voltage Process Corner Insensitive Subthreshold CMOS Voltage Reference Circuit

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Abstract — **A reference voltage circuit is presented for generating a constant reference voltage of 278mV using subthreshold characteristics of 0.18μm CMOS technology at supply voltages from 0.8V to 2.6V with total current of 3.6μA. The threshold voltage variation due to process corner variation is minimized by a threshold voltage tracking technique between the normal and high threshold NMOS transistors. In the mean time, channel-length modulation effect is also compensated. The proposed circuit on chip area of 0.04*mm*^{2} achieves the total reference voltage variation of 2.5mV for various process corners and temperature variation from -20°C to 120°C.**

I. INTRODUCTION

In many applications, a precise and stable reference voltage is widely used in analog and mixed-signal circuits like A/D and D/A converters, voltage regulators, DRAM/flash memories and other communication devices. It may requires small area, low power consumption and low sensitivity to the supply voltage (V_{DD}) as well as temperature. The conventional voltage reference circuits usually employ the characteristics of bandgap using diodes or BJT transistors. To achieve low supply voltage operation, some people pushed the limit to sub 1-V [1]-[2]. Since the turn-on voltage of diode or parasitic BJT transistor is around 0.6V at room temperature and even 0.8V at -20°C. It is almost impossible to reduce the supply voltage any further. The possibility to further reduce the supply voltage may require some other approaches, such as employing subthreshold characteristics of MOS transistors to generate the reference voltage [3]-[4].

However, unlike the accurate bandgap reference circuits, which are insensitive to process corners, the problem of MOSFET's in subthreshold is the process corner variation of threshold voltages. That may result in significant reference voltage variation up to ±15% in the worst process corner. The inaccuracy may make it difficult to be applied in many circuits. To overcome this problem, a new subthreshold voltage reference circuit resisting process corner variation is proposed by using another type of MOS transistor with the different threshold voltage (V_{th}) to compensate the variation. With this new technique, the variation can be reduced to ±0.7% or lower in the worst process corner.

This work was supported by National Science Council of Taiwan, R.O.C. (NSC-94-2215-E-005-013 and NSC94-2220-E-005-005)

II. DESIGN PRINCIPLES

For an NMOS Transistor in subthreshold, *i.e.* $V_{GS}<V_{th}$, the drain current I_D is quite small but non-zero, where V_{th} is the threshold voltage. It exhibits an exponential dependence on V_{GS}. This effect can be formulated for V_{DS} greater than roughly 200mV [4]-[5]:

$$I_D = I_0 \frac{W}{L} \exp \frac{V_{GS}}{\varsigma V_T} \quad , \tag{1}$$

where $\varsigma > 1$ is a non-ideal factor and $V_T = kT/q$ is the thermal voltage.

It is well known that the threshold voltage of NMOS transistor is decreased as temperature is increased. The following is the simplified expression:

$$V_{th}(T) = V_{th}(T_0) - K_T(T/T_0 - 1) \quad , \tag{2}$$

where $K_T > 0$ and T_0 is the reference temperature.

The above equation indicates V_{th} is a good candidate to make a reference voltage due to linear temperature variation. However, V_{th} may have significant variations for different process corners, unlike the diode having a nearly constant turn-on voltage with little variation due to process corners. Fig. 1 shows V_{th} as functions of temperature for a normal NMOS transistor in fast (FF), typical (TT) and slow (SS) corners of 0.18μm CMOS technology.

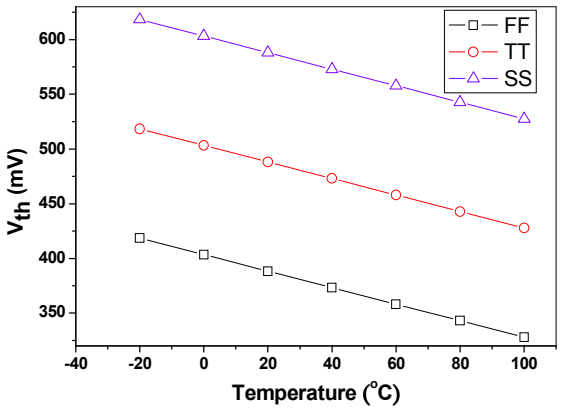

Fig. 1 V_{th} as functions of temperature for different process corners

The large V_{th} variation in different process corner leads significant variation of reference voltage if V_{th} is utilized. Fig. 2 demonstrates significant reference voltage fluctuation due to process corner variation using the reference voltage generator [4] operated in subthreshold region using 0.18μm CMOS technology. It can be observed that the reference voltage is quite stable at the typical corner, but fluctuation could reach ±40mV at the worst process corner. That is approximately ±15% deviation from the target value.

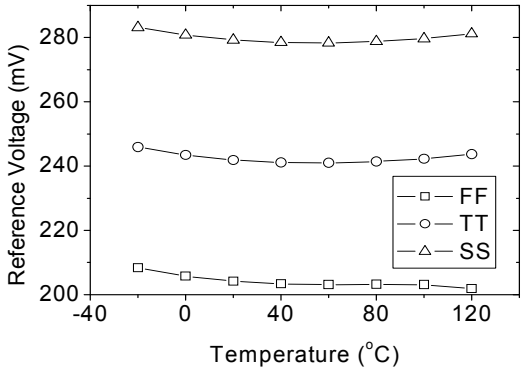

Fig. 2 The reference voltages in different process corners using the circuit proposed in Ref. [4]

To overcome this problem, another NMOS transistor with higher V_{th} in the same 0.18μm CMOS technology can be used to compensate the process variation. Since the major process difference is the gate oxide thickness, the threshold voltage variations of both the normal and high-V_{th} NMOS transistors go to the same trend for different corners due to the same doping conditions. In addition, the thicker gate oxide of high-V_{th} NMOS is obtained by additional oxidation. The first gate oxidation is the same as the normal NMOS. Therefore, the process corner variations of these two types of transistors will be very similar. If the difference of V_{th} between them is plotted as functions of temperature, the different process corners will have negligible difference as shown in Fig. 3.

It is worth noting that another medium-V_{th} NMOS transistor may be in place of the high-V_{th} NMOS transistor for even lower supply voltage operation. The process difference is the V_{th} doping in the channel, while the gate oxide is as the same as the normal NMOS transistor. In this paper, the high-V_{th} transistor is used for demonstration.

For a MOSFET in subthreshold region, the relation between V_{GS} and V_{th} as a function of temperature can be approximated as [5]

$$V_{GS}(T) \approx V_{GS}(T_0) - K_G\left(\frac{T}{T_0} - 1\right), \qquad (3)$$

where $K_G \cong K_T + V_{th}(T_0) + V_{OFF} - V_{GS}(T_0)$. The quantity K_G is positive, so V_{GS} is decreased with the temperature. With the characteristics of Fig. 3, the difference of V_{GS} between the normal and high-V_{th} NMOS transistors can be modeled as

$$\begin{aligned}\Delta V_{GS}(T) &\approx \Delta V_{GS}(T_0) - (K_{Gh} - K_{Gn})\left(\frac{T}{T_0} - 1\right) \\ &= \Delta V_{GS}(T_0) + \Delta K_G - \Delta K_G \frac{T}{T_0}\end{aligned} \qquad (4)$$

where $\Delta V_{GS} = V_{GSh} - V_{GSn}$ and $\Delta K_G = K_{Gh} - K_{Gn}$. V_{GSh}, K_{Gh} and V_{GSn}, K_{Gn} are V_{GS}, K_G of high-V_{th} and normal NMOS transistors, respectively. Eqn. (4) still shows negative temperature coefficients of ΔV_{GS}, since $K_{Gh} > K_{Gn}$.

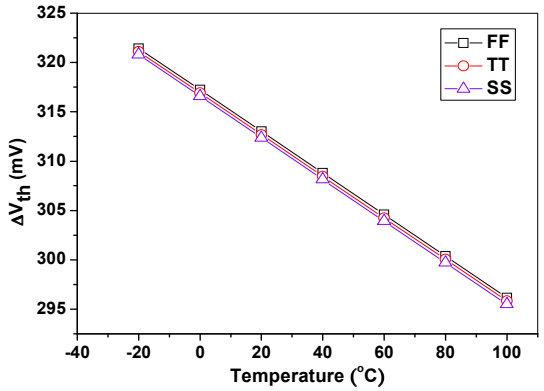

Fig. 3 Difference of V_{th} between the normal and high-V_{th} NMOS transistors is small for various process corners.

III. THE PROPOSED CIRCUIT

The proposed circuit in Fig. 4 is composed of one current source with positive temperature coefficients and two current sources with different negative temperature coefficients as well as a current sum with a resistor to generate the reference voltage.

Transistors M10~M13 and Resistor R3 generate a constant current source. If the sizes of M10, M12 are equal and those of M11, M13 as well as R3 are selected properly, M11 and M13 may be operated in subthreshold region. With $V_{GS11} = V_{GS13} + I_{12}R3$, where I_{12} is the current through M12, the following expression can be obtained.

$$I_{12} = \frac{\varsigma V_T}{R3}\ln\left(\frac{P_{13}}{P_{11}}\right), \qquad (5)$$

where $P_i = (W_{eff}/L_{eff})_i$ and "i" is the device number. Obviously, I_{12} gives a positive temperature coefficient. Note that the current source generator requires a startup circuit [4] which is not shown in Fig. 4.

Transistors M1 and M8 mirror the current I_{12} to generate V_{GS3} and V_{GS9}, which are used to produce $I_{R1} = V_{GS3}/R1$ and $I_{R2} = V_{GS9}/R2$. Since the currents

in M1 and M8 force M3 and M9, which is the special high-V_{th} NMOS transistor, conducting in subthreshold regions, the current through M6 is $I_{R2} - I_{R1}$ if M5 mirrors the current in M2. If $R1 = R2 = R$, the current (I_6) in M6 can be expressed as follows by using Eqn. (4):

$$I_6 = \frac{V_{GS9}}{R} - \frac{V_{GS3}}{R} = \frac{\Delta V_{GS}(T_0) + \Delta K_G}{R} - \frac{\Delta K_G}{R}\frac{T}{T_0} \quad (6)$$

Since the above equation has the similar characteristics given in Fig. 3, the process corner variation can be minimized.

After Currents I_6 and I_{12} mirror to Transistors M14 and M15 with appropriate ratios to generate I_{14} and I_{15}, the constant current goes through R4 producing the reference voltage given by the following expression:

$$V_{ref} = \left(\frac{P_{14}}{P_6} I_6 + \frac{P_{15}}{P_{12}} I_{12}\right) R4 = \frac{P_{14}R4}{P_6 R}\left[\left(\Delta V_{GS}(T_0) + \Delta K_G\right) - \Delta K_G \frac{T}{T_0}\right] + \frac{P_{15}R4}{P_{12}R3}\varsigma V_T \ln\left(\frac{P_{13}}{P_{11}}\right) \quad (7)$$

By choosing appropriate transistor and resistor ratios, the positive and negative temperature coefficients can be compensated to achieve a constant V_{ref} with a zero-temperature coefficient $\left(\partial V_{ref}/\partial T = 0\right)$.

Another important feature of I_{R2} subtracted by the current (I_5) through M5 is that the current I_5 may help reduce the channel-length modulation (CLM) effect in M6. The theoretical formulation was derived in our previous work [6]. If M5 is chosen to have a shorter channel length, the more CLM effect in M5 help reduce CLM effect in M6, and thus M14. It could even make I_{14} slightly decreased as the supply voltage (V_{DD}) is increased. The opposite trends of I_{14} and I_{15} compensate each other to minimize V_{ref} increment as V_{DD} is increased.

IV. IMPLEMENTATION RESULTS

The new voltage reference circuit was simulated using TSMC 0.18μm CMOS technology. The device parameters are listed in Table I. Note that since process corner variations of the normal and high-V_{th} NMOS transistors are not exactly the same, it is intentionally to make R1 and R2 slightly unmatched. Fig. 5 shows the layout which is in fabrication. The chip area of the core circuit with the startup circuit is about $0.04mm^2$. The output voltage is 278mV with the total current consumption of 3.6μA.

The lowest V_{DD} for the circuit to work correctly may be down to 0.8V at the typical corner. However, for the slow NMOS corners including SS and SF corners, the lowest V_{DD} has to be raised to 0.95V. Fig. 6 shows the post-layout simulation results of the reference voltage versus the supply voltage up to 2.6V for the five process corners including SS, SF, TT, FS, FF corners at the room temperature. Since the circuit was tuned at V_{DD} = 1.5V, the fluctuation for V_{ref} = 278mV is ±0.3%, while it is increased to ±0.7% at V_{DD} = 1V. The sensitivity of power supply varied from 0.8V to 2.6V is 1.6mV/V at the typical corner.

TABLE I The parameters of transistors and resistors

Component name	W/L (μm)	Component name	W/L (μm)
M3	5/2	M1, M8, M21, M61	2/4
M5	1.6/0.8	M2, M4, M6, M7	2/1
M9	10/2		
M10, M12	6/3	Component name	kΩ
M11	4/4	R1	570
M13	100/3	R2	600
M14	2.5/1	R3	400
M15	6/3	R4	300

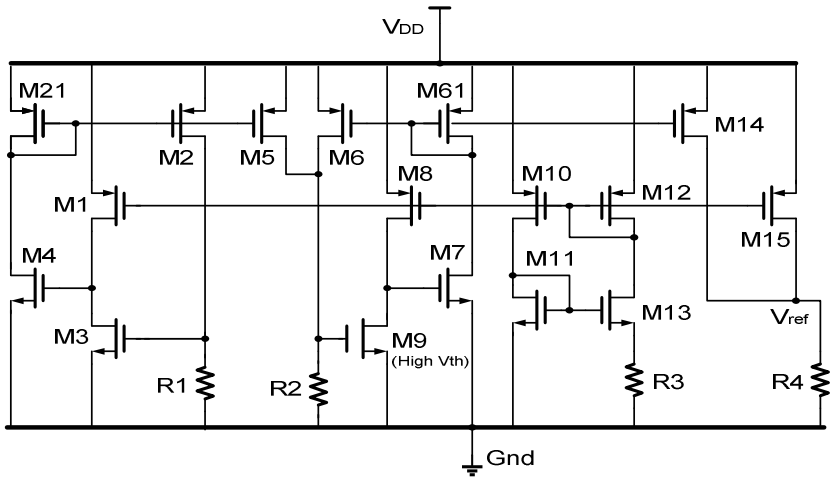

Fig. 4 The schematic of the proposed voltage reference circuit

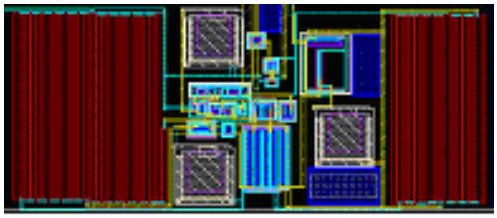

Fig. 5 The layout of the proposed circuit

The performance for temperature from -20°C to 120°C at V_{DD} = 1.5V is demonstrated in Fig. 7. The variation is only 1.1mV or 0.4% at the typical corner. The largest fluctuation in the worst corner is about ±1.34mV, or ±0.48%. In contrast to Fig. 2, in which no compensation of process corners was applied, the fluctuation could reach ±40mV. The new compensation technique significantly improves the stability of the reference voltage. Even though some more components are required, the quality is approaching the conventional bandgap reference. If the threshold voltage keeps lower and lower in the future, the proposed circuit can still work at very low supply voltage due to lower V_{th} in the new technology, while the bandgap reference circuit will be failed in that situation.

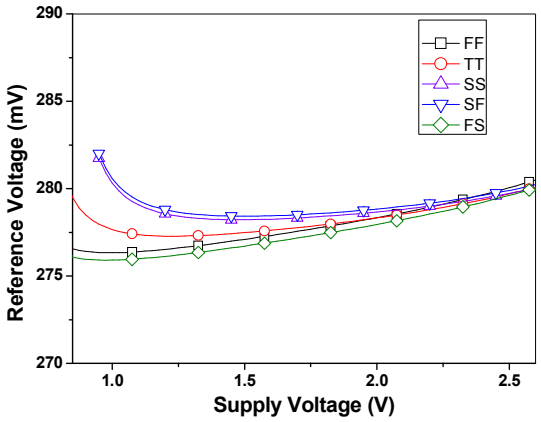

Fig. 6 The reference voltage vs. supply voltage for different process corners at room temperature.

V. CONCLUSIONS

A low-voltage CMOS reference circuit using subthreshold characteristics with compensation technique of high V_{th}-NMOS to improve process-corner variation is proposed. It occupies chip area of $0.04mm^2$ using TSMC 0.18μm CMOS technology. The reference voltage is about 278mV with voltage variation 1.6mV/V for V_{DD} = 0.8V ~ 2.6V and 1.1mV peak-to-peak variation for temperature from -20°C to 120°C in the typical case. The fluctuation due to process corners is limited to ±0.7% in the worst corner condition. It is convinced that the proposed circuit may be useful in the future very low voltage circuit applications.

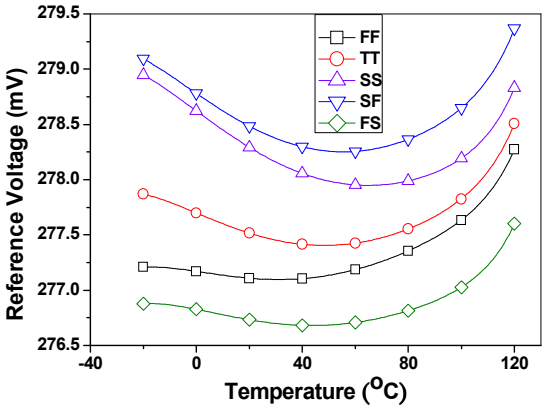

Fig. 7 The output voltage vs. temperature for different process corner at V_{DD} = 1.5V

ACKNOWLEDGMENT

The authors acknowledge the National Chip Implementation Center of Taiwan for their support in chip fabrication.

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