A Novel High-Speed Sense Amplifier for Bi-NOR Flash Memories

Chiu-Chiao Chung, Hongchin Lin, *Member, IEEE*, and Yen-Tai Lin

***Abstract*—A novel high-speed current-mode sense amplifier is proposed for Bi-NOR flash memory designs. Program and erasure of the Bi-NOR technologies employ bi-directional channel FN tunneling with localized shallow P-well structures to realize the high-reliability, high-speed, and low-power operation. The proposed sensing circuit with advanced cross-coupled structure by connecting the gates of clamping transistors to the cross-coupled nodes provides excellent immunity against mismatch compared with the other sense amplifiers. Furthermore, the sensing times for various current differences and bitline capacitances and resistances are all superior to the others. The agreement between simulation and measurement indicates the sensing speed reaches 2 ns for the threshold voltage difference of lower than 1 V at 1.8-V supply voltage even with the high threshold voltage of the peripheral CMOS transistors up to 0.8 V.**

***Index Terms*—Advanced cross-couple, Bi-NOR, clamping transistor, flash memory, FN tunneling, mismatch, threshold voltage.**

I. Introduction

FOR contemporary memories, array structures and periphery circuits, such as decoders, charge pumps, level shifters, and sense amplifiers, determine the overall system performance in terms of power dissipation and access speed. The high-speed low-power sense amplifier is one of the critical components. Due to low-voltage operation, current sensing techniques have received a lot of attention in the last decade. Many sense amplifiers based on cross-coupled transistor structures were designed to overcome the loading effects [1]–[3] for DRAM or SRAM, but few have been discussed about the mismatch of sense amplifiers. Another category of memories is flash memory [4], [5]. The trend is not only high-density and low-voltage, but also multi-level. Therefore, the threshold voltage deviation of the programmed memory cells has to be well controlled for low-voltage operation. The sense amplifiers require high sensitivity and excellent mismatch immunity in threshold voltage and W/L (channel width/channel length) ratio of devices.

For flash memories, comparison of current difference between the flash cell and the reference cell is the direct and fast method to read the data. However, for the Bi-NOR [6], [7] flash memory arrays, most of the sensing circuits developed for the conventional flash memory cells [8], [9], such as the simple four-transistor sense amplifier [10], PMOS bias type sense amplifier [11], and differential latch type sense amplifier [12], are not appropriate. Since these sense amplifiers were designed for draining cell current at the drain node of the flash cell, their bitlines were usually pre-charged to high before sensing. However, the current direction for Bi-NOR cells is reversed. The sense amplifier drains the current of the flash cell at the source node, thus the bias at the bitline source node has to be low enough for the cell current flowing to the sense amplifier. Though the clamped bitline (CBL) sense amplifier [13] was appropriate for the Bi-NOR cells, it would result in higher power consumption, lower sensing speed, and poor mismatch effects due to the equalization of the bitlines before sensing.

To comply with these restrictions, we propose a new sense amplifier (NSA) that utilizes advanced cross-coupled structure by connecting the gates of the clamping MOS transistors to the cross-coupled nodes to improve the mismatch characteristics and reduce the power consumption without scarification of sensing time. The mismatch is also improved if the equalization between the drains of the two clamping MOS transistors is removed, since the currents from the selected cell and the reference cell slightly charge the drains before sensing.

The new circuit and its operation principle for Bi-NOR cells are described in Section II. Section III compares the sensing speed versus threshold voltage difference, bitline capacitance, and channel length mismatch with the clamped bitline sensing scheme. The theory of mismatch improvement is also given in this section. In Section IV, the measurement results show the agreement with simulations. Section V is the conclusion.

II. The New Sense Amplifier and Its Operation

The flash memory cell used in this study is based on the Bi-NOR technology [6], [7], which uses bi-directional channel FN tunneling with localized shallow P-well structure to realize the high-reliability, high-speed, and low-power operation. The conduction channel width of the flash cell is no longer one-dimensional. Fig. 1(a) illustrates the cross-sectional view of Bi-NOR flash memory cells. The current consists of the conventional current path (solid arrow) and the side conduction path shown by the dashed arrow. Since the electron current is flowing from the width, length, and bottom (deep N-well) directions, more than 15% read conduction current enhances the read performance. The typical operating conditions for Bi-NOR cell are listed in Table I. Fig. 1(b) shows the read path from an array to the sense amplifier. For a selected cell, since the drains of the flash cells in the same row are connected and biased at 1 V from the source switch, the current has to flow to the sense amplifier at the bitline of the flash cell. Therefore, the bias at the bitline must be close to zero to comply with

Manuscript received March 4, 2004; revised August 1, 2004. This work was supported by NSC of Taiwan, R.O.C., under NSC91-2622-E-007-033.

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Digital Object Identifier 10.1109/JSSC.2004.840965

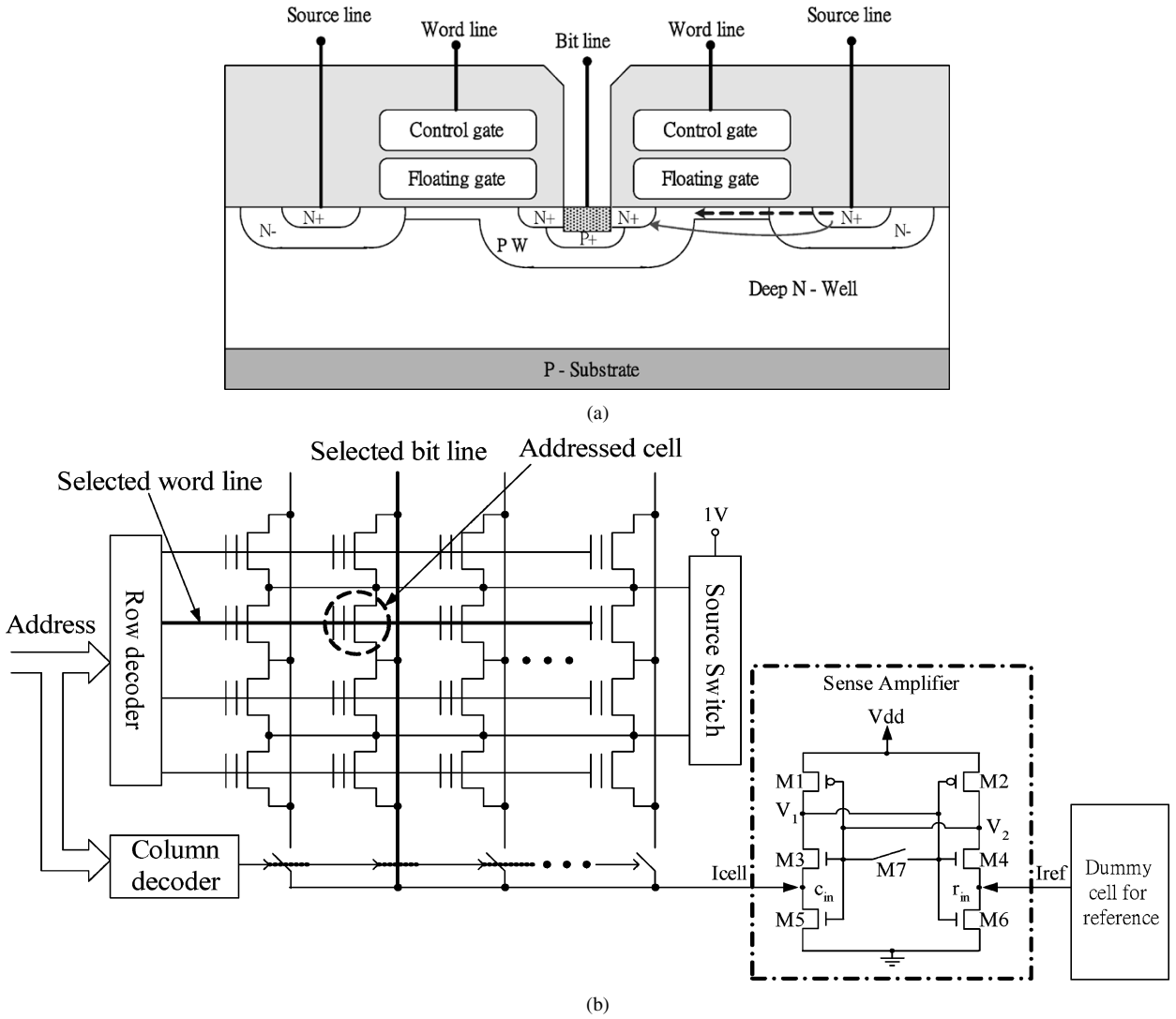

Fig. 1. (a) Cross-sectional view of the Bi-NOR flash memory cell. (b) The read path in an array organization.

TABLE I
TYPICAL OPERATING CONDITIONS FOR THE BI-NOR CELL

Operation	Bit line		Word line		Source line	Deep N-Well
	Select	unselect	select	unselect		
Program	6V	0V	-10V	0V	Float	Float
Erase	Float	Float	18V	0V	0V	0V
Read	0V	1V	4V	0V	1V	1V

the requirement. This new operation makes most of the sense amplifiers designed for the conventional flash cell arrays not appropriate for the new cell array.

Generally, the sensing circuit is composed of a current source transporting the cell's contents through the bitline to the data line, and a latch stage converting the differential current in the data line to the output node. According to the Bi-NOR cell array mentioned above, the new current-mode sense amplifier shown in Fig. 2(a) employs the cross-coupled latch structure (M1–M4) with sensor activation (Men) and equalization of output nodes (M7). Transistors M5 and M6 clamp the bitline voltage close to ground, and the sensing nodes (c_{in} and r_{in}) drain currents from the selected cell and the reference cell, respectively. The $R_{bitline}$ and $C_{bitline}$ represent the parasitic resistance and capacitance at the bitline. The timing diagram of signals SE, En, Nodes a, b, and out for the new sense amplifier is illustrated in Fig. 2(b).

The operation of the sense amplifier can be divided into three phases: pre-charge, signal amplification, and reset for the next operation. In the pre-charge phase, the appropriate signals are applied to force the sensing nodes to certain potentials. In the amplification phase, the comparison and amplification are executed between the sensing nodes, so the content of the selected memory cell is retrieved. After that, the sense amplifier is reset for the next operation.

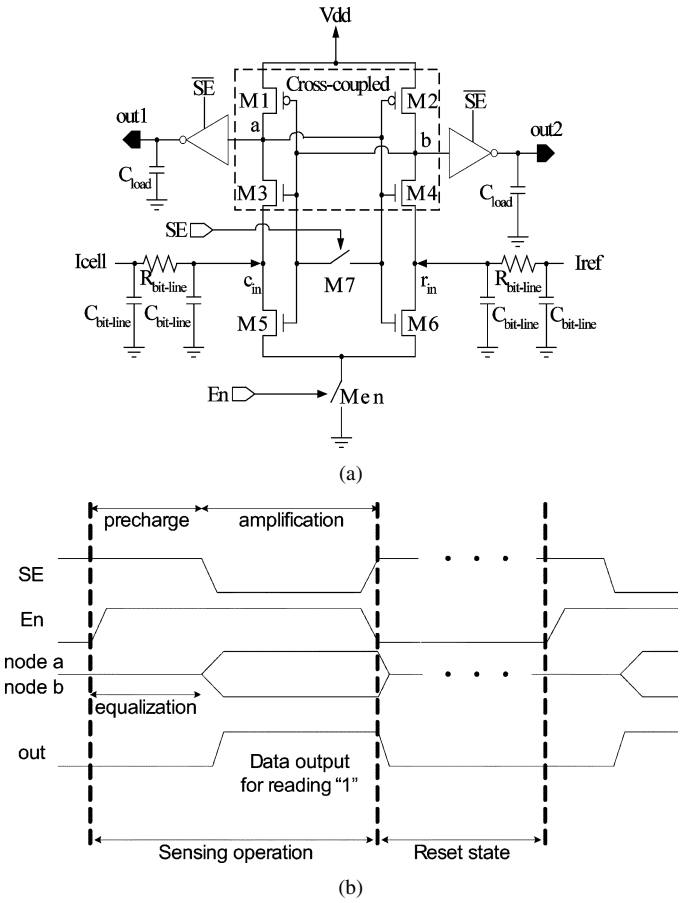

Fig. 2. (a) Circuit diagram of the new sense amplifier. (b) Timing diagram for the operation of the new sense amplifier.

The sensing operation starts by turning on Switch Men and Switch M7. During the pre-charge phase, the output node voltages are equalized ($V\mathrm{a}{=}V\mathrm{b}$) so that the currents in M1 and M2 are the same. For the case of $I_{\mathrm{cell}} > I_{\mathrm{ref}}$, the current through M5 will be larger than that of M6 ($I_{\mathrm{M5}} > I_{\mathrm{M6}}$). Therefore, the bias at Node $\mathrm{c_{in}}$ is slightly higher than that at $\mathrm{r_{in}}$. In the meanwhile, since M3 and M4 are all in the saturation region, the gate to source voltage (V_{gs}) of M3 is less than that of M4 ($V_{gs3} < V_{gs4}$), the current through M3 is smaller than that of M4 ($I_{\mathrm{M3}} < I_{\mathrm{M4}}$).

At the end of the pre-charge cycle, M7 is turned off, so transistors M1–M4 act as a high-gain positive feedback amplifier. Due to positive feedback, the impedance looking into the source node of either M3 or M4 is negative. That makes M3 and M4 begin to source the currents when M7 is turned off. Since M4 has stronger ability than M3 does to discharge the voltage at the node b, the different currents flowing through the drains of transistors M3 and M4 amplify the voltage difference across the output nodes (a and b) of the sensing amplifier. During the pre-charge phase, it is important that the sizes of clamping transistors M5 and M6 should be chosen slightly larger to allow them biased in linear region, thus activating the regeneration procedure of inverter pairs (M1/M3 and M2/M4) as a latch in the later amplification phase.

Since the inputs of the sense amplifier are low-impedance current sensing nodes, the high capacitive bitlines only need to be charged slightly for sensing operation. This results in the minimal influence of the sensing speed for various bitline capacitances and current differences. In addition, due to the fact that the potentials of bitlines always keep low during the sensing operation, power consumption is significantly reduced. Another important feature is improvement of the mismatch problem, which will be explained in the next section.

III. Performance Evaluation

The new sensing circuit was designed and fabricated using 0.25-μm Bi-NOR flash memory technologies with 0.4-μm CMOS transistors with threshold voltage $|V_t| \cong 0.8$ V for peripheral circuits at supply voltage of 1.8 V. Fig. 3(a) shows the simulated waveforms of the signal SE, the nodes a, b, and out of the proposed sense amplifier in the case of $I_{\mathrm{cell}} > I_{\mathrm{ref}}$ with the output load capacitance of 20 fF. The simulation results show the sensing speed is about 2.3 ns for the current difference ($\Delta I = I_{\mathrm{cell}} - I_{\mathrm{ref}}$) of 6.5 μA. Fig. 3(b) gives the waveforms of current input nodes with bitline resistance of 320 Ω and capacitance of 2 pF for the flash cell ($\mathrm{c_{in}}$) and the reference cell ($\mathrm{r_{in}}$). As mentioned before, the potentials at the sources of the cells are pretty low. They are pre-charged to 0.5 V at $\mathrm{c_{in}}$ and 0.1 V at $\mathrm{r_{in}}$ for the pre-charging time of 30 ns.

In order to evaluate the proposed design, the clamped bitline (CBL) sense amplifier [13] illustrated in Fig. 4(a) is compared. Its small-signal equivalent model for the typical cross-coupled circuit is given in Fig. 4(b), in which Cd is the equivalent capacitance at the output nodes of the sense amplifier including the Miller capacitance from the diffusion capacitances $\mathrm{C_{gd}}$, and Rd includes the parallel combination of the output resistances of both n-channel and p-channel transistors. The clamp transistors M5 and M6 are biased in the linear region with equivalent capacitances Cs and conductance g_{ds}. Resistors $\mathrm{R_{12}}$ and $\mathrm{R_{34}}$ mimic the small impedances of switches during the equalization phase. For the current difference $\Delta I = I_{\mathrm{cell}} - I_{\mathrm{ref}} > 0$, the voltage difference between Nodes $\mathrm{c_{in}}$ and $\mathrm{r_{in}}$ is defined as $\Delta V = V_3 - V_4$. For the CBL sense amplifier, ΔV_{CBL} is

$$\Delta V_{CBL} \cong \frac{1}{g_{ds}} \left[(I_{\mathrm{cell}} + I_{M3} - \Delta I_{34}) - (I_{\mathrm{ref}} + I_{M4} + \Delta I_{34}) \right] \quad (1)$$

where g_{ds} is the drain-source conductance of M5 and M6 and ΔI_{34} is the current through $\mathrm{R_{34}}$.

On the other hand, the new sense amplifier with the gates M5 and M6 are connected to the cross-coupled nodes, and the currents through the flash cell, M3, and M4 are denoted as I'_{cell}, I'_{M3}, and I'_{M4}, respectively. Therefore, the voltage difference of proposed circuit ΔV_{NSA} between $\mathrm{c_{in}}$ and $\mathrm{r_{in}}$ without ΔI_{34} term becomes

$$\Delta V_{NSA} \cong \frac{1}{g_{ds}} \left[(I'_{\mathrm{cell}} + I'_{M3}) - (I_{\mathrm{ref}} + I'_{M4}) \right]. \quad (2)$$

For the same sense amplification capability, $\Delta V_{CBL} = \Delta V_{NSA}$, (1) should be equal to (2):

$$\lfloor (I_{\mathrm{cell}} + I_{M3} - \Delta I_{34}) - (I_{\mathrm{ref}} + I_{M4} + \Delta I_{34}) \rfloor \cong \lfloor (I'_{\mathrm{cell}} + I'_{M3}) - (I'_{\mathrm{ref}} + I'_{M4}) \rfloor. \quad (3)$$

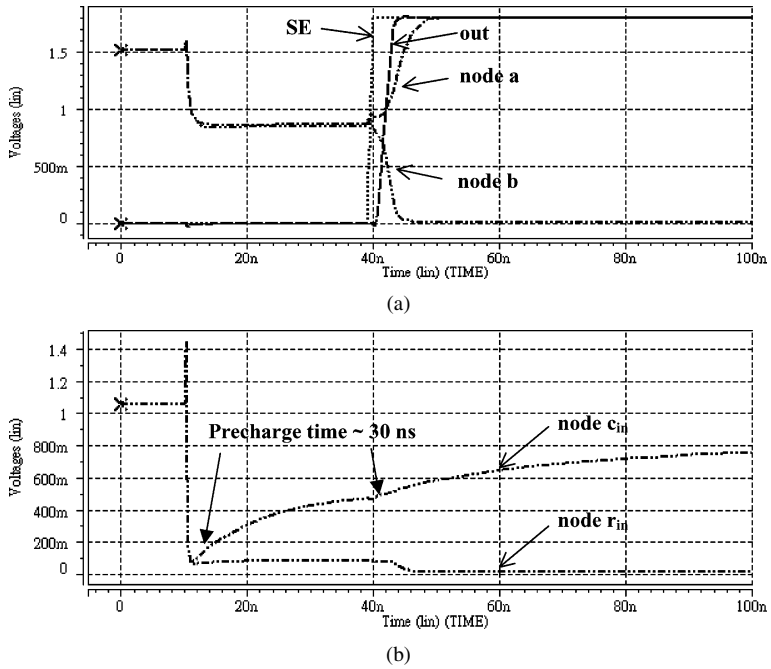

Fig. 3. (a) Simulated waveforms of Signal SE, out, Nodes a and b of the new sense amplifier. (b) Simulated waveforms of Nodes c_{in}, and r_{in} of the new sense amplifier.

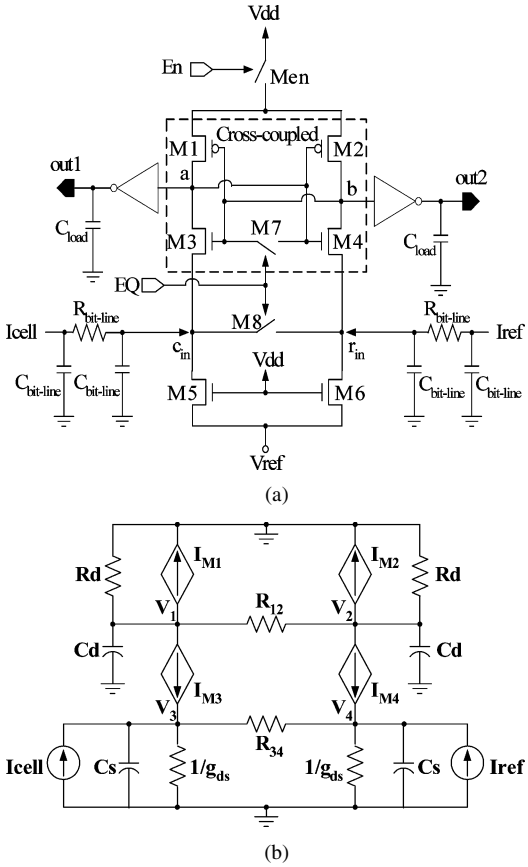

Fig. 4. (a) Circuit diagram of the clamped bitline sense amplifier. (b) Equivalent circuit with M5/M6 denoted as resistors of $1/g_{ds}$.

If we assume $I_{M3} - I_{M4} = I'_{M3} - I'_{M4}$ before the amplifier, it means

$$(I_{\text{cell}} - I_{\text{ref}}) - 2(\Delta I_{34}) \cong (I'_{\text{cell}} - I_{\text{ref}}). \tag{4}$$

It clearly shows that the CBL sense amplifier requires more current difference to compensate the offset [14], since $\Delta I_{34} > 0$ due to $\Delta I = I_{\text{cell}} - I_{\text{ref}} > 0$. The basic difference of the proposed and the CBL sense amplifiers relies on the fact that the equalization device of the proposed circuit is not placed in the current path during the pre-charge phase. Thus, the proposed circuit provides faster response time and better mismatch immunity than the CBL sense amplifier.

The following comparisons were carried out with the same fan-in and fan-out conditions for both circuits with the transistor sizes listed in Table II. Fig. 5 compares the sensing speed and average power dissipation as functions of the current difference for given bitline resistance of 320 Ω and capacitance of 2 pF at $V_{\text{dd}} = 1.8$ V and switch frequency of 25 MHz. The simulations were performed for the current difference of the flash cell (I_{cell}) and the reference cell (I_{ref}) equal to $3 \sim 10$ μA. As expected, the more current difference results in the faster sensing speed. It is obvious that the proposed circuit provides much faster sensing speed and less power consumption compared to the CBL sensing circuits. The reason is that the proposed sense amplifier does not consume sensing current of the cells to either compensate the current path (ΔI_{34}) offset or maintain low biases at c_{in} and r_{in}, thus incurs less power dissipation.

The comparison of sensing speed versus bitline capacitance between the proposed and the CBL sense amplifier for the typical, best and worst transistor models with current difference of 10 μA at $V_{\text{dd}} = 1.8$ V is illustrated in Fig. 6. According to the simulations both sense amplifiers exhibit almost constant sensing delay independent of the bitline load capacitance, since both amplifiers separate the outputs and the bitlines. However, the new circuit has variation of 14% between the typical and the best/worst cases, while the CBL has variation of 22%. The sensing time as functions of pre-charging time for variations in the capacitance and resistance of the bitlines in the memory cell

TABLE II
TRANSISTOR W/L SIZES FOR THE NEW AND THE CBL SENSE AMPLIFIERS

Transistor	NSA	CBL
M1, M2	2 μ / 0.55 μ	
M3, M4	8 μ / 0.55 μ	
M5, M6	25 μ / 0.65 μ	
M7, Men	25 μ / 0.55 μ	
M8	NA	25 μ / 0.55 μ

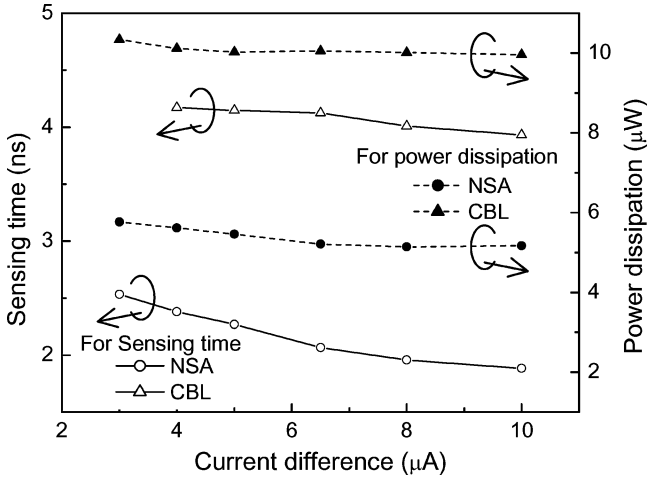

Fig. 5. Simulated sensing speed and average power dissipation for various current differences (ΔI).

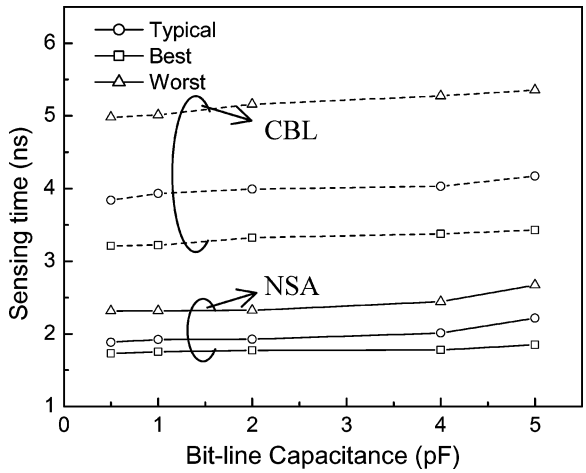

Fig. 6. Sensing speed versus bitline capacitance for different process corners for bitline resistance of 320 Ω.

array is plotted in Fig. 7. In general, the shorter pre-charging time takes the longer sensing time. It can be observed that the pre-charging time is longer with heavier capacitance. However, the variation is not large. Note that the sensing time is barely affected by the resistance variation.

The mismatch in W/L ratio or threshold voltage plays a critical role in the symmetric cross-couple sense amplifiers, since it may result in erroneous sensing output. A simplified model shown in Fig. 8 explains the effect of mismatch in the sensing

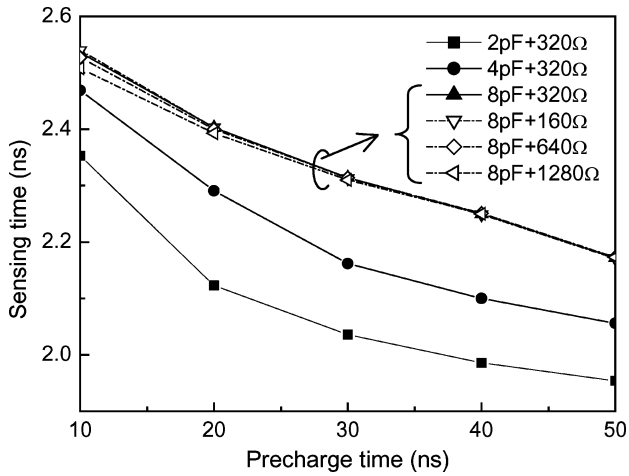

Fig. 7. Sensing speed versus pre-charging time with respect to various bitline resistance and capacitance.

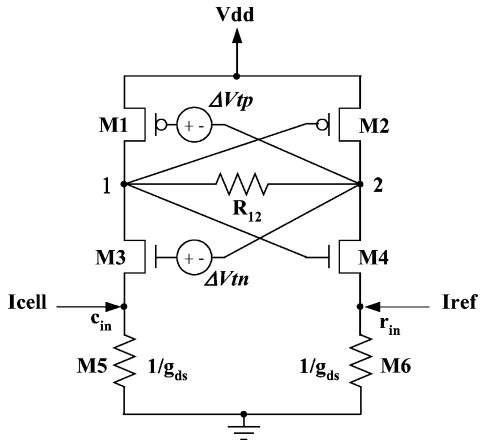

Fig. 8. Equivalent circuit of the new sense amplifier with threshold voltage mismatches.

operation. The ΔV_{tp} and ΔV_{tn} represent the threshold voltage mismatch of PMOS and NMOS transistors, respectively, while g_{ds} denotes as the identical drain to source channel conductance of M5 and M6. By assuming no mismatch of M5 and M6 in the following analysis, the worst polarity for the offset voltage in threshold voltage at the regenerative nodes (Nodes 1 and 2) may be expressed as

$$V_{\text{offset}} = \Delta V_{tn} + \Delta V_{tp} = (g_{mn}\Delta V_{tn} + g_{mp}\Delta V_{tp}) \cdot \mathrm{R}_{12} \quad (5)$$

where g_{mn} and g_{mp} are the transconductances of PMOS and NMOS transistors, and the offset voltage in threshold voltage mismatch is translated into a current mismatch at the drain with a gain of g_m through resistance R_{12}. Since the current difference between the selected cell and reference cell $\Delta I = I_{\text{cell}} - I_{\text{ref}}$, which results in a differential voltage V_{diff} representing the data of selected cell to be read. V_{diff} can be written as

$$V_{\text{diff}} = \Delta I \cdot R_{12}. \quad (6)$$

The ratio of the differential voltage across the differential nodes to the offset voltage called safety margin is defined as [15]

$$\text{Margin} = \frac{V_{\text{diff}}}{V_{\text{offset}}} = \frac{\Delta I}{g_{mn}\Delta V_{tn} + g_{mp}\Delta V_{tp}} \equiv \frac{\Delta I}{I_{\text{offset}}} \quad (7)$$

where I_{offset} is effective offset current, which equals to $g_{mn}\Delta V_{tn} + g_{mp}\Delta V_{tp}$.

The safety margin depends on the transconductance and threshold voltage mismatch of the cross-coupled devices. When switch M7 is on, the currents through M3 and M4 can be approximated as

$$I_{\text{M3}} \cong \frac{\mu_n C_{\text{ox}} W}{2L}(V_{gs3} - V_{tn})^2 = I_{\text{M4}} \cong \frac{\mu_n C_{\text{ox}} W}{2L}(V_{gs4} - V_{tn})^2 . \tag{8}$$

where μ_n is the electron mobility, C_{ox} is the gate capacitance, and V_{tn} is the threshold voltage of NMOS.

In the case of threshold voltage mismatch shown in Fig. 8, the current through M3 is denoted as $I_{\text{M3(mismatch)}}$ varied by a mismatch ΔV_{tn}

$$I_{\text{M3(mismatch)}} \cong \frac{\mu_n C_{\text{ox}} W}{2L}(V_{gs3} - V_{tn} + \Delta V_{tn})^2 . \tag{9}$$

For $I_{\text{cell}} > I_{\text{ref}}$, the source of M3 is charged by a voltage on sensing node c_{in} denoted as V_{cin}, therefore (9) can be rewritten as

$$\begin{aligned} I_{\text{M3(mismatch)}} &\cong \frac{\mu_n C_{\text{ox}} W}{2L}[V_{g3} - (V_{s3} + V_{cin}) - V_{tn} + \Delta V_{tn}]^2 \\ &\cong \frac{\mu_n C_{\text{ox}} W}{2L}[V_{g3} - V_{s3} - V_{tn} + (\Delta V_{tn} - V_{cin})]^2 \\ &\cong \frac{\mu_n C_{\text{ox}} W}{2L}[V_{gs3} - V_{tn} + (\Delta V_{tn} - V_{cin})]^2 \end{aligned} \tag{10}$$

where the V_{g3} and V_{s3} are gate and source voltages of M3, respectively. The threshold voltage mismatch for the proposed circuit is reduced due to the term $(\Delta V_{tn} - V_{cin}) \equiv \Delta V_{tn(NSA)}$ in (10). According to the safety margin definition in (7), $\Delta I/\Delta I_{\text{offset}}$, either the more current difference ΔI or the less offset current benefits the sensing operation in case of mismatch arising. The proposed circuit charges the sensing node c_{in} to reduce the offset current ΔI_{offset} with the term of $(\Delta V_{tn} - V_{cin})$ instead of ΔV_{tn} in (10). However, the CBL sense amplifier does not have this effect due to equalization between c_{in} and r_{in}. Therefore, with the same current difference for amplification, the proposed circuit is superior to the CBL sense amplifier for mismatch improvement.

Since the threshold voltage mismatch can be equivalent to the geometry (W/L ratio) mismatch [15], the worst-case mismatch may be obtained by tuning the possible worse cases at the same time. Therefore, the sensing circuits were simulated using the center dimensions given in Table II with channel length mismatches on M1, M4, and M6, which were selected as $L_{\text{M1}} = L_{\text{M2}} + \Delta L$, $L_{\text{M4}} = L_{\text{M3}} + \Delta L$, and $L_{\text{M6}} = L_{\text{M5}} + \Delta L$, respectively, where ΔL is the channel length mismatch. The sensing speed slightly degrades with channel length mismatch up to $\Delta L = 0.05\ \mu$m for the new sensing circuit, while the CBL sense amplifier cannot afford mismatches beyond $0.015\ \mu$m in case of current difference $\Delta I = 10\ \mu$A at the pre-charging time of 50 ns, as shows in Fig. 9. On the contrary, for the case of $I_{\text{cell}} < I_{\text{ref}}$, the mismatch seems not critical, since the mismatch helps the sensing operation.

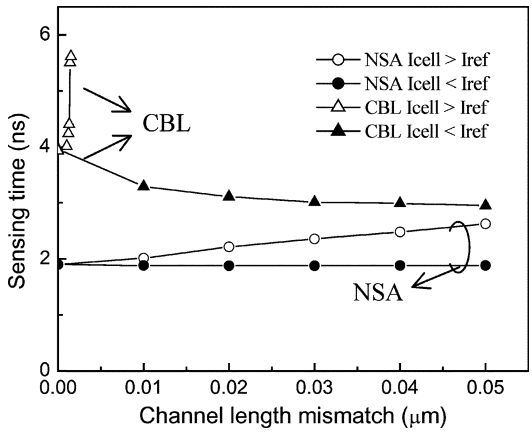

Fig. 9. Sensing speed versus channel length mismatch for $I_{\text{cell}} > I_{\text{ref}}$ and $I_{\text{cell}} < I_{\text{ref}}$ for current difference of 10 μA, and pre-charging time of 50 ns.

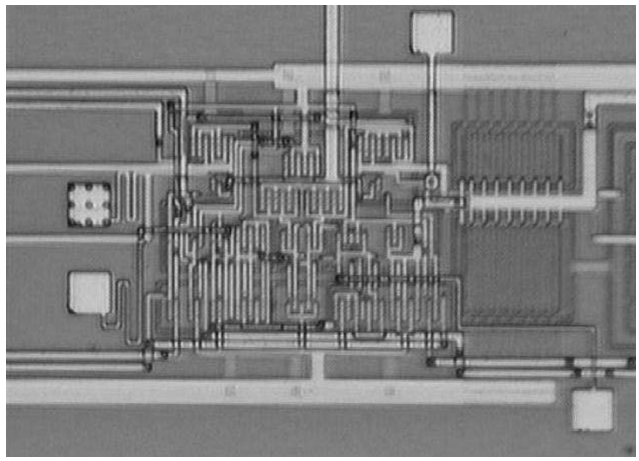

Fig. 10. Chip microphotograph of the new sense amplifier.

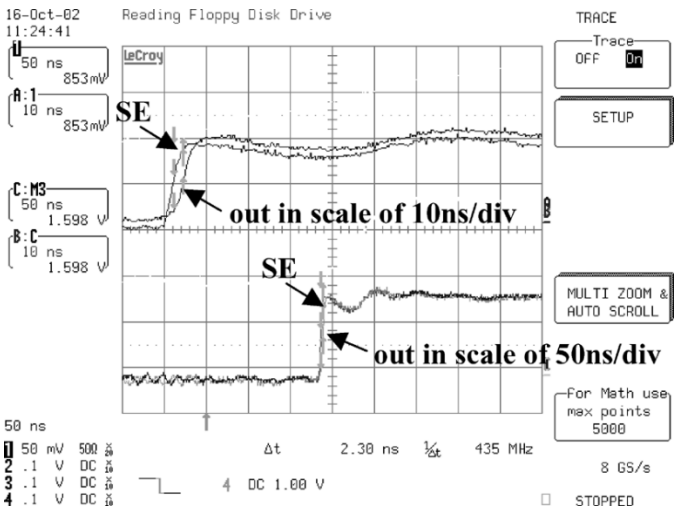

Fig. 11. Measured delay time between the signal SE and node out.

IV. Experimental Results

The chip microphotograph of the new circuit fabricated using 0.25-μm Bi-NOR flash memory with 0.4-μm CMOS for peripheral circuits is presented in Fig. 10. The test chip was designed

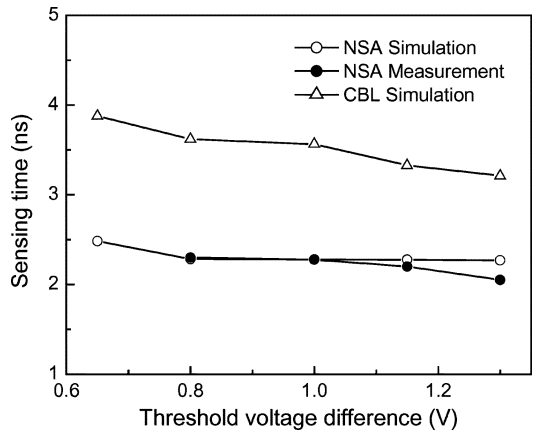

Fig. 12. Sensing speed versus various threshold voltage differences (ΔV).

using the currents generated from the selected cell and reference cell. Each has resistor 320 Ω and two parallel capacitors of 2 pF in between to mimic the parasitic effects in the memory arrays. The cell currents are obtained by applying 1 V to the drains of the selected cell and reference cell with different wordline voltages to the gates of the cells. Since the wordline voltage difference between the selected cell and the reference cell was assumed to be equivalent to the threshold voltage differences between them, the current difference resulted from varying the wordline voltage of the reference cell. Fig. 11 demonstrates that the on-chip measured delay time between the signals SE and output node for the new sense amplifier is about 2.3 ns when the threshold voltage difference is 0.8 V.

The comparison of the sensing delay times between simulation and measurement for the given threshold voltage difference from 0.8 to 1.3 V is shown in Fig. 12. The CBL sense amplifier needs more current difference to compensate the offset, so it takes longer sensing time. The new sense amplifier with the currents slightly charging the sensing nodes before sensing makes the response time shorter. The agreement between measurement and simulation is also observed.

V. Conclusion

A new low-power sensing circuit for 0.25-μm Bi-NOR flash memory technology was designed and measured. The proposed scheme presents outstanding performance with sensing speed reaches 2 ns and power consumption less than 6 μW at switch frequency of 25 MHz and supply voltage of 1.8 V. With the special connection of the gates to the cross-coupled output nodes, the immunity to device mismatch is improved significantly. That also makes the new current-mode sense amplifier much easier to design and fabricate. According to these analyses, it has also proven that the sensing delay of the new sense amplifier is almost independent of the bitline capacitance, which indicates that it is an excellent candidate for higher density memory.

Acknowledgment

The authors would like to acknowledge Power Semiconductor Corporation and eMemory Inc. for their support in chip fabrication and measurement, respectively.

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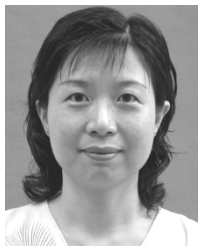

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