A Simple Subthreshold CMOS Voltage Reference Circuit With Channel- Length Modulation Compensation

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***Abstract*—This brief presents a simple reference circuit with channel-length modulation compensation to generate a reference voltage of 221 mV using subthreshold of MOSFETs at supply voltage of 0.85 V with power consumption of 3.3 μW at room temperature using TSMC 0.18-μm technology. The proposed circuit occupied in less than 0.0238 mm ^{2} achieves the reference voltage variation of 2 mV/V for supply voltage from 0.9 to 2.5 V and about 6 mV of temperature variation in the range from −20°C to 120 °C. The agreement of simulation and measurement data is demonstrated.**

***Index Terms*—Compensation, channel-length modulation, reference voltage, subthreshold.**

I. Introduction

In many applications, a precise and stable reference voltage is widely used in digital and analog circuits like analog–digital (A/D) and digital–analog (D/A) converters, voltage regulators, DRAM/flash memories and other communication devices. The demands for smaller area, low power consumption and low sensitivity to the supply voltage ($V_{\rm dd}$) and temperature are getting increased. Recently, the voltage reference circuits were proposed to achieve smaller area without resistors [1], or low power supply, such as 1 V [2], [3]. However, all of them require big-area diodes or parasitic bipolar junction transistors (BJTs) with turn-on voltage as high as 0.6 V at room temperature. Thus, some people started to exploit MOSFETs operated in subthreshold region to generate the reference voltage independent of the power supply and temperature, while reduce the chip area and power dissipation [4], [5]. However, the former one [4] is focused on constant reference current. It requires a thermal-independent grounded resistor to convert to the desired reference voltage. The latter [5] can generate a good reference voltage, but is more complicated than the one proposed in this brief.

II. Design Principles

The subthreshold characteristics of MOSFETs [5], [6] are briefly explained in this section. When $V_{\rm GS} < V_{\rm TH}$, the drain current I_D is quite small but nonzero, where $V_{\rm TH}$ is the threshold voltage. It exhibits an exponential dependence on $V_{\rm GS}$. This effect can be formulated for $V_{\rm DS}$ greater than roughly 200 mV

$$I_D = I_0 \exp \frac{V_{\rm GS}}{\zeta V_T} \tag{1}$$

where $\zeta > 1$ is a non-ideal factor and $V_T = KT/q$. The above equation can be rewritten as

$$V_{\rm GS} = \zeta V_T \ln\left(\frac{I_D}{I_0}\right). \tag{2}$$

From the above equation, we know $V_{\rm GS}$ is a positive-temperature coefficient voltage if I_D/I_0 remains constant but it relies on some circuit technique to achieve.

If the MOSFET is in subthreshold region, the relation between $V_{\rm GS}$ and $V_{\rm TH}$ as a function of temperature is [5]

$$V_{\rm GS}(T) = V_{\rm TH}(T) + V_{\rm OFF} + \frac{n(T)}{n(T_0)} \times [V_{\rm GS}(T_0) - V_{\rm TH}(T_0) - V_{\rm OFF}]\frac{T}{T_0} \tag{3}$$

where, $n(T) = 1 + C_d/C_{\rm ox}$ is the subthreshold slope factor and $V_{\rm OFF}$ is a corrective constant term used in BSIM3v3 models [7]. By assuming $n(T)$ only varied slightly with temperature, which means $n(T) \approx n(T_0)$, the threshold voltage can be modeled as $V_{\rm TH}(T) = V_{\rm TH}(T_0) + K_T(T/T_0 - 1)$, where $K_T < 0$. Therefore, $V_{\rm GS}$ can be approximated as

$$V_{\rm GS}(T) \approx V_{\rm GS}(T_0) + K_G\left(\frac{T}{T_0} - 1\right) \tag{4}$$

where $K_G \cong K_T + V_{\rm GS}(T_0) - V_{\rm TH}(T_0) - V_{\rm OFF}$. The quantity K_G is negative, so $V_{\rm GS}$ is decreased with the temperature. By combining the effects of (2) and (4), the reference voltage independent of the temperature can be obtained.

III. Proposed Circuit and Analysis

A new less complicated circuit than that presented in [5] is proposed in Fig. 1. The circuit in Fig. 1 can be divided into three parts. The first part is made of transistors M1 to M5 and resistor R_1. The second part includes M6 to M9 and resistor R_2. The

Manuscript received February 17, 2005; revised November 21, 2005. This work was supported by the National Science Council (NSC) of Taiwan, R.O.C. under Grant NSC-92-2622-E-007-002 and Grant NSC92-2220-E-005-005. This paper was recommended by Associate Editor W. Porod.

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Digital Object Identifier 10.1109/TCSII.2006.881813

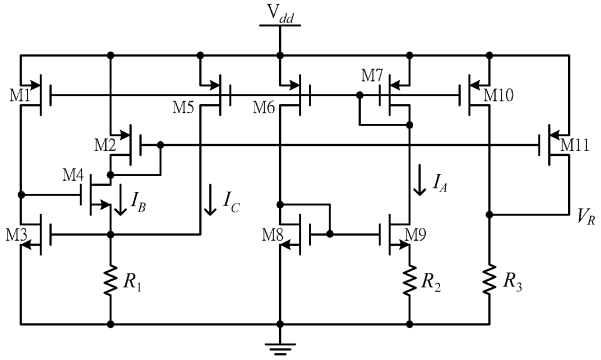

Fig. 1. Schematic of the proposed voltage reference circuit.

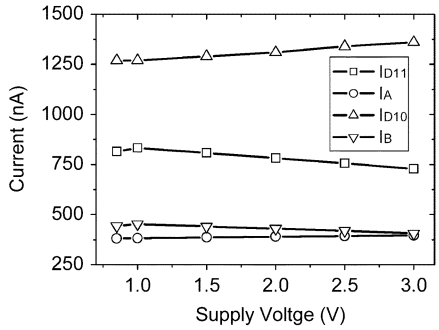

Fig. 2. Currents I_A, I_B, I_{D10}, and I_{D11} indicated in Fig. 1 as functions of supply voltage.

last part is composed of transistors M10, M11 and resistor R_3 to generate the reference voltage V_R.

A. Circuit Analysis

To analyze the circuit, we start from the current I_A in the second part. It is generated by transistors M8, M9 in subthreshold region to obtain a current independent of power supply variation. With $V_{\rm GS8} = V_{\rm GS9} + I_A R_2$ and the relation from (2), the following expression can be obtained:

$$I_A = \frac{\varsigma V_T}{R_2} \ln\left(\frac{P_9}{P_8}\right) \tag{5}$$

where $P \equiv W_{\rm eff}/L_{\rm eff}$ and transistors M6 and M7 are assumed to be identical. Obviously, I_A provides a proportional-to-absolute temperature (PTAT) current.

In the first part, transistor M1 mirrors the current I_A to generate $V_{\rm GS3}$, which is used to produce $I_B = V_{\rm GS3}/R_1$ if $I_C = 0$. From (4), we know I_B gives a negative-temperature coefficient. It is important to note that the transistor M3 should be operated in subthreshold region.

The drain current of M5 mirroring N times of current I_A is expressed as $I_C = NI_A$. It is used to compensate channel-length modulation to be explained below. I_B can be written as (6). It means increment of I_C results in decrement of I_B due to constant $V_{\rm GS3}$

$$I_B = \frac{V_{\rm GS3}}{R_1} - I_C. \tag{6}$$

After I_A and I_B mirror to M10 and M11, we have the reference voltage V_R given as

$$V_R = \left(\frac{P_{10}}{P_7} I_A + \frac{P_{11}}{P_2} I_B\right) \times R_3. \tag{7}$$

By substituting (5) and (6) into (7), we have

$$V_R = \alpha V_{\rm GS3} + \beta V_T \tag{8}$$

where $\alpha = (P_{11}R_3/P_2R_1)$ and $\beta = ((P_{10}/P_7) - N(P_{11}/P_2))(R_3/R_2)\zeta \ln(P_9/P_8)$. To obtain a constant V_R, i.e., $\partial V_R/\partial T = 0$, the following condition must be satisfied to achieve a zero-temperature coefficient:

$$\frac{\alpha}{\beta} = -\frac{T_0}{K_G} \cdot \frac{K}{q}. \tag{9}$$

TABLE I
PARAMETERS OF TRANSISTORS AND RESISTORS USED IN THE PROPOSED VOLTAGE REFERENCE CIRCUIT

name	W/L (μm)	name	W/L (μm)
M1	40/8	M10	160/12
M2	20/8	M11	16/12
M3, M4	50/2		
M5	3/0.5	name	Resistance (kΩ)
M6, M7	25/6	R1	250
M8	2/2	R2	350
M9	100/2	R3	130

B. Compensation of Channel Length Modulation

The current I_C mirroring N times of I_A may help reduce the channel-length modulation effect. The following gives the reason.

$I_B = (V_{\rm GS3}/R_1) - NI_A$ can be obtained, after $I_C = NI_A$ is substituted into (6). Thus, (7) becomes

$$V_R = \left[\frac{P_{10}}{P_7} I_A + \frac{P_{11}}{P_2}\left(\frac{V_{\rm GS3}}{R_1} - NI_A\right)\right] \times R_3. \tag{10}$$

Since $(V_{\rm GS3}/R_1) = (\zeta V_T/R_1)\ln(I_{D3}/I_0)$, the derivative with respect to V_{dd} is

$$\frac{\partial (V_{\rm GS3}/R_1)}{\partial V_{dd}} = \frac{\zeta V_T}{I_{D3}R_1}\frac{\partial I_{D3}}{\partial V_{dd}} = \frac{\zeta V_T}{I_{D3}R_1}\frac{P_1}{P_7}\frac{\partial I_A}{\partial V_{dd}}. \tag{11}$$

By taking the derivative of (10) with respect to V_{dd}, the following expression may be derived:

$$\frac{\partial V_R}{\partial V_{dd}} = \left[\frac{P_{10}}{P_7} - \frac{P_{11}}{P_2}N + \frac{P_{11}}{P_2}\frac{P_1}{P_7}\frac{\zeta V_T}{I_{D3}R_1}\right] \times R_3 \times \frac{\partial I_A}{\partial V_{dd}} \tag{12}$$

From the above equation, it can be observed that the minus sign in front of $(P_{11}/P_2)N$ helps reduce the variation of V_R due to the channel-length modulation effect of I_A.

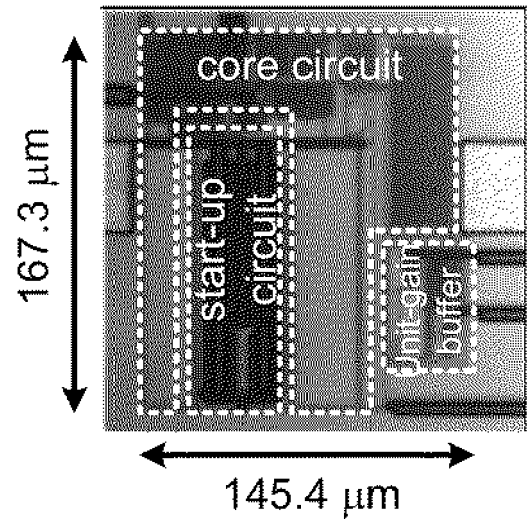

Fig. 3. Die photo of the proposed circuit.

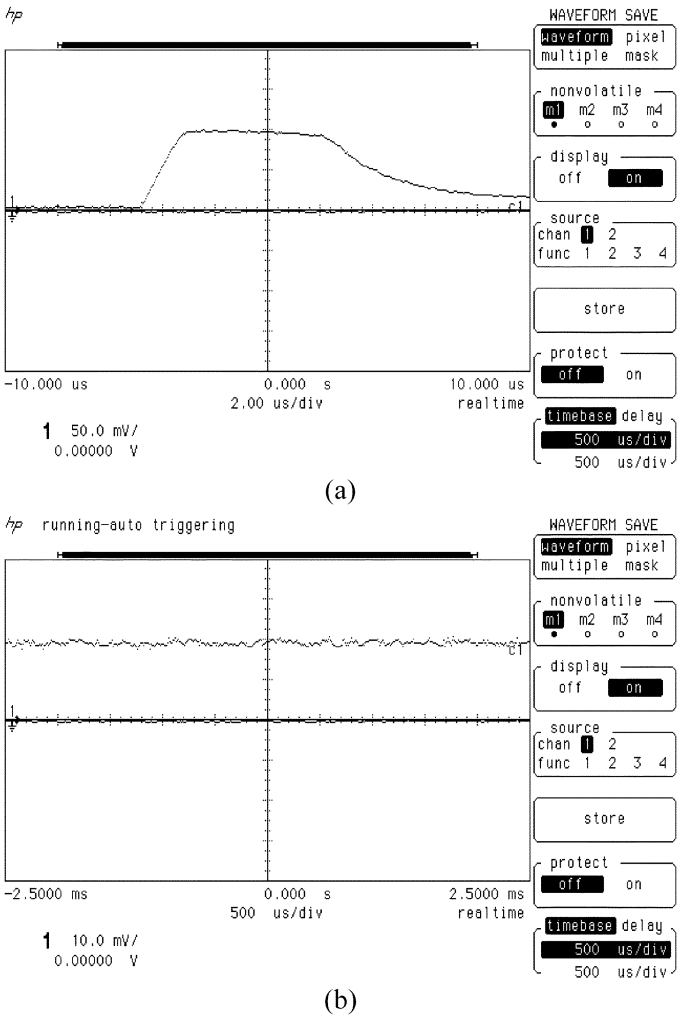

Fig. 4. (a) The $V_{\rm ref}$ output waveform during the start-up period. (b) The constant reference voltage waveform after the circuit reaching the steady state.

Note that even though the factor N can be used to compensate channel-length modulation, it can not be selected to be too large so that Transistors M2 and M4 can not have the reasonable current for conduction.

Fig. 2 demonstrates the simulated currents I_A and I_{D10} are increased when V_{dd} is increased, where I_{D10} is the current of transistor M10. However, I_C helps I_B and I_{D11} decreased instead of increased, where I_{D11} is the current of transistor M11. The opposite trends of I_{D10} and I_{D11} compensate each other to minimize V_R increased as V_{dd} is increased.

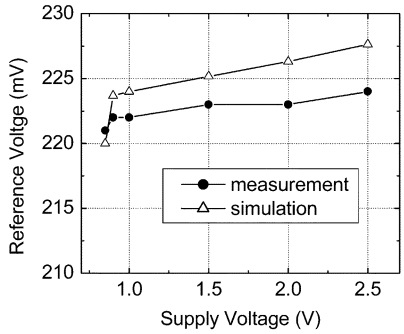

Fig. 5. Simulated and measured reference voltages versus different supply voltages at room temperature.

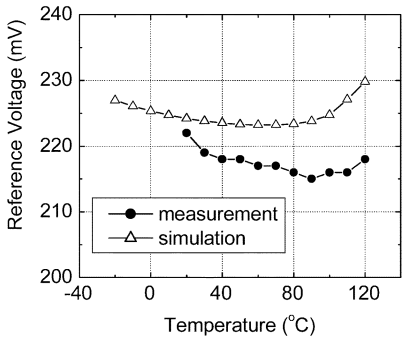

Fig. 6. Simulated and measured reference voltages versus different temperatures at $V_{dd} = 1$ V.

TABLE II
PERFORMANCE SUMMARY OF THE SIMULATED AND MEASURED RESULTS

Parameter	Sim.	Mea.	Units
Supply voltage ($V_{dd\,\min}$)	1	0.85	V
Power consumption	4.2	3.3	μW
Nominal V_{ref}	224	221	mV
V_{ref} sensitivity to V_{dd}	3	2	mV/V
V_{ref} sensitivity to temperature	6	6	$mVp\text{-}p$
Die area	0.0238		mm^2

IV. Simulation and Measurement Results

The new voltage reference circuit was fabricated using TSMC 0.18-μm technology with threshold voltages of nMOS and pMOS to be 0.461 V and −0.439 V at room temperature. The device parameters are listed in Table I. The output voltage is 221 mV with the average power dissipation of 3.3 μW at the

lowest supply voltage $V_{dd} = 0.85$ V. The sensitivity to power supply (V_{dd}) from 0.9 to 2.5 V is 2 mV/V.

Fig. 3 shows the die photo, the area is only about 0.0238 mm^2 including the core voltage reference circuit, the start-up circuit and the output unit-gain buffer for measurement. Fig. 4 demonstrates the measured waveform with $V_{dd} = 1$ V at room temperature. Fig. 4(a) shows the output jumps to near 1 V when the power is turned on and then approaches to the constant voltage, 222 mV as shown in Fig. 4(b).

Figs. 5 and 6 compare the simulated and measured results for different supply voltages at room temperature and different temperatures at $V_{dd} = 1$ V, respectively. In general, the measured results agree well with the simulation results. The summary of the performance is listed in Table II.

V. Conclusion

A new less complicated low-voltage low-power CMOS reference circuit using subthreshold characteristics with the technique to compensate channel-length modulation is presented. The reference voltage about 222 mV with voltage variation 2 mV/V for $V_{dd} = 0.9$ to 2.5 V and 6 mV peak-to-peak for temperature variation from -20°C to 120 $^{\circ}$C is achieved in the chip area less than 0.0238 mm^2 with minimum power consumption of 3.3 μW.

Acknowledgment

The authors acknowledge the National Chip Implementation Center (CIC) of the National Applied Research Laboratories of Taiwan for their support in chip fabrication.

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