BRIEF PAPER

An 11-bit Single-Ended SAR ADC with an Inverter-Based Comparator for Design Automation

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SUMMARY This paper proposes a low power single-ended successive approximation register (SAR) analog-to-digital converter (ADC) to replace the only analog active circuit, the comparator, with a digital circuit, which is an inverter-based comparator. The replacement helps possible design automation. The inverter threshold voltage variation impact is minimal because an SAR ADC has only one comparator, and many applications are either insensitive to the resulting ADC offset or easily corrected digitally. The proposed resetting approach mitigates leakage when the input is close to the threshold voltage. As an intrinsic headroom-free, and thus low-rail-voltage, friendly structure, an inverter-based comparator also occupies a small area. Furthermore, an 11-bit ADC was designed and manufactured through a 0.35-μm CMOS process by adopting a low-power switching procedure. The ADC achieves an FOM of 181 fJ/Conv.-step at a 25 kS/s sampling rate when the supply voltage V_{DD} is 1.2 V.

key words: *Analog-to-digital converter, successive approximation register ADC, inverter-based, design automation.*

1. Introduction

Mobile applications drive an increased need for circuits with low power consumption, and successive approximation register (SAR) analog-to-digital converter (ADC) architecture offers minimal analog circuit blocks; therefore, in addition to low amounts of power, migrating to advanced low power processes is easy to achieve [1]. Monotonic SAR ADC further improves low power capability by eliminating the MSB-related capacitor [2].

Several flash or flash-based ADCs use inverter-based comparators to obtain high speeds and low power consumption. However, the variation among inverter-based comparators limits flash ADC resolution [3]. A pipelined ADC uses several inverter-based comparators, but the measured result only shows a subcircuit with one inverter-based comparator [4]. One SAR ADC with an inverter-based comparator is designed with non-CMOS technology [5]. The result is a low-speed (i.e., 100 Hz), low-resolution (i.e., 6 bits) design with performance shown only with INL/DNL and without ENOB.

This study originated from designing an ultrasonic indoor positioning system and focused on a single-ended input SAR ADC with an inverter-based comparator. With a single-ended input, designers need not consider signal symmetry. For power supply noise concerns, because the design aims at low power applications, which usually use batteries, the power supply is close to an ideal one, and the noise is not problematic. In the implementation, 20% transistors are used for driving off-chip loadings for measurement purposes. The created supply noise effect was included in the measurement results. With the digital inverter-based comparator replacing the conventional analog comparator [6], the SAR ADC design has only one passive analog block, the capacitor array. Although the structure creates an ADC offset variation, in many cases, the ADC offset is easy to compensate for digitally. Therefore, the structure helps in the design automation environment [7].

2. Proposed Single-Ended SAR ADC

The proposed single-ended SAR ADC structure is illustrated in Fig. 1. One pair of capacitor arrays exists with binary weighting, where Cp9 and Cn9 are the largest capacitors and Cp0, Cpb, Cn0, and Cnb are the smallest capacitors.

At the sampling stage, input Vi is connected to V_{shdac}, switches Sp9, Sp8, …, Sp0 are connected to V_{ref}, and switches Sn9, Sn8, …, Sn0 are connected to V_{gnd}. The inverter-based comparator is equivalent to having V_{shdac} and $V_{th} = 0.5\ V_{ref}$ as inputs.

Fig. 2 depicts the operation, assuming V_i to be larger than $0.5\ V_{ref}$. At the sampling stage, $V_i = V_{shdac}$. Because $V_i > 0.5\ V_{ref}$, Bit 10 is set to 1, and Cp9 is switched to V_{gnd} from the original V_{ref} to reduce V_{shdac} to $V_{shdac} = V_i - 0.25\ V_{ref}$.

Hence, V_{shadc} becomes lower than $0.5\ V_{ref}$, and Bit 9 is set to 0; Cn8 is connected to V_{ref}. Therefore, V_{shdac} is increased to $V_{shdac} = V_i - 0.25\ V_{ref} + 0.125\ V_{ref}$.

In a similar procedure, the remaining bits are set, and V_{shdac} approaches $0.5\ V_{ref}$. This structure maintains the advantage of the monotonic SAR ADC because only one highly sensitive range is required, which is close to $0.5\ V_{ref}$. If $V_{ref} = V_{DD}$, then the input range is rail to rail. The voltage swing of V_{shdac} is from V_i to $0.5\ V_{ref}$, which is smaller than the swing of the conventional monotonic SAR from V_i to ground.

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The structure differs from the capacitor splitting structure mentioned in Ginsburg [8]; here, V_i is connected to V_{shdac} at the sampling stage.

For single-ended ADC structures proposed by [9] and [10], the DAC outputs converge either to one of two fixed voltages [9], or to an input-dependent voltage [10]. These two designs do not always use the highly sensitive range, around V_{th}, of an inverter-based comparator for the LSB comparisons such as the proposed structure does. Therefore, the proposed structure is more effective for high resolution applications.

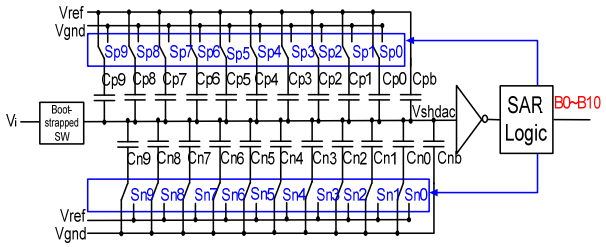

Fig. 1 Proposed SAR ADC structure with an inverter-based comparator.

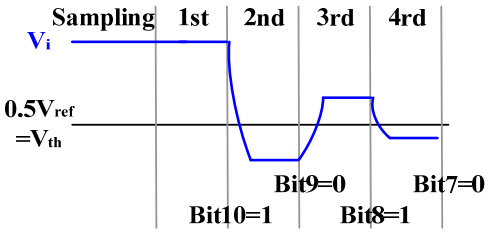

Fig. 2 Comparator input voltage, V_{shdac}, procedure from Bit 10 down to Bit 7.

3. Proposed Single-Ended SAR ADC Switching Power

This section compares the switching power of four single-ended switching procedures. The first is a conventional single-ended switching procedure [6], called the input convergence procedure, because a capacitor array output voltage gradually approaches the original input voltage in the conversion procedure. The second switching procedure is a low power single-ended approach modified from a differential version of [8], and is called a rail convergence procedure because a corresponding capacitor array output voltage gradually approaches the rail voltage. The proposed single-ended switching procedure is known as a half-rail convergence procedure. The last switching procedure is a variation of the proposed procedure: a half-rail with a splitting convergence procedure.

Fig. 3 illustrates the power consumption of each procedure with each fixed input voltage. The average switching energies for input convergence, rail convergence, half-rail convergence, and half-rail with splitting convergence, are 9.90 CV_{REF}^2, 6.625 CV_{REF}^2, 5.78 CV_{REF}^2, and 5.69 CV_{REF}^2, respectively. Compared with input convergence and rail convergence, half-rail convergence reduces energy by 41% and 13%, respectively. The energy consumption difference between half-rail and half-rail with splitting is approximately 1%, and is not discussed here.

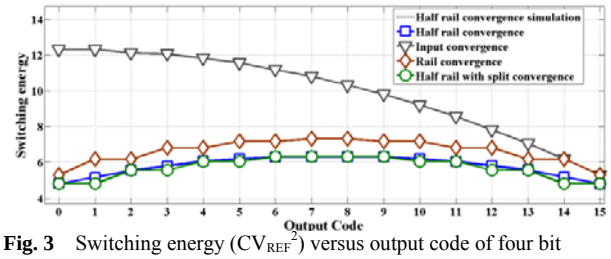

Fig. 3 Switching energy (CV_{REF}^2) versus output code of four bit examples.

4. Inverter-Based Comparator and Sample/Hold Circuit

To increase the final comparator gain, three stages of inverters form the inverter-based comparator, as shown in Fig. 4. To reduce leakage when the input is close to Vth, a resetting mechanism is incorporated into the first stage of the inverter chains through a NAND gate consisting of transistors, M_3–M_6. The reset signal is connected to the bit cycling clock signal, and when the value is high, the drain source path of transistor M_4 is broken, the drain of M_6 is fixed to V_{DD}, and regardless of the V_{IN}, there is no leaking path from V_{DD} to the ground.

Compared with a conventional analog comparator design [6], the proposed inverter-based does not have the headroom problem since none of the MOSFETs needs to be in the saturation region. Therefore, V_{DD} can be very low, and thus, the structure is good for low power.

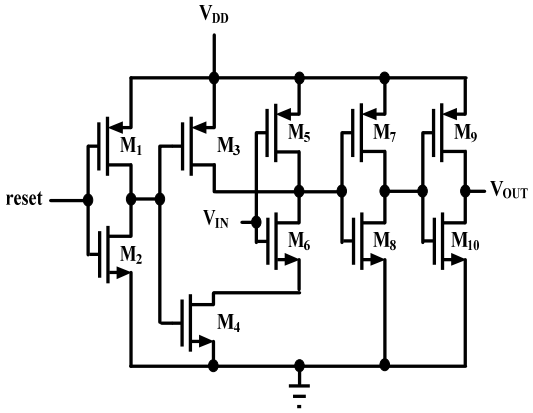

Fig. 4 Inverter-based comparator.

The sample and hold circuit consists of a bootstrapped switch and an equivalent sampling capacitor, C_H, as shown in Fig. 5. The bootstrapped switch [2] reduces the sampling path input resistance. When clk is high,

Capacitor C_B is charged to V_{DD}; when clk is low, the gate voltage of NMOS Switch is $V_{DD} + V_{in}$, and the gate/source voltage difference is always maintained as V_{DD}. Thus, the input resistance is input independent. Capacitor C_H is equivalent to the summation of the Cps and Cns in Fig. 1.

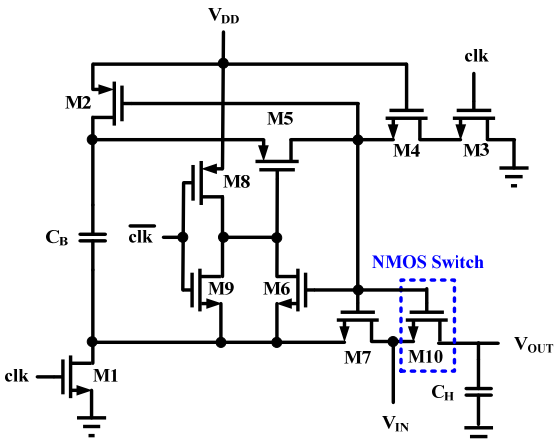

Fig. 5 Sample and hold circuit consisting of a bootstrapped switch and an equivalent sampling capacitor, C_H.

5. Measurement results

The 11-bit design was manufactured through a 0.35-µm CMOS process. The active area is 1.41 mm^2. Each unit capacitor is a poly-insulation-poly capacitor with a 15f F capacitance. Fig. 6 shows a photo of the chip. The inverter-based comparator occupies a space of only 1.05 μm^2.

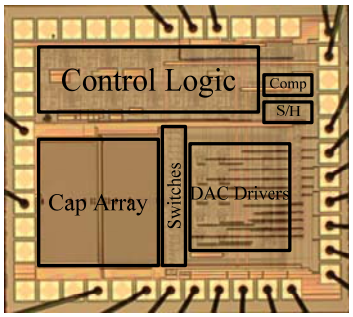

Fig. 6 Micrograph of the test chip.

When V_{DD} = 3.2 V, DNL = 0.88/–0.90 LSB and INL = 0.72/–1.14 LSB, as shown in Fig. 7. When the input and sampling frequencies are 5.45 kHz and 83.3 kHz, respectively, SNDR = 65.14 dB, SFDR = 80.59 dB, and ENOB = 10.61 bits. Fig. 8 displays a power spectrum from a sample that has an ENOB of 10.53. An ENOB of 10.61 is our best result from another sample.

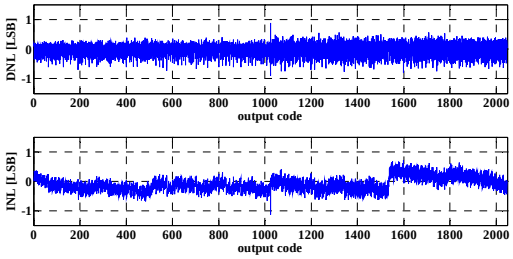

Fig. 7 DNL = 0.88/–0.90 LSB and INL = 0.72/–1.14 LSB, V_{DD} = 3.2 V.

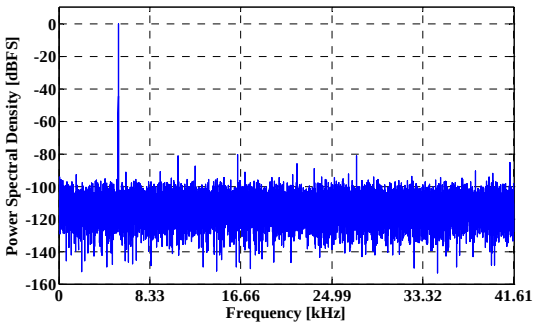

Fig. 8 Power spectrum with 65536-point FFT and an ENOB = 10.53 when V_{DD}=3.2V.

Fig. 9 shows the SNDR and SFDR when the sampling rate is 83.3 kS/s, and the input frequencies range from 5.45 to 165.83 kHz. When the input is close to the Nyquist rate, the SNDR decreases less than 0.5 bits. Therefore, the ERBW is higher than the Nyquist rate.

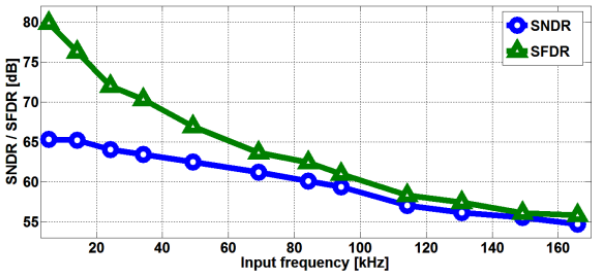

Fig. 9 SNDR/SFDR performance vs input frequencies when V_{DD} = 3.2 V.

When the ratio of input frequency to sampling frequency is 0.07, and for variable sampling frequencies, the measured SNDR and SFDR are shown in Fig. 10. When the sampling rate is close to 160 kHz, the ENOB remains higher than 10 bits.

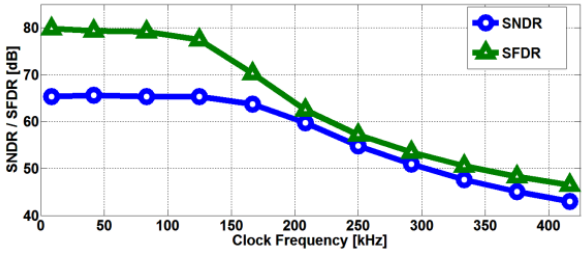

Fig. 10 SNDR/SFDR performance vs sampling frequencies when V_{DD} = 3.2 V.

When V_{DD} = 3.2 V, the ADC consumes 288.3 µW. The lowest FOM, 181 fJ/Conv-step, occurs when V_{DD} = 1.2 V, and the sampling frequency is then 25 kHz.

6. Conclusion

Table I compares the measured results with four different V_{DD}s and those in the literature. Those with superior results have a more advanced process. With the same 0.35-µm process, the measured result here is superior, with a similar V_{DD}. The proposed ADC reduces analog devices to only capacitor arrays by using an inverter-based comparator. The reduction is good for later design automation. With a low-power switching procedure, the proposed design achieves an FOM of 181 fJ/Conv.-step when V_{DD} = 1.2 V. The inverter threshold voltage variation impact is minimal because an SAR ADC has only one comparator, and the communication application is insensitive to the resulting ADC offset. Therefore, the proposed approach is effective.

Table I. Comparison of state-of-the-art works with a SAR structure

	[11]	[12]	[9]	[10]	[13]	This work			
Archi-tecture	Differential		Single-ended						
Tech-nology [µm]	0.18	0.18	0.18	0.18	0.35	0.35			
Supply voltage [V]	1.8	0.9	1.1	1.0	1	1.2	1.6	2.4	3.2
Sampl-ing rate [kS/s]	20 MS/s	1 MS/s	10	100	1	25	41.7	62.5	83.3
ENOB [bits]	9.89	8.38	7.4	9.48	10.2	10.3	10.4	10.4	10.6
Power [µW]	750	7.16	0.127	1.72	0.23	3.37	13.7	140	288
FOM [fJ/Conv.-step]	39.5	21.56	63.4	24.1	195	181	262	1680	2370

Acknowledgments

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