An Analysis of Output Ripples for PMOS Charge Pumps and Design Methodology

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***Abstract* — An analysis of output ripples for PMOS charge pumps is presented. Since the on-resistance of switching transistor plays an important role, the analytical model including this effect is derived and extensively verified by simulations using the 0.35 μm CMOS technology with errors within 7%. The measurement results also agree with the simulations. Based on the model, the guidelines to select the boosting capacitors, on-die output filtering capacitor and the optimized transistor sizes at the output stage are proposed. It would be helpful to design reduced-ripple PMOS charge pumps with good power efficiency and high boosted voltages.**

I. INTRODUCTION

The charge pump (CP) circuit acted as a simple on-die DC-DC voltage converter has been widely used in MEMS, flash memories, electrically erasable programmable read-only memory (EEPROM) to provide voltages higher than the supply voltage. A high-voltage regulator usually cascades several stages of charge pumps to generate the required voltage with high precision. To improve regulation quality, reduced-ripple output voltages of charge pump are preferred.

Most of the charge pumps are based on the Dickson structure using metal-oxide-semiconductor (MOS) field-effect transistors [1]. The PMOS based versions [2][3] using the low-cost twin-well CMOS technology without device reliability issues have been proposed to minimize degradation of boosted voltages due to threshold voltages and body effects. However, all the existing charge pump circuits require large filtering capacitor at the output to reduce ripples. Thus, the extra chip area is needed if the charge pump is embedded in the chip. In order to investigate the ripples at the output, the analytical model for the PMOS charge pumps is derived and verified using the 0.35μm CMOS process. Based on the model, the design methodology to lower ripples is also proposed.

II. THE PMOS CHARGE PUMP

The two-stage PMOS charge pump [3] without overstress is shown in Fig. 1 (a). The upper branch including M_1~M_3, M_7~M_9, C_1~C_2, and C_{a1}~C_{a2}, and the lower branch alternately transfer charges to the output. The transistor sizes are identical for these two branches. A two-phase clock scheme to increase the overdrive voltage of the transfer devices is presented in Fig. 1(b). According to Fig. 1 (b), two auxiliary clocks ϕ_{1a} and ϕ_{2a} are generated from the two out-of-phase clocks ϕ_1 and ϕ_2 by a pair of voltage doublers to help charge transfer through M_1, M_4, M_7 and M_{10}. When ϕ_1 is low and ϕ_2 is high, transistors N_1 and P_1 are turned on. At this moment ($t1$), ϕ_{1a} goes to 0V. Then, during time $t2$, ϕ_1 switches to V_{DD} and ϕ_2 goes to 0V, transistors N_1 and P_1 are turned off and transistor P_2 is turned on to make ϕ_{1a} become $2V_{DD}$. The operation of the auxiliary clock ϕ_{2a} is similar to that of clock ϕ_{1a}.

The authors would like to thank the Chip Implementation Center (CIC) of the National Applied Research Laboratories (NARL) of Taiwan for chip fabrication and the National Science Council of Taiwan for financially supporting this research under Contract no. NSC 98-2221-E-005-078.

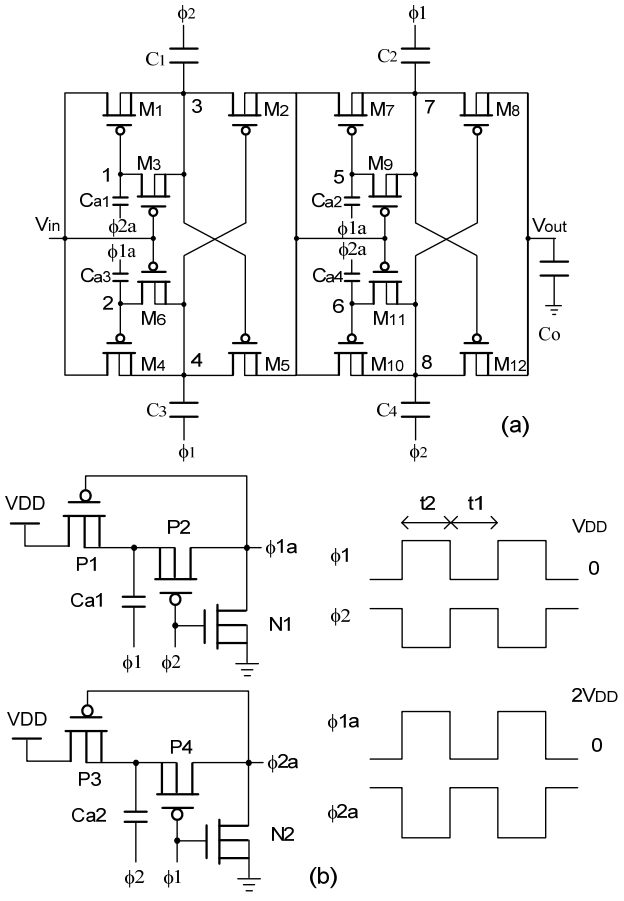

Figure 1. (a) The two-stage PMOS charge pump (b) The clock scheme

Conventionally, the on-resistance of the switching transistor is neglected in the charge pump circuit when the average boosted output voltage is analyzed. To improve the accuracy, our previous work [4] took the on-resistance into account for the other version of PMOS charge pumps to formulate the average boosted output voltage. Based on the formulation [4], the boosted output voltage of the 2-stage PMOS charge pump in Fig. 1 (a) can be modified as follows:

$$V_O \cong 2V_{DD} - 5\Delta V + V_t + \frac{2(V_{DD} + \Delta V - V_t)}{1 + \frac{\Delta V}{2V_{DD} + \Delta V - 2V_t}\exp\left(-\frac{T}{2R_1 C}\right)} - \Delta V \exp\left(-\frac{T}{R_{57}C}\right) - \frac{V_{DD} - \Delta V - V_t}{1 - \frac{\Delta V}{V_{DD} - V_t}\exp\left(-\frac{T}{R_8 C}\right)} \quad (1)$$

where $V_t = |V_{tp}|$; $\Delta V = I_O T/2C$; I_O is the output current and is assumed to be constant; R_1 and R_8 are the turn-on resistances of M_1 and M_8; R_{57} is the turn-on resistance of M_5 and M_7 in series; $C = C_1 = C_2 = C_3 = C_4$ denotes the boosting capacitor and T is the clock period. Note that the turn-on resistance can be approximated by $L/(\mu C_{ox} W V_{ov})$ and V_{ov} is the average of $|V_{gs}\text{-}V_{tp}|$.

III. Analysis of Output Ripples

To analyze the output ripple, we only consider the output stage which is composed of M_8, M_{12}, C_2 and C_4 in Fig. 1 (a). The simplified equivalent circuit for the output stage is depicted in Fig. 2, where R is the on-resistance of the switching transistor of M_8 or M_{12} (When one is on, the other is off.); C is the boosting capacitor; C_O is the output capacitor; V_2 is equivalent to the voltage at Node 7 or 8 in Fig. 1(a); V_{ro} is the ripple voltage at output node. As before, I_O is the constant output current. By applying KCL, the differential equations in time domain for the equivalent circuit in Fig. 2 can be expressed as

$$C\frac{dV_2}{dt} = -C_O\frac{dV_{ro}}{dt} - I_O \quad (2)$$

$$-C\frac{dV_2}{dt} = \frac{V_2 - V_{ro}}{R} \quad (3)$$

Substituting Eq. (2) into Eq. (3) and taking the derivative with respect to time give

$$RC_O\frac{d^2V_{ro}}{dt^2} = \frac{dV_2}{dt} - \frac{dV_{ro}}{dt} \quad (4)$$

The derivative of V_2 in Eq. (4) can be replaced using Eq. (2). Then, reordering the terms yields

$$\frac{d^2V_{ro}}{dt^2} + \left(\frac{1}{C} + \frac{1}{C_O}\right)\frac{dV_{ro}}{Rdt} = -\frac{I_O}{RCC_O} \quad (5)$$

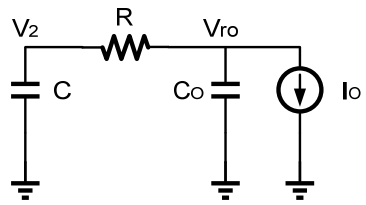

Figure 2. The simplified equivalent circuit at the output stage

Since the charge transfer through M_8 or M_{12} occurs in every time interval $T/2$, the charge stored in C transferring to C_O needs some time to go through the equivalent resistance R. Thus, V_{ro} increases from 0 to the maximum $V_{ro,max}$, *i.e.* the ripple, and then return to 0. The waveforms of V_{ro} and V_2 are illustrated in Fig. 3. Therefore, the boundary conditions for Eq. (5) are

$$V_{ro}(t = 0) = 0 \quad (6)$$

$$V_{ro}(t = T/2) = 0 \quad (7)$$

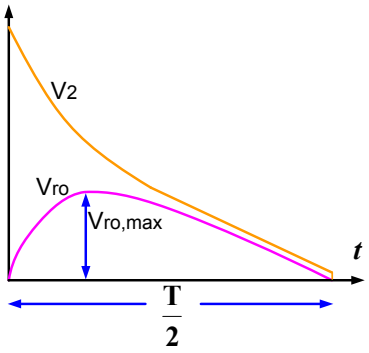

Figure 3. The waveforms of V_{ro} and V_2 in one half of the clock cycle

With these boundary conditions, the differential equation of V_{ro} can be derived as

$$V_{ro} = \frac{TI_O\left(\exp^{\frac{-t}{RC_P}} - 1\right)}{2(C + C_O)\left(\exp^{\frac{-T/2}{RC_P}} - 1\right)} - \frac{I_O t}{C + C_O} \quad (8)$$

where $C_P = C // C_O = (1/C + 1/C_O)^{-1}$ means C and C_O in parallel. When RC_P is much smaller than $T/2$, V_{ro} can be approximated as

$$V_{ro} = \frac{TI_O}{2(C + C_O)}\left(1 - \exp^{\frac{-t}{RC_P}}\right) - \frac{I_O t}{C + C_O} \quad (9)$$

If V_{ro} is assumed to reach its maximum value $V_{ro,max}$ at the time t_{max}, $V_{ro,max}$ can be obtained by solving $dV_{ro}(t = t_{max})/dt = 0$. The result yields t_{max}

$$t_{\max} = RC_P \ln\left(\frac{T/2}{RC_P(1 - \exp(-T/2RC_P))}\right) \quad (10)$$

By substituting t_{max} into Eq. (8), we can obtain the expression of the maximum output ripple.

$$V_{ro,\max} = \frac{TI_O}{2(C+C_O)} - \frac{RI_O CC_O}{(C+C_O)^2}\left(1+\ln\left(\frac{T/2}{RC_P}\right)\right) \quad (11)$$

The above expression indicates that the ripple of the output voltage can be decreased if T or I_O is small, or C_O is large. Alternatively, increasing R can help reduce ripples. That means W/L of M_8 and M_{12} can be reduced, but they must be chosen appropriately to avoid degradation of the boosted output voltage and the output current. In fact, I_O and T are usually determined by the specifications. C/T is selected to achieve the maximum power efficiency according to Ref. [4]. Therefore, R is the best parameter to adjust the ripples. Note that it is trivial that the large C_O can reduce ripples. If C_O is built on the die, it is preferred to make it as small as possible. The trade-off to select C_O is to make the second term of Eq. (11) as large as possible. That is to pick $C_O = C$, which is the most efficient approach to ripples.

IV. Comparison and Discussion

The 2-stage PMOS charge pump was fabricated using the 0.35 μm CMOS technology on the die area of 0.182 mm^2, as shown in Fig. 4. Figure 5 demonstrates the output ripple waveform by measuring the AC signals. Owing to the parasitic effects of the package and the measurement equipment, the effective output filtering capacitor was estimated to be C_O = 15 pF for the ripple around 22 mV.

To verify the accuracy of Eq. (11), comparison of output ripples between the model and simulated data of the two-stage PMOS charge pump was performed using the 0.35 μm CMOS process with the nominal conditions of W/L = 10, an output current I_O = 20 μA, a supply voltage of 1.8 V, and a clock period T = 100 ns.

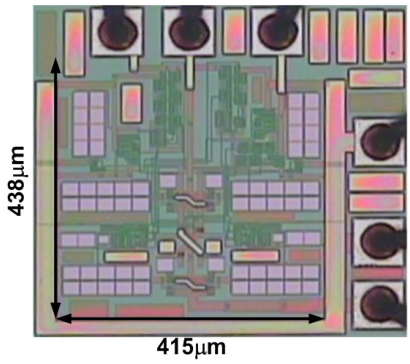

Figure 4. Microphotograph of the 2-stage PMOS charge pump

Figure 6 shows the agreement of the output voltages obtained from Eq. (1), simulated output voltages and measured output voltages for different output currents with C = 5 pF at a clock frequency of 10 MHz and V_{DD} = 1.8 V. Figures 7 to 10 compare the output ripples between the calculated data using Eq. (11) and the simulated or measured results. The output ripples versus the output currents are demonstrated in Fig. 7 for C_O = 5 pF and 15 pF at V_{DD} = 1.8 V. The on-resistance R is obtained by taking the inverse of the average of $|V_{gs}-V_{tp}|$ multiplied by $L/\mu C_{ox}W$. Here, R ≅ 2.7 kΩ for V_{DD} = 1.8 V. The simulated or measured ripples at the output are close to $V_{ro,max}$ calculated by the model. The errors of all the results are less than 7%.

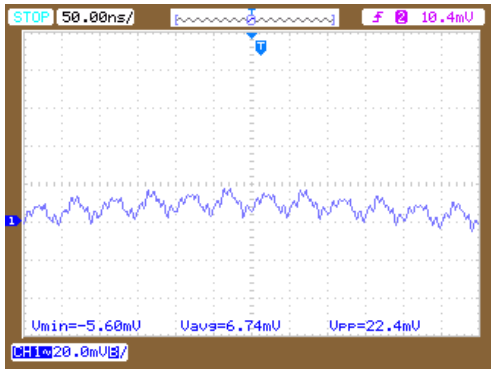

Figure 5. The measured output ripple waveform of the charge pump for C_O = 15 pF and I_O = 18 μA

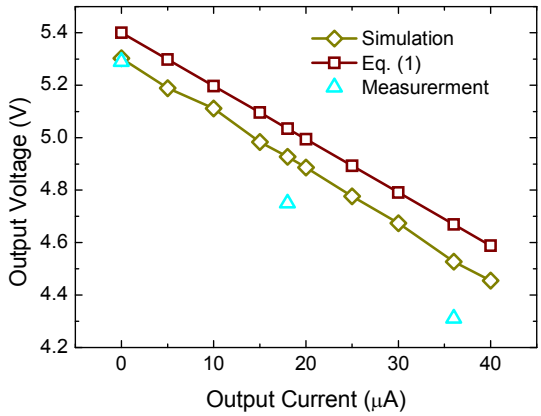

Figure 6. Comparison of the simulated and measured output voltages as functions of output current.

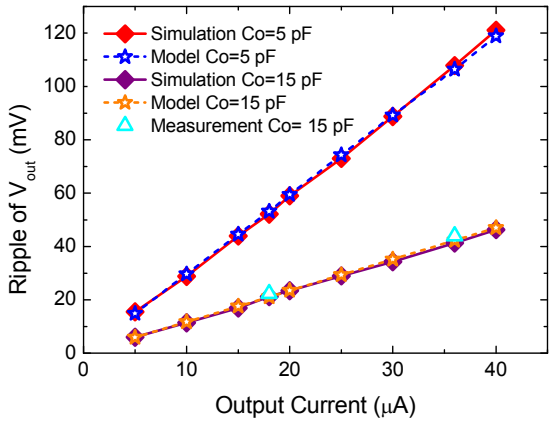

Figure 7. Output ripples are plotted as functions of output current at V_{DD} = 1.8 V.

Figure 8 shows the output ripples increase when W/L of M_8 or M_{12} is increased for I_O = 20 μA due to reduced on-resistance given in Eq. (11). In the mean time, the boosted output voltages are also increased to

the maximum value and then decreased slightly. The slight decrement may be owing to parasitic effects of large transistors, which were not considered in Eq. (1). The differences between simulated output ripples and maximum output ripples from the model are less than 6%. By inspection in the figure, the optimized *W*/*L* is between 10 and 15, since the boosted output voltage is close to the maximum and the ripple is smaller than those of larger *W*/*L* ratios.

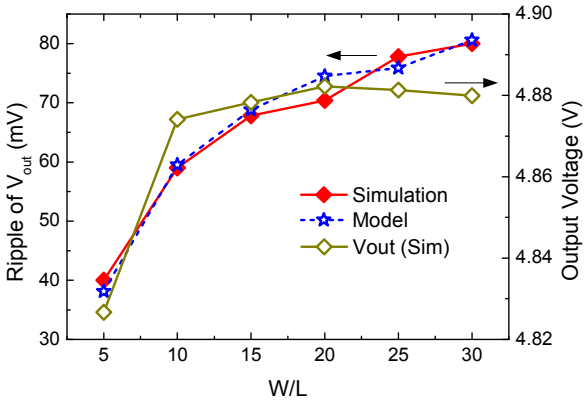

Figure 8. The output ripples and boosted output voltages are plotted as functions of *W*/*L* of M_8 or M_{12}, which is proportional to the inverse of on-resistance *R*.

The comparisons of output ripples between the model and simulations for different clock frequencies and output capacitors at V_{DD} = 1.8V, 2.5V and 3.3V are shown in Figs. 9 and 10, respectively. The discrepancies are all within 6%.

In summary, to design a good charge pump, the highest priority is high pumping gain with good power efficiency, and then reducing ripples as much as possible. The suggested design procedures are

(a). The optimized factor $\Delta V = I_O T/2C$ is calculated for a given supply voltage with the number of stages *N* [4] for power efficiency. Since the clock period *T* and output current I_O is given, the boosting capacitor *C* can be determined

(b). The smallest C_O to have relatively small ripples from Eq. (11) is to select $C_O = C$.

(c). From Eq. (1) and Eq. (11), the output voltage is increased until saturated as *W*/*L* is increased [4] but the ripple is decreased as *W*/*L* is reduced. Therefore, the optimized *W*/*L* is a trade-off factor as illustrated in Fig. 8.

I. Conclusions

Output ripples of the PMOS charge pump were investigated. The analytical model can be applied to most PMOS charge pump circuits. The accuracy of the model was verified by simulations with discrepancies less than 7% using the 0.35 µm CMOS technology. With the output voltage and the output ripple models, the optimized boosting capacitors, output filtering capacitor, transistor sizes of the output stage can be selected using the proposed design procedures.

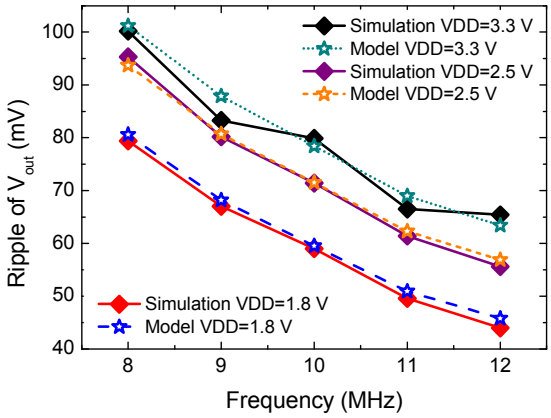

Figure 9. Comparison of output ripples versus clock frequencies between the model and simulated results at different supply voltages with $C = C_O = 5$ pF

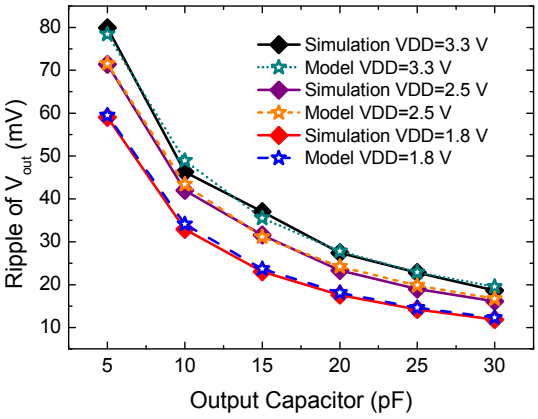

Figure 10. Comparison of output ripples vs. output filtering capacitor C_O between the model and simulated data at different supply voltages with $C = 5$ pF.

References

[1] J. Dickson, "On-chip high-voltage generation NMOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. SC-11, no. 3, pp. 374–378, Mar. 1976.

[2] E. Racape and J.-M.Daga, "A PMOS-switch based charge pump, allowing lost cost implementation on a CMOS standard process," in *Proc. IEEE Eur. Conf. Solid-State Circuits*, pp. 77–80, Sep. 2005.

[3] Chien-pin Hsu and Hongchin Lin, "Enhanced P-channel Metal-Oxide-Semiconductor Field-Effect Transistor Charge Pump for Low Voltage Applications," *Japanese Journal of Applied Physics*, vol.49, pp.04DE16-1~04DE16-6, April 2010.

[4] Chien-pin Hsu and Hongchin Lin, "Analytical Models of Output Voltages and Power Efficiencies for Multi-stage Charge Pumps," *IEEE Trans. Power Electronics*, vol.25, no.6, pp.1375-1385, June 2010.