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A Power-Efficient High-Voltage CMOS Gate Driver for Power MOS Transistors

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1. Introduction

The power MOS transistors are one of the key components in DC-DC converters [1,2] for power electronic applications. The on/off states of power transistors are controlled by DSP or ASIC chips. Thus, a gate driver is required to converter low voltage signals such as 3V to high voltage signals of 12V or above. Figure 1 illustrates the gate drivers marked by bold lines applied to the power MOS transistors in a push-pull DC-DC converter [1].

Several CMOS-based gate drivers have been proposed for different constraints of CMOS processes. For the standard CMOS processes, the voltage drop between any two electrodes of a transistor is limited to 5V or lower. Therefore, multiple transistors are cascaded if the output voltage is multiple times of 5V [3,4], which limits the driving ability and occupies large chip area. Usually, the high-voltage gate drivers were implemented using high-voltage SOI processes with complicated bootstrap capacitor technique [5] or zener diodes without considering short circuit power consumption [6]. Both capacitors and diodes occupy significant chip area. Here, we propose a MOS-transistor-only high-voltage gate driver without short circuit current for high power efficiency using the TSMC high-voltage (HV) bulk 0.25μm CMOS process.

2. Circuits of the Gate Driver

The proposed inverted-type gate driver is composed of a level shifter, PMOS and NMOS delay circuits and the output stage as illustrated in Fig. 2. The transistors with circles represent HV transistors. The $|V_{DS}|$ can be up to 60V but $|V_{GS}|$ must be less than 5V. The signal swings of input (Vin) and output (Vout) are VDDL and VDDH to ground, respectively. The outputs XH and XL are used to drive the PMOS and NMOS delay circuits, which are used to avoid short-circuit current occurred at the output stage during high/low transitions. Since the swing of PH is between VDDH and VDDHL+$|V_t|$, where V_t is the threshold voltage, $|V_{GS}|$ of Mop can be limited less than 5V. It is possible to connect XH and XL to PH and NL, respectively, without the delay circuits, but the power efficiencies are poor and will be demonstrated in Fig. 10.

Figures 3(a), (b) and (c) are the schematics of the level shifter, PMOS and NMOS delay circuits, respectively. The transistors without circles are normal 5V MOS transistors which occupy much less area than the HV MOS transistor does, so the 5V transistors are employed wherever they can to minimize chip area. Note that the bias voltages of VDDHL or VDDL at the gates of HV transistors limit the swings of their source electrodes less than 5V.

The timing diagram is illustrated in Fig. 4. If Vin is from 0 to VDDL, then XL and XH go to 0 and VDDHL+$|V_t|$. Then, PH becomes VDDH to turn off Transistor Mop. The next is ND lowered to 0, which forces NL to VDDL and then turns on Transistor Mon. Therefore, Mop and Mon will not be on simultaneously during signal transition. Similarly, for Vin from VDDL to 0, we can follow the timing diagram to check Mon is completely off before Mop starts to charge the output load. Thus, no short circuit power is consumed.

3. Implementation Results

The die microphotograph of the proposed gate driver is shown in Fig. 5. Because the output stage needs to drive the equivalent capacitance over 3600pF, the area is 0.308mm^2, while the rest only occupies 0.055mm^2.

Figures 6 and 7 are the measurement results for the switching frequency of 20kHz when the output (Vout2) was connected to the gate of IRFP460 power MOS transistor fabricated by International Rectifier (IR). The external resistors RL1 and RL2 shown in Fig. 2 are 33Ω and 22kΩ. Figure 6 shows the waveforms of the input and output with the amplitudes of 3V and 12V, respectively. The definitions of rise and fall times as well as rise and fall delays are also sketched. These delays and rise/fall times as well as power consumption for VDDH = 12V or 15V, VDDL = 3V or 5V are plotted in Fig. 7. As expected, the higher VDDH, the longer delays and rise/fall times. In fact, it still works for VDDH up to 50V, since $|V_{DS}|$ of HV MOS transistor is 60V.

Figures 8 to 10 are the measurement results for various ceramic capacitors as the load (CL). The rise/fall times are nearly proportional to load capacitance for (VDDH, VDDL) = (15V, 5V) and (12V, 3V) as shown in Fig. 8. Figure 9 verifies power consumption of the gate driver working up to 160kHz with CL of 600pF and 3600pF. Figure 10 compares power efficiencies, which are defined as power dissipated at the output divided by the total power provided by the power supplies, between measurement and simulations with and without delay circuits for (VDDH, VDDL) = (12V, 3V). For CL = 3600pF, the efficiency is increased from 70% to over 95% at the higher frequencies.

4. Conclusions

A power-efficient gate driver for power MOS transistors using 60V/0.25μm CMOS technology is proposed and was verified by measurement for frequencies up to 160kHz with power efficiency of 95%. The 3V~5V input signals can be converted to 12V~50V output signals. This gate driver can be integrated with DSP chips using the HV 0.25μm bulk CMOS process to reduce the sizes and cost of power electronic systems.

References

[1] E.-H. Kim and B.-H. Kwon, *IET Power Electron.*, **2**, (2009) 79.
[2] S. M. Mukhtar, A. R. M. Saad, N.H. Hanafi, *IEEE Intl. Conf. Power and Energy (PECon)*, 2010, p. 141.

[3] C. Huang and H. Lin, *Intl. Conf. Solid State Devices and Materials* (*SSDM*), 2011, p. 170.
[4] C. Huang and H. Lin, *Jpn. J. Appl. Phys.*, **51**, (2012) 02BE08.

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[5] M. A. Huque, L. M. Tolbert, B. J. Blalock, S. K. Islam, *IET Power Electron.*, **3**, (2010)1001.
[6] B. D. Choi, *IEEE Trans. Consumer Electron.*, **55**, (2009) 992.

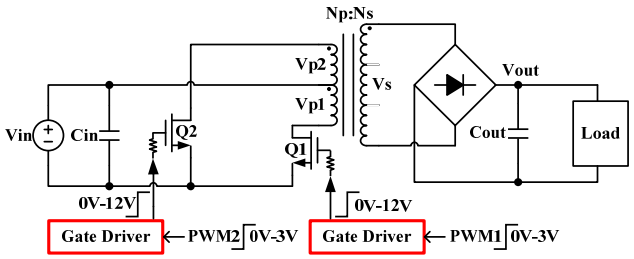

Fig. 1 Application of gate drivers in a push-pull DC-DC converter

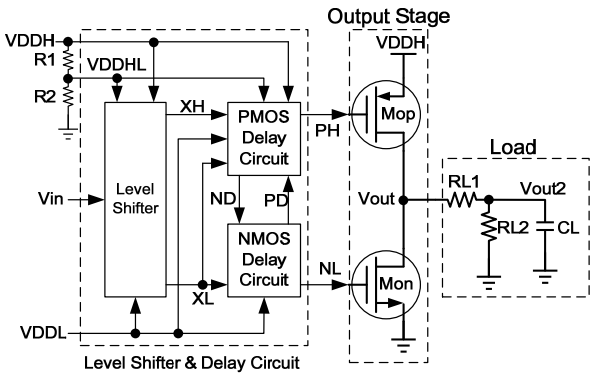

Fig. 2 The circuit blocks of the proposed gate driver

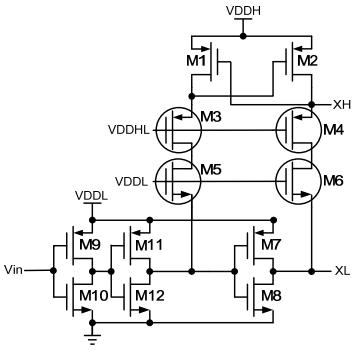

Fig. 3(a) Level shifter circuit

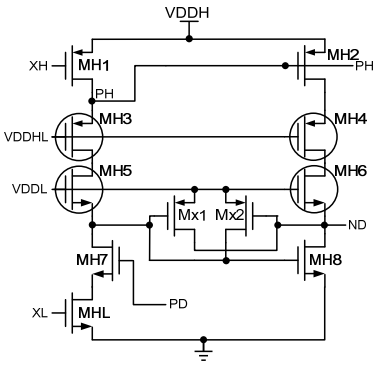

Fig. 3(b) PMOS delay circuit

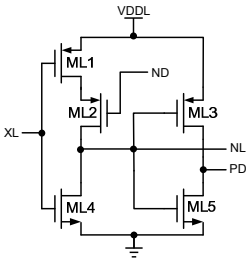

Fig. 3(c) NMOS delay circuit

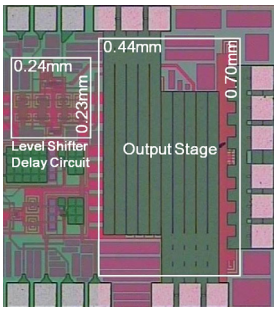

Fig. 5 The chip microphotograph

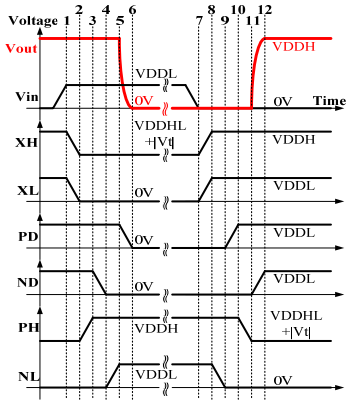

Fig. 4 Timing diagram

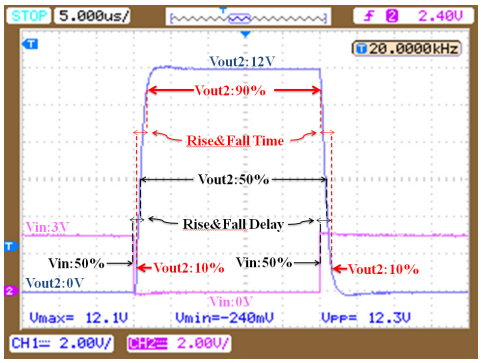

Fig. 6 Measured waveforms with the definitions of delay and rise/fall times

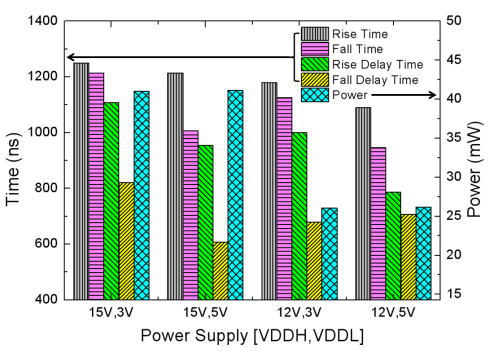

Fig. 7 Delay, rise/fall times and power consumption for IRFP 460 as the load

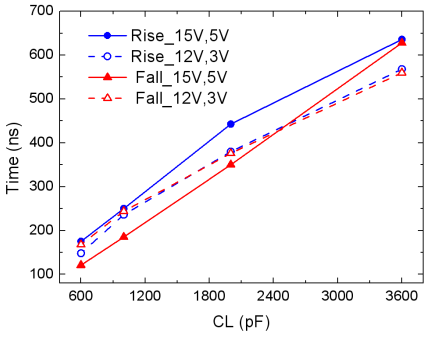

Fig. 8 Rise/fall times for various ceramic capacitors as the load

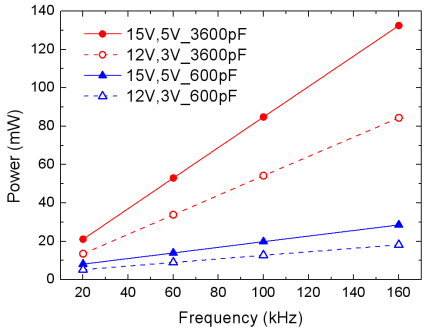

Fig. 9 Power vs. switching frequencies for various loads and voltages

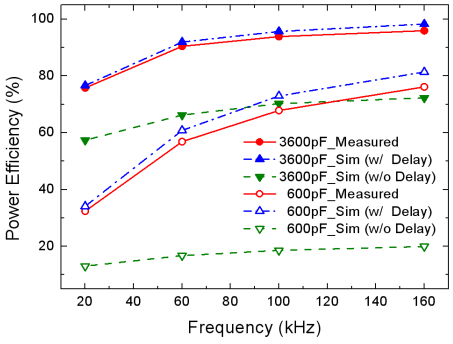

Fig. 10 Power efficiencies are compared between measurement and simulation.