An Analytical Model of Output Ripples for PMOS Charge Pumps

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***Abstract* — An analytical model of output ripples for PMOS charge pumps is derived. Since the on-resistance of switching transistor is considered, the accuracy is improved significantly. The model is extensively verified by simulations using the 0.35 μm CMOS technology with relative errors within 7%. The measurement results also agree with the simulations. Based on the model, the on-die output filtering capacitor and the optimized transistor sizes of the output stage of charge pump can be selected for ripple reduction without degrading the boosted output voltage.**

I. INTRODUCTION

The charge pump (CP) circuit acted as a simple on-die DC-DC voltage converter has been widely used in MEMS, flash memories, electrically erasable programmable read-only memory (EEPROM) to provide voltages higher than the supply voltage. A high-voltage regulator usually cascades several stages of charge pumps to generate the required voltage with high precision. To improve regulation quality, reduced-ripple output voltages of charge pump are preferred.

Most of the charge pumps are based on the Dickson structure using metal-oxide-semiconductor (MOS) field-effect transistors [1]. The PMOS based versions [2][3] without device reliability issues can effectively reduce the degradation due to threshold voltage and body effect, and can be implemented using the low-cost twin-well CMOS technology. However, all the existing charge pump circuits require large filtering capacitor at the output to reduce ripples. Thus, the extra chip area is needed if the charge pump is embedded in the chip. In order to investigate the ripples at the output, the analytical model for the PMOS charge pumps is derived and verified using the 0.35μm CMOS process. Based on the model, the design methodology to lower ripples is also proposed.

II. THE PMOS CHARGE PUMPS

The two-stage PMOS charge pump [3] without overstress is shown in Fig. 1 (a). The upper branch including M_1~M_3, M_7~M_9, C_1~C_2, and C_{a1}~C_{a2}, and the lower branch alternately transfer charges to the output. The transistor sizes are identical for these two branches.

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A two-phase clock scheme to increase the overdrive voltage of the transfer devices is presented in Fig. 1(b). According to Fig. 1 (b), two auxiliary clocks ϕ_{1a} and ϕ_{2a} are generated from the two out-of-phase clocks ϕ_1 and ϕ_2 by a pair of voltage doublers to help charge transfer through M_1, M_4, M_7 and M_{10}. When ϕ_1 is low and ϕ_2 is high, transistors N_1 and P_1 are turned on. At this moment ($t1$), ϕ_{1a} goes to 0V. Then, during time $t2$, ϕ_1 switches to V_{DD} and ϕ_2 goes to 0V, transistors N_1 and P_1 are turned off and transistor P_2 is turned on to make ϕ_{1a} become $2V_{DD}$. The operation of the auxiliary clock ϕ_{2a} is similar to that of clock ϕ_{1a}.

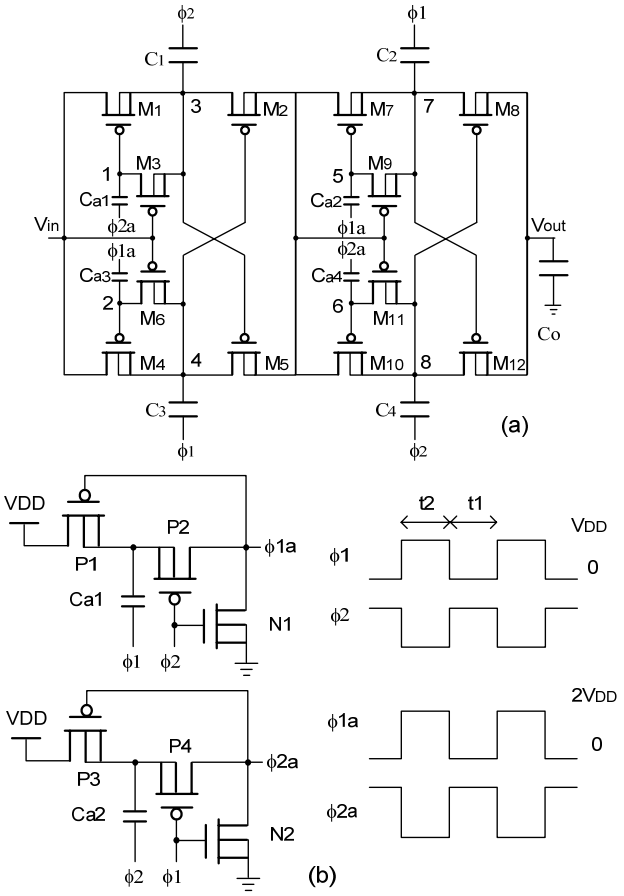

Figure 1. (a) The two-stage PMOS charge pump (b) The clock scheme

Conventionally, the on-resistance of the switching transistor is neglected in the CP circuit when the

average boosted output voltage is analyzed. To improve the accuracy, our previous work [4] took the on-resistance into account for the other version of PMOS CPs to formulate the average boosted output voltage. Based on the formulation [4], the boosted output voltage of the 2-stage PMOS CP in Fig. 1 (a) can be modified as follows:

$$V_O \cong 2V_{DD} - 5\Delta V + V_t + \frac{2(V_{DD} + \Delta V - V_t)}{1 + \frac{\Delta V}{2V_{DD} + \Delta V - 2V_t}\exp\left(-\frac{T}{2R_1C}\right)} - \Delta V \exp\left(-\frac{T}{R_{57}C}\right) - \frac{V_{DD} - \Delta V - V_t}{1 - \frac{\Delta V}{V_{DD} - V_t}\exp\left(-\frac{T}{R_8C}\right)} \quad (1)$$

where $V_t = |V_{tp}|$; $\Delta V = I_O T/2C$; I_O is the output current and is assumed to be constant; R_1 and R_8 are the turn-on resistances of M_1 and M_8; R_{57} is the turn-on resistance of M_5 and M_7 in series; $C = C_1 = C_2 = C_3 = C_4$ denotes the boosting capacitor and T is the clock period. Note that the turn-on resistance can be approximated by $L/(\mu C_{ox} W V_{ov})$ and V_{ov} is the average of $|V_{gs}\text{-}V_{tp}|$.

III. Analytical Model of Output Ripple

To analyze the output ripple, we only consider the output stage which is composed of M_8, M_{12}, C_2 and C_4 in Fig. 1 (a). The simple equivalent circuit for the output stage is depicted in Fig. 2, where R is the on-resistance of the switching transistor of M_8 or M_{12} (When one is on, the other is off.); C is the boosting capacitor; C_O is the output capacitor; V_{ro} is the ripple voltage at output node. As before, I_O is the constant output current. By applying KCL, the differential equations in time domain for the equivalent circuit in Fig. 2 can be expressed as

$$\frac{dV_2}{dt} = -\frac{C_O dV_{ro}}{Cdt} - \frac{I_O}{C} \quad (2)$$

$$-\frac{RCdV_2}{dt} = V_2 - V_{ro} \quad (3)$$

By substituting Eq. (2) into Eq. (3) and taking the derivative with respect to time, the following equation is obtained.

$$\frac{RC_O d^2V_{ro}}{dt^2} = \frac{dV_2}{dt} - \frac{dV_{ro}}{dt} \quad (4)$$

The derivative of V_2 in Eq. (4) can be replaced using Eq. (2). Then, reordering the terms yields

$$\frac{d^2V_{ro}}{dt^2} + \left(\frac{1}{C} + \frac{1}{C_O}\right)\frac{dV_{ro}}{Rdt} = -\frac{I_O}{RCC_O} \quad (5)$$

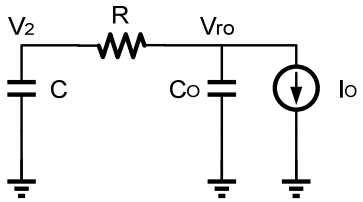

Figure 2. The equivalent circuit of the output stage

Since the charge transfer through M_8 or M_{12} occurs in every time interval $T/2$, the charge stored in C transferring to C_O needs some time to go through the equivalent resistance R. Thus, V_{ro} increases from 0 to the maximum $V_{ro,max}$, and then return to 0. The waveforms of V_{ro} and V_2 are illustrated in Fig. 3. The boundary conditions for Eq. (5) are given as

$$V_{ro}(t = 0) = 0 \quad (6)$$

$$V_{ro}(t = T/2) = 0 \quad (7)$$

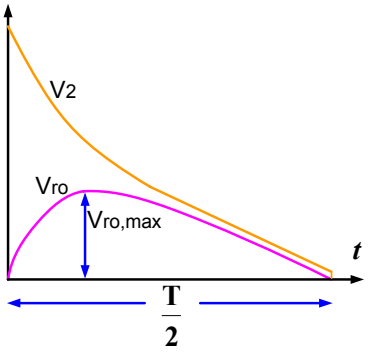

Figure 3. The waveforms of V_{ro} and V_2

With these boundary conditions, the differential equation of V_{ro} can be derived as

$$V_{ro} = \frac{TI_O\left(\exp\left(\frac{-t}{R(C//C_O)}\right) - 1\right)}{2(C + C_O)\left(\exp\left(\frac{-T/2}{R(C//C_O)}\right) - 1\right)} - \frac{I_O}{C + C_O}t \quad (8)$$

where $C//C_O = (1/C + 1/C_O)^{-1}$. When $R(C//C_O)$ is much smaller than $T/2$, V_{ro} can be simplified to

$$V_{ro} = \frac{TI_O}{2(C + C_O)}\left(1 - \exp\left(\frac{-t}{R(C//C_O)}\right)\right) - \frac{I_O}{C + C_O}t \quad (9)$$

If V_{ro} is assumed to reach its maximum value $V_{ro,max}$ at the time t_{max}, it can be obtained by solving $dV_{ro}(t = t_{max})/dt = 0$. The result is

$$t_{\max} = R(C//C_O)\ln\left(\frac{T/2}{R(C//C_O)\{1 - \exp[-T/2R(C//C_O)]\}}\right) \quad (10)$$

Substituting Eq. (10) into Eq. (8) yields the maximum output ripple equal to

$$V_{ro,\max} = \frac{TI_O}{2(C+C_O)} - \frac{RI_O CC_O}{(C+C_O)^2}\left\{1+\ln\left[\frac{T/2}{R(C//C_O)}\right]\right\} \quad (11)$$

The above expression indicates that the ripple of the output voltage can be decreased if T or I_O is small, or C_O is large. Alternatively, increasing R can help reduce ripples. That means W/L of M_8 and M_{12} can be reduced, but they must be chosen appropriately to avoid degradation of the boosted output voltage and the output current. Furthermore, from the second term of Eq. (11), if C_O is usually built in the die for given T, I_O, R and C in the CP, the smallest C_O with the most efficient ripple reduction is to select $C_O = C$. Nevertheless, it is trivial that the large C_O can reduce ripples.

IV. Comparison and Discussion

The 2-stage PMOS CP was fabricated using the 0.35μm CMOS technology on the die area of 0.182 mm^2, as shown in Fig. 4. Figure 5 demonstrates the output ripple waveform by measuring the AC signals. Owing to the parasitic effects of the package and the measurement equipment, the effective output filtering capacitor was estimated to be C_O = 15 pF for the ripple around 22mV.

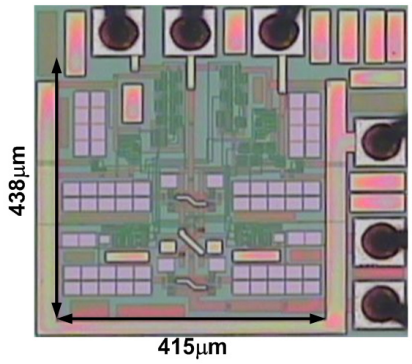

Figure 4. Microphotograph of the 2-stage PMOS charge pump

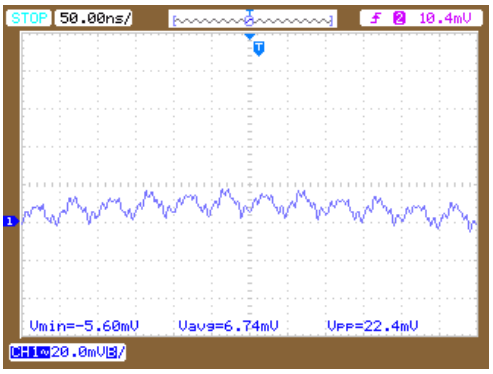

Figure 5. Measured output ripple waveform of the charge pump for C_O = 15 pF and I_O = 18 μA

To verify the accuracy of the analytical model, extensive comparison of output ripples between the model and simulated data of the two-stage PMOS CP was performed using the 0.35μm CMOS process with the nominal conditions of W/L = 10, an output current I_O = 20 μA, a supply voltage of 1.8 V, and a clock period T = 100 ns.

Figure 6 shows the simulated and measured output voltages for different output currents with C = 5 pF at a clock frequency of 10MHz and V_{DD} = 1.8V. Figures 7 to 10 compare the output ripples between the calculated data using Eq. (11) and simulated or measured results. The output ripples versus the output current are demonstrated in Fig. 7 for V_{DD} = 1.8V and C_O = 5pF or 15pF. The on-resistance R was obtained by taking the inverse of the average of $|V_{gs}-V_{tp}|$ multiplied by $L/\mu C_{ox}W$. Here, $R \cong 2.7$ kΩ for V_{DD} = 1.8V. The simulated or measured ripples at the output are close to $V_{ro,max}$ calculated by the model. All the relative errors are less than 7%.

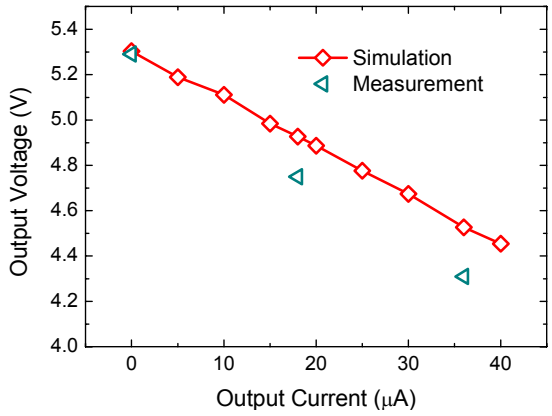

Figure 6. The comparison of the simulated and measured output voltages as functions of output current.

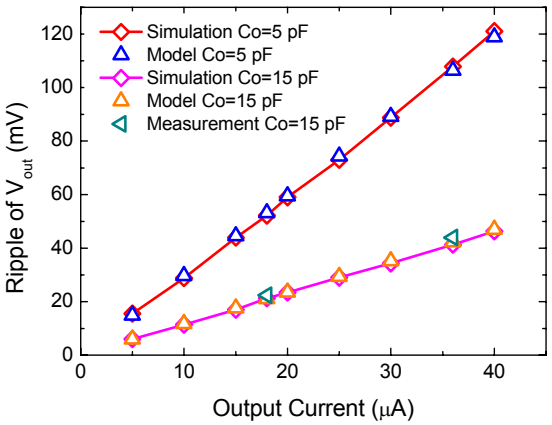

Figure 7. The output ripples and boosted output voltages are plotted as functions of output current at V_{DD} = 1.8 V.

Figure 8 shows the output ripples are increased when W/L of M_8 or M_{12} is increased for I_O = 20 μA, which can be explained by Eq. (11). In the mean time, the boosted output voltages are also increased to the maximum value and then decreased slightly. The slight decrement may be owing to parasitic effects of large transistors, which were not considered in Eq. (1). The differences between simulated output ripples and maximum output ripples from the model are less than

6%. By inspection in the figure, the optimized *W*/*L* is between 10 and 15, since the boosted output voltage is close to the maximum and the ripple is smaller than those of larger *W*/*L* ratios.

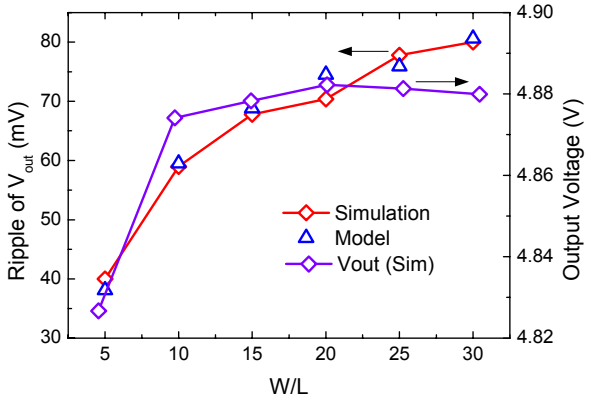

Figure 8. The output ripples and boosted output voltages are plotted as functions of *W*/*L* of M_8 or M_{12}, which is equivalent to the inverse of on-resistance *R*.

The comparisons of output ripples between the analytical model and simulations for different output capacitors and clock frequencies are demonstrated in Figs. 9 and 10, respectively. The discrepancies are always within 4%.

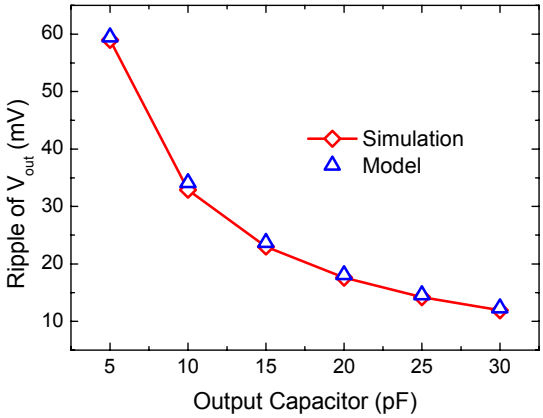

Figure 9. The comparison of output ripples vs. output filtering capacitor C_O between the model and simulated data with $C = 5$ pF.

In summary, to design a good charge pump, the highest priority is high pumping gain with good power efficiency, and then reducing ripples as much as possible. The suggested design procedures are

(a). The optimized factor $\Delta V = I_O T/2C$ is calculated for a given supply voltage with the number of stage $N = 2$ [4] for power efficiency. Since the clock period T and output current I_O is given, the boosting capacitor C can be determined

(b). The smallest C_O to have relatively small ripples from Eq. (11) is to select $C_O = C$.

(c). From Eq. (1) and Eq. (11), the output voltage is increased until saturated as *W*/*L* is increased [4] but the ripple is decreased as *W*/*L* is reduced. Therefore, the optimized *W*/*L* is a trade-off factor as illustrated in Fig. 8.

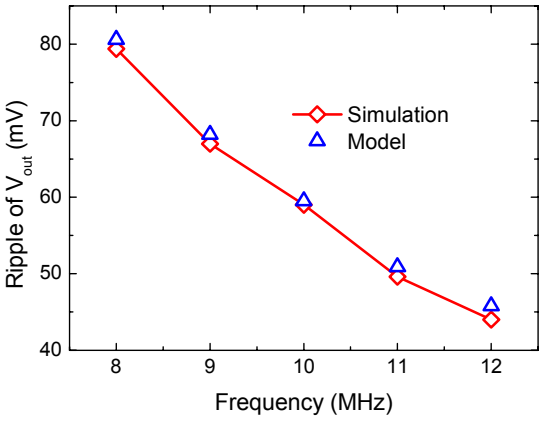

Figure 10. The comparison of output ripples between the model and simulated results for various clock frequencies with $C = C_O = 5$ pF

V. Conclusions

An analytical output ripple model for the PMOS CP was formulated and can be applied to most PMOS charge pump circuits. The accuracy of the model was verified by simulations with the relative errors less than 7% using the 0.35 μm CMOS technology. The measurement also agrees with the simulation results. With the output voltage and the ripple models, the optimized boosting capacitors, output capacitor, transistor sizes of the output stage can be selected. That helps speed up the design of PMOS charge pump circuits.

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