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Reduced-Ripple p-Channel Metal–Oxide–Semiconductor Field-Effect Transistor Charge Pump Circuit with Small Filtering Capacitance

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This paper presents a two-stage, two-phase, p-channel metal–oxide–semiconductor field-effect transistor (PMOSFET) charge pump with special two-step clocks for ripple reduction. The ripple voltage can be reduced by adjusting the overdrive voltage during charge transfer. The charge pump including the circuit of the proposed clocks and 5 pF boosting capacitance was fabricated using 0.35 μm complementary metal–oxide–semiconductor field-effect transistor (CMOSFET) technology in an area of 0.182 mm^2. With the new clock scheme, high voltage gain and driving capacity without overstress of the transistors are preserved. The experimental results reveal that the output voltage ripple is reduced from 23.2 to 12.8 mV for an output current of 36 μA at a frequency of 10 MHz and a supply voltage of 1.8 V, which indicates a 45% ripple reduction without increasing filtering capacitance.

1. Introduction

The charge pump (CP) circuit has been widely used in micro electro-mechanical systems (MEMS), flash memories, electrically erasable programmable read-only memory (EEPROM), and so on. It is usually used as a simple on-die DC–DC voltage converter to provide voltages higher than the supply voltage. A high-voltage regulator usually cascades several stages of CP units to provide the required voltage with high precision. To improve regulation quality, CPs with reduced-ripple output voltages are preferred.

Most CPs are based on the Dickson structure using metal–oxide–semiconductor (MOS) field-effect transistors.[1)] p-Channel MOS (PMOS) based versions[2–4)] can effectively reduce the degradation due to the threshold voltage and body effect, and can be implemented using low-cost twin-well complementary metal–oxide–semiconductor (CMOS) technology. In addition, a simple CP[3,4)] enhances the performance without device reliability issues. However, all the existing CP circuits require large filtering capacitance at the output to reduce ripples; thus, extra chip area is required if the CP is embedded in the chip. A parallel CP,[5)] which has low reliability, splits the CP into N parallel modules to reduce ripples. However, it requires a complex delay clock circuit and high N (= 8) values to reduce reverse charging leakage.

In this study, special two-step clock patterns for the last stage were designed for a two-phase PMOS CP.[3,4)] The obtained results show that the ripple of the output voltage is significantly reduced without degrading the pumping ability. Simulations and measurements based on 0.35 μm CMOS technologies were performed to demonstrate the performance of the pump.

This paper is organized as follows. The clock scheme of the proposed CP is illustrated in §2. Section 3 presents the circuits used to generate the special two-step clocks. In §4, the analysis of output voltage and ripple is described. In §5, the simulation and measurement of the proposed CP are demonstrated. Conclusions are given in §6.

2. Clock Scheme for Ripple Reduction

The two-stage PMOS CP circuit with two out-of-phase clocks, ϕ_1 and ϕ_{1b}, with amplitudes varying from 0 to V_{DD} is shown in Fig. 1. The circuit has top and bottom branches, which alternatively transfer charges to the filtering capacitor (C_O) at the output. The first stage of the PMOS CP consists of six transistors, a pair of boosting capacitors, C_1 and C_3, and a pair of auxiliary capacitors, C_{a1} and C_{a2}. Two auxiliary clocks, ϕ_{1a} and ϕ_{2a}, are generated using ϕ_1 and ϕ_{1b} to double the amplitudes of the clocks. The second stage is identical to the first stage, except that the two special two-step clocks N_{ck1} and N_{ck2} are used to replace ϕ_1 and ϕ_{1b} in our previous work.[3,4)] The reason for this is that when the transistor M_8 or M_{12} is fully turned on, charges may instantaneously transfer to C_O. If all parasitic capacitances and turn-on resistances of the transistors are ignored, the ideal maximum value of ripples can be approximated as

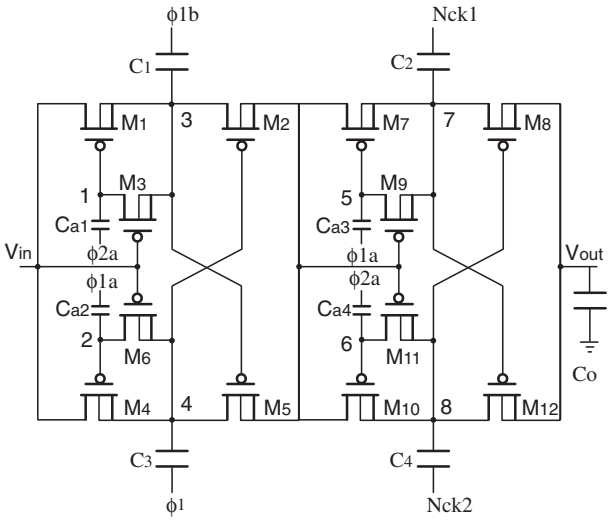

Fig. 1. Two-stage PMOS CP using N_{ck1} and N_{ck2} in the second stage.

$$V_R \cong \frac{T}{2(C + C_O)} I_O, \tag{1}$$

where T is the period, I_O is the output current, and C is the boosting capacitance.

Without increasing C_O, if the turn-on resistance r_{on} of the PMOS transistors is not neglected and is increased instead, the ripple can be reduced, but the charge in C may not be transferred to C_O completely, which could affect the pumping ability and has to be controlled carefully. Notably,

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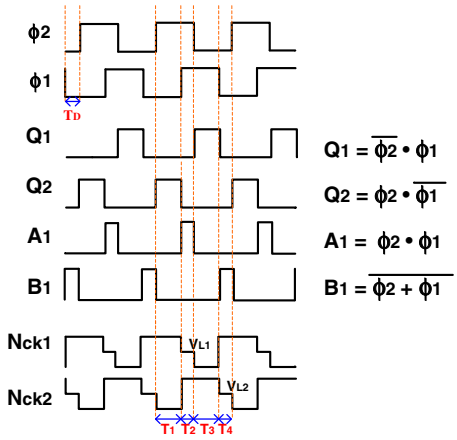

Fig. 2. (Color online) Waveforms used to generate N_{ck1} and N_{ck2} based on ϕ_1 and ϕ_2.

the turn-on resistance of a transistor in the triode region is expressed as $r_{on} \cong L/\mu C_{ox} W V_{ov}$, where $V_{ov} = |V_{GS}| - |V_t|$. Therefore, the waveforms of the proposed N_{ck1} and N_{ck2} shown in Fig. 2 are used to adjust V_{ov} during charge transfer so that the ripple can be reduced effectively without degradating the voltage gain and driving capacity. These two clocks stay at voltages V_{L1} and V_{L2} for a while before returning to zero. Therefore, r_{on} in the beginning of charge transfer is higher than that in the rest of the turn-on period.

3. Clock Generation Circuit

The waveforms of N_{ck1} and N_{ck2} in Fig. 2 can be generated using the circuits in Fig. 3. Each circuit comprises four transistors and a pair of capacitors, C_{s1} and C_{s2} (or C_{s3} and C_{s4}). The control signals ϕ_1, ϕ_2, Q_1, Q_2, A_1, and B_1 are illustrated in Fig. 2. The overlapping time T_D between ϕ_1 and ϕ_2 is equal to T_2 and T_4. According to Fig. 2, Q_1, Q_2, A_1, and B_1 can be obtained using simple logic gates with ϕ_1 and ϕ_2 as the inputs.

In the time interval T_1, ϕ_1, Q_1, and A_1 are low, and Q_2 is high. M_{k3} and M_{k1} are turned on to transfer charges from V_{DD} to C_{s2} and discharge C_{s1}, respectively, while M_{k2} and M_{k4} are turned off; thus, N_{ck1} becomes V_{DD}. In the time interval T_2, ϕ_1 and A_1 are high, while Q_1 and Q_2 are low; thus, M_{k1}, M_{k2}, and M_{k3} are turned off, and M_{k4} is turned on to transfer charges from C_{s2} to C_{s1}. By adjusting the ratio between C_{s1} and C_{s2}, the voltages V_{L1} and V_{L2} can be determined. In the time interval T_3, A_1 is 0 and Q_1 becomes V_{DD}; therefore, N_{ck1} drops to 0. In the time interval T_4, since ϕ_1 and Q_1 are reduced to 0, N_{ck1} becomes V_{DD}. N_{ck2} can be generated via the other circuit in Fig. 3. The operation of N_{ck2} is similar to that of N_{ck1} but with a 180° phase difference.

4. Analysis of Output Voltage and Ripples

Conventionally, the on-resistance of the switching transistor is neglected for simplicity. Thus, the output voltage of the proposed two-stage PMOS CP can be expressed as

$$V_O = V_{DD} + \left(\frac{2}{1+\beta}\right)V_{DD} - I_O R_O, \tag{2}$$

where I_O is the output current, R_O is the output resistance, β is the ratio of the top-plate parasitic capacitance to the

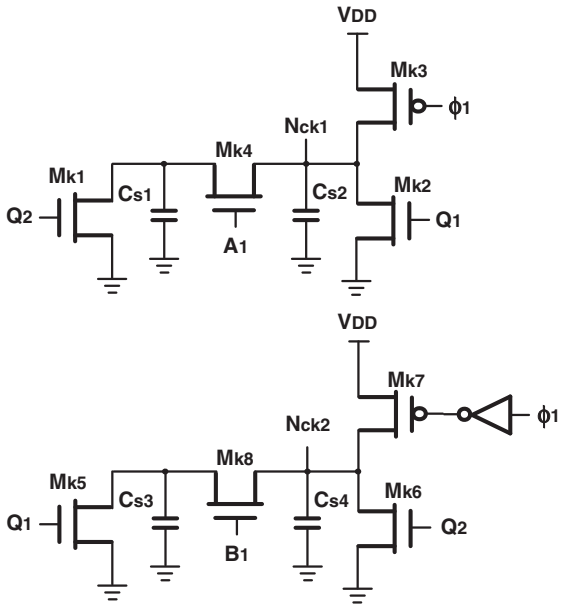

Fig. 3. Clock generation circuits used to produce N_{ck1} and N_{ck2}.

pumping capacitance, and $R_O = N/2fC$, where C denotes the boosting capacitance and f is the clock frequency. When the resistance of the switching transistor is taken into account, R_O can be approximated as[6]

$$R_O = \frac{N}{2fC}\coth\left(\frac{T/2}{r_{on}C}\right). \tag{3}$$

This means that the output voltage decreases when r_{on} increases from 0. To prevent the degradation of output voltage, the two-step N_{ck1} and N_{ck2} clocks return to 0 V in the time intervals T_3 and T_1, respectively, to make r_{on} as small as possible.

The ideal ripple expression given in eq. (1) is valid when the turn-on resistance (r_{on}) of M_8 and M_{12} in Fig. 1 is neglected. By taking r_{on} into account, the output ripple voltage V_R can be approximated as

$$V_R \cong \frac{TI_O}{2(C+C_O)} - \frac{r_{on}I_O C}{C+C_O}, \tag{4}$$

where r_{on} is the turn-on resistance of M_8 and M_{12}. The second term is the voltage drop due to the turn-on resistance r_{on}. Since the transfer of the charge stored in C to C_O requires time to go through r_{on}, the ripple V_R is reduced, as shown in Fig. 4, where ΔV is the first term in eq. (4). For the proposed two-step clocks, the overdrive voltages of M_8 and M_{12} are reduced when N_{ck1} and N_{ck2} remain at V_{L1} and V_{L2}, respectively. Thus, the turn-on resistance r_{on} increases, and the ripple voltage is reduced. It is apparent that the ripple of the output voltage can be decreased if C_O increases. By applying this approach, ripple reduction can be achieved with small filtering capacitance.

5. Simulation and Measurement Results

The proposed reduced-ripple PMOS CP was designed and fabricated using the twin-well 0.35 μm CMOS process with boosting and auxiliary capacitances of 5 and 0.5 pF, respectively. The CPs with and without[3,4] the special two-step clocks were simulated using the same capacitances,

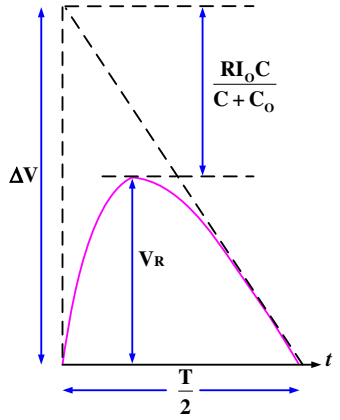

Fig. 4. (Color online) Illustration of waveform of output ripple.

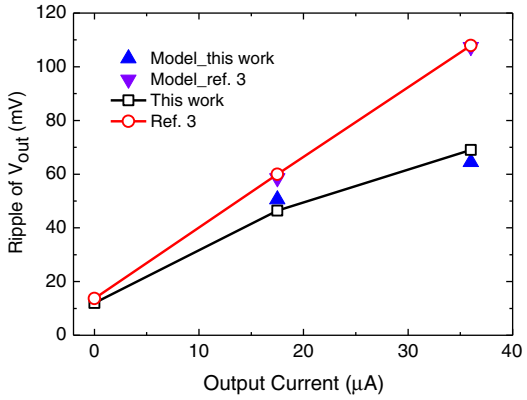

Fig. 6. (Color online) Comparison of output ripples between model and simulation of the two-stage CPs for different output currents with $V_{DD} = 1.8\,V$.

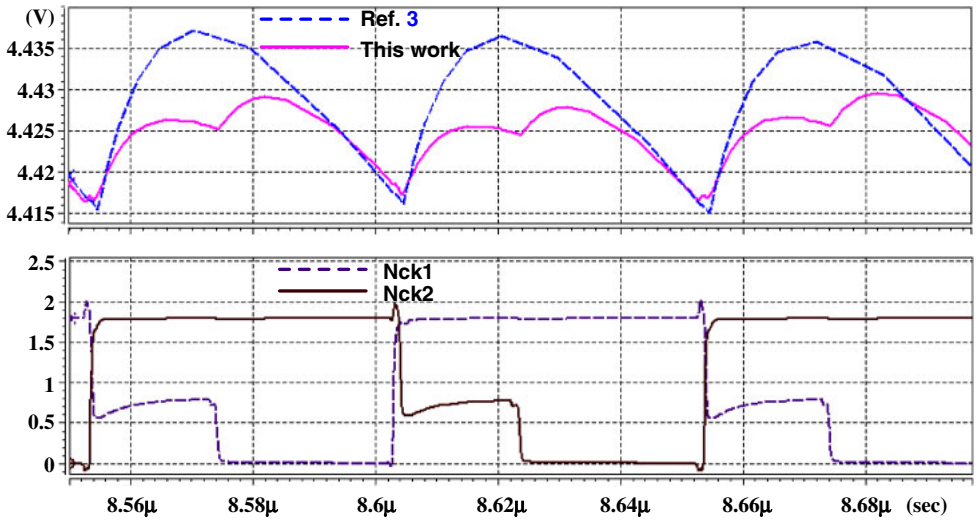

Fig. 5. (Color online) Comparison of simulated output ripple waveforms of the two-stage CPs with $I_{out} = 36\,\mu A$ at 10 MHz and $V_{DD} = 1.8\,V$.

transistor sizes, and clock frequency. Figure 5 shows the waveforms of N_{ck1} and N_{ck2}, as well as the simulated output waveforms for the existing CP[3,4] and the proposed CP with the filtering capacitance (C_O) of 30 pF and $I_{out} = 36\,\mu A$ at a frequency of 10 MHz and $V_{DD} = 1.8\,V$. The overlapping time T_D, which is denoted by T_2 and T_4 in Fig. 2, between ϕ_1 and ϕ_2 is 20 ns. We can observe that the average output voltage is about the same for the two CPs, while the proposed CP has smoother rising edges than the existing CP. Simulation results show that the ripples are reduced by about 40% with two humps in one half-cycle of a period due to the two-step clocks.

Figure 6 shows the output ripples of the prior CP[3,4] and the proposed CP with $T_D = 20\,ns$ for different output currents at a frequency of 10 MHz, with small filtering capacitance of $C_O = 5\,pF$, and $V_{DD} = 1.8\,V$. Solid lines indicate the simulated results, and solid symbols indicate the data calculated using eq. (4). In addition to the agreement between the model and simulated data, owing to different V_{gs} values for the two curves, a maximum ripple reduction of up to 45% can be observed. For a high output current, the improvement of ripple reduction is even more pronounced.

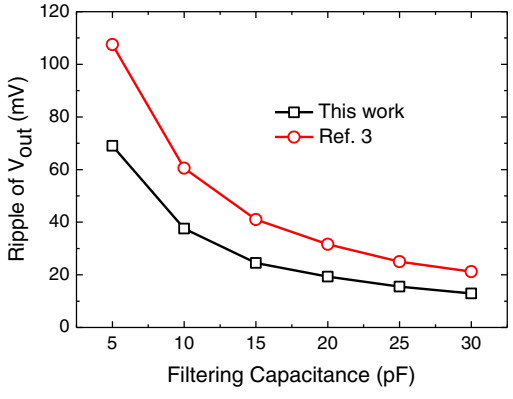

Fig. 7. (Color online) Comparison of the simulated output ripples of the two-stage CPs with $T_D = 20\,ns$ for different filtering capacitances at a frequency of 10 MHz and $V_{DD} = 1.8\,V$.

A comparison of simulated output ripples for different filtering capacitances with $T_D = 20\,ns$ at a frequency of 10 MHz, $I_{out} = 36\,\mu A$, and $V_{DD} = 1.8\,V$ is shown in Fig. 7. The ripple is reduced significantly, especially for small filtering capacitances.

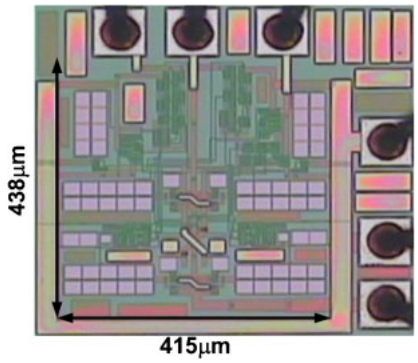

Fig. 8. (Color online) Microphotograph of the proposed PMOS CP circuit.

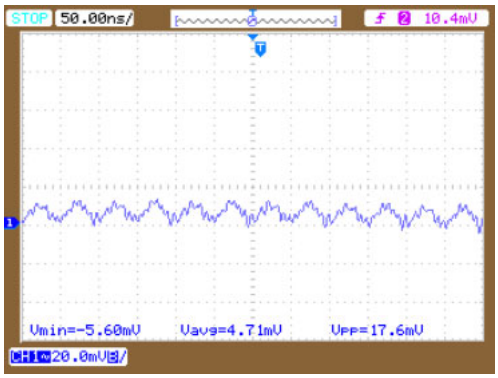

Fig. 9. (Color online) Measured output ripple waveform of the CP with the proposed clock scheme at $V_{DD} = 1.8$ V.

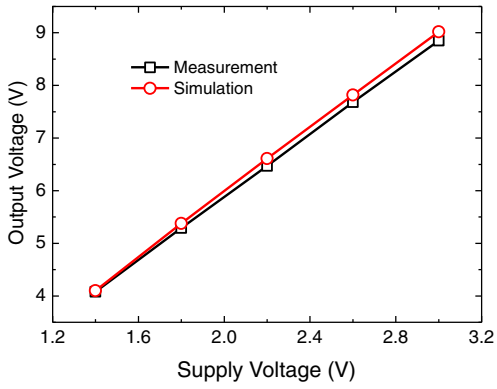

Fig. 10. (Color online) Comparison of the simulated and measured output voltages of the proposed CP for various supply voltages at 10 MHz and $I_{out} = 0$.

Figure 8 shows a microphotograph of the proposed CP circuit in an area of 0.182 mm^2 using 0.35 μm CMOS technology. From Figs. 9–12, the filtering capacitance was estimated to be 30 pF by including all the parasitic capacitances of the pad, packaging, and testing fixtures. Figure 9 shows the output ripple waveform obtained by measuring the AC signals to observe the ripple for $I_{out} =$ 36 μA at $V_{DD} = 1.8$ V with $T_D = 8$ ns.

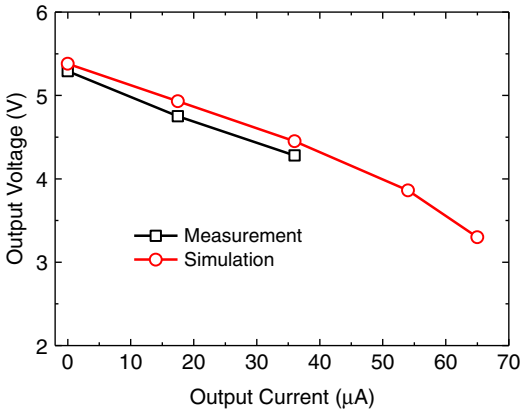

Fig. 11. (Color online) Comparison of the simulated and measured output voltages as functions of output current at $V_{DD} = 1.8$ V for $T_D = 8$ ns.

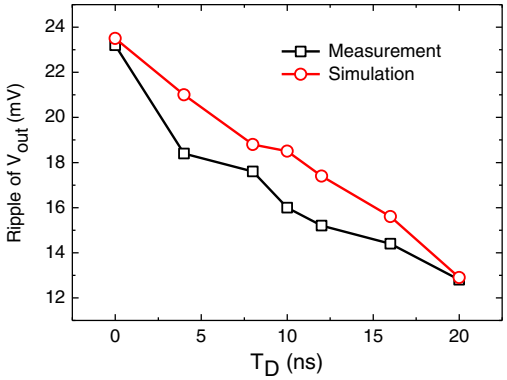

Fig. 12. (Color online) Comparison of the simulated and measured output voltage ripples for various T_D values at $V_{DD} = 1.8$ V for $I_{out} = 36$ μA.

Figure 10 shows the simulated and measured output voltages of the proposed CP for various supply voltages at 10 MHz and $I_{out} = 0$ with $T_D = 8$ ns. The output voltage increases linearly with the supply voltage as expected. The maximum measured voltage gains for the proposed two-stage CP are 97.1 and 98.3% at supply voltages of 1.4 and 3 V, respectively. Figure 11 shows the simulated and measured output voltages for different output currents at 10 MHz, $V_{DD} = 1.8$ V, and $T_D = 8$ ns. The output voltage decreases linearly when the output current increases, as predicted from eq. (2). These results indicate that the proposed clock scheme maintains good pumping ability for various V_{DD} and output current values. Notably, owing to the parasitic effects of the package and testing fixtures, the measured values are slightly lower than the simulated results.

The simulated and measured output voltage ripples for different T_D values and $I_{out} = 36$ μA at 10 MHz and $V_{DD} = 1.8$ V are plotted in Fig. 12. The measured output voltage ripples are 23.2 mV at $T_D = 0$ ns and 12.8 mV at $T_D = 20$ ns. These results imply that the output voltage ripple decreases significantly when T_D increases from 0 to 20 ns. It is worth noting that if T_D is too large, the pumping

gain may be degraded. Thus, T_D should be selected appropriately.

6. Conclusions

In this study, a reduced-ripple two-stage CP is proposed and implemented using the standard 0.35 μm CMOS process in an area of 0.182 mm^2. The proposed clock scheme can reduce the chip area by reducing the on-die filtering capacitance. We also demonstrate that the ripples can be adjusted by modifying the overlapping time T_D. In addition, the proposed two-stage CP also has high voltage gains and high driving capacity with good device reliability. The measured voltage gains of the proposed two-stage CP are more than 97% with V_{DD} higher than 1.4 V. Moreover, the measured ripples can be reduced by about 45% at 10 MHz and $V_{DD} = 1.8$ V using small filtering capacitance. We can expect that a larger area reduction will be achieved if the boosting capacitance used for providing a higher output current is larger.

Acknowledgments

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