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High-Voltage-Tolerant Level Converter for Embedded Complementary Metal–Oxide–Semiconductor Nonvolatile Memories

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In this paper, a high-voltage-tolerant level converter for embedded complementary metal–oxide–semiconductor (CMOS) nonvolatile memories is proposed. The level converter circuit includes a high-voltage driver and a level shifter, which makes use of 1 × V_{DD} devices to generate 2 × V_{DD} signals without overstress. In addition, it features one select signal to make the level converter have the tri-state. The high-voltage driver efficiently stacks two transistors to allow a voltage drop of V_{DD} for each transistor, which helps maximize the driving ability. The level shifter using the cross-coupled structure with small metal–oxide–semiconductor (MOS) capacitors drives the high-voltage driver without the "preconditioning" process. The level converter implemented using the 0.35 μm CMOS process on the area of 0.002 mm^2 was measured at V_{DD} = 3.5 V to generate the output signal swinging from 0 to 7 V.

1. Introduction

The advanced complementary metal–oxide–semiconductor (CMOS) technologies push nanoscale geometries of metal–oxide–semiconductor field-effect transistors (MOSFETs). To avoid high electric field stress, the operating voltages become lower and lower. However, in some applications high-voltage level converters are still required, such as micro electro-mechanical systems (MEMS) device control, power converter switching, and embedded nonvolatile memory control circuits. The on-die high-voltage level converter in the standard CMOS processes is a key component for the system to perform correct functions.

To design a high-voltage level converter circuit, the voltage drops between any two electrodes of a MOSFET must be well controlled for good reliability. High-voltage drivers using large capacitors have been reported.[1,2] They need large area to implement the capacitors, so the cost of the chip is increased. Another tri-state level converter was proposed for 3 × V_{DD} output,[3] but the voltage drops between the drain and the source may have risks of overstress. In addition, it requires four transistors in series at the output stage instead of three, which is the ideal number owing to 3 × V_{DD}. That requirement may degrade the driving ability of the output. The input/output (I/O) buffer[4] enhances the driving ability, but the voltage drops between the gate and the body of some transistors may be larger than V_{DD}, so the overstress issue still exists. The low voltage to transistor–transistor logic (TTL) output buffer[5] utilizes 2.2-V-tolerant MOS transistors to generate 3.3 V output swing signals by stacking two n-type MOS (NMOS) or p-type MOS (PMOS) transistors. The node voltage at the connecting node of the two series transistors is not set to 2.2 V by the other transistors, and is only approximated by V_{gs} = threshold voltage. If the high voltage is higher than 3.3 V, such as 2 × 2.2 V = 4.4 V, one of the MOS transistors is overstressed between the drain and the source.

In this paper, a high-voltage-tolerant level converter is proposed for embedded CMOS nonvolatile memories.[6] Because of the grounded bodies of NMOS transistors in the 0.35 μm CMOS process, we propose a special level converter circuit without large capacitors or overstress with good driving capability. It receives signals with an amplitude of 1 × V_{DD} to generate an output signal with an amplitude of 2 × V_{DD} or a floated output.

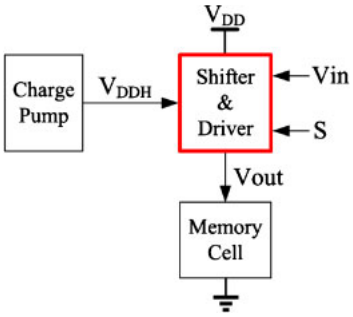

Fig. 1. (Color online) Application of level converter circuit used in the embedded nonvolatile memory.

The organization of this paper is as follows. In the next section, the structure of the circuit is introduced. In §3, the circuits and operations of the high-voltage driver and the level shifter are described. The simulation and the measurement results are demonstrated in §4. The conclusions are given in the last section.

2. Configuration

Figure 1 shows the application of the high-voltage level converter marked by the bold lines between the high-voltage source, such as the 7 V generated by the charge pump, and the multiple-time-program (MTP) cells in the standard 0.35 μm CMOS process.[5] Here, V_{DD} is 3.5 V and V_{DDH} = 2 × V_{DD} = 7 V. The bit-line of the memory cell requires 7 or 0 V during program or erase, and is floated during read. Note that the bit-line voltages are less than V_{DD} during read, so only the voltage variation between 0 V to V_{DD} needs to be considered for the floated output.

The proposed level converter consists of a level shifter and a high-voltage driver with a select signal (S) to drive the bit-line, as shown in Fig. 2. The level shifter provides high-voltage signals to control the driver. Notably, since the level shifter requires small MOS capacitors to boost the voltage level, it is not efficient to deliver large driving current at the output. Moreover, it cannot provide the option of tri-state. The level converter requires two voltage sources, V_{DD} = 3.5 V and V_{DDH} = 7 V, one input signal (V_{in}), and one select signal (S). The voltages of these two signals both

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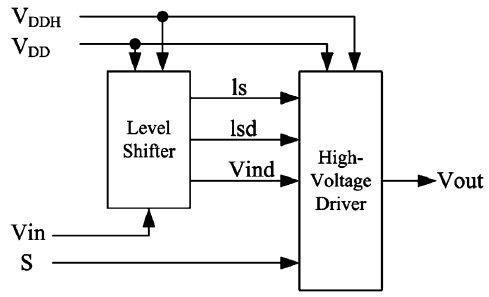

Fig. 2. Level converter consisting of two circuit blocks.

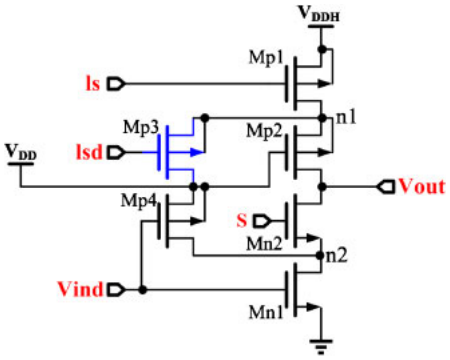

Fig. 3. (Color online) Circuits of high-voltage driver for the bit-line of memory cell.

vary from 0 to V_{DD}. When $S = V_{DD}$, the output (V_{out}) becomes V_{DDH} or 0 V when the input signal (V_{in}) is 0 V or V_{DD}, respectively. The high-impedance status can be achieved when $S = 0$ V and $V_{in} = V_{DD}$, that is, the output is floated.

3. High-Voltage Driver and Level Shifter

3.1 High-voltage driver

The high-voltage driver is composed of a pair of two NMOS and two PMOS transistors in series with two nodes n1 and n2 determined by two PMOS transistors Mp3 and Mp4, as shown in Fig. 3. Note that because the Si wafer substrate is p-type, the bodies of all NMOS transistors must be grounded owing to the twin-well process. Therefore, as many as possible of the commonly used NMOS transistors were replaced by PMOS transistors for both circuits in Figs. 3 and 5. For example, Mp3 is a PMOS transistor with its source tied to the body. Alternatively, if the triple-well process is available, it can be replaced by an NMOS transistor with its body and gate tied to V_{DD} and the node "ls", respectively. The only possible risk of overstress is the reverse PN junction bias between the drain and the body of Mn2, which is acceptable in the 0.35 μm CMOS process.

The node voltages of three possible operation situations of the high-voltage driver are listed in Table I. Notably, the fourth mode with $S = 0$ V and $V_{in} = 0$ V is not permitted. Because V_{out} becomes V_{DDH}, transistor Mn2 is overstressed. Figure 4 illustrates the node voltages and on/off states of each transistor for these three situations. The transistors sketched by black lines are on, while those shown by gray lines are off. We can observe that no transistors suffer overstress problems.

Table I. Corresponding node voltages for different output conditions in the high-voltage driver.

V_{in}	S	V_{ind}	ls	lsd	n1	n2	V_{out}
V_{DD}	V_{DD}	V_{DD}	V_{DDH}	0 V	V_{DD}	0 V	**0 V**
0 V	V_{DD}	0 V	V_{DD}	V_{DDH}	V_{DDH}	V_{DD}	V_{DDH}
V_{DD}	0 V	V_{DD}	V_{DDH}	0 V	V_{DD}	0 V	**Floated**

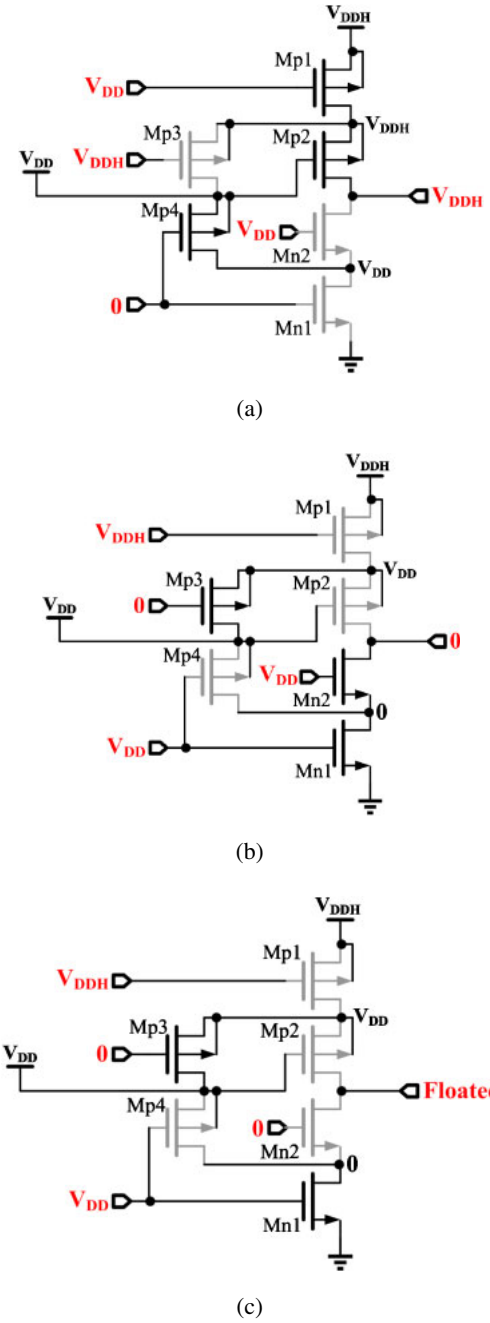

Fig. 4. (Color online) On/off state of the transistors of the driver: (a) when V_{out} is V_{DDH}, (b) when V_{out} is 0 V, (c) when V_{out} is floated.

In Fig. 4(a), when $S = V_{DD}$ and $V_{in} = 0$ V, ls, lsd, and V_{ind} are V_{DD}, V_{DDH}, and 0 V provided by the level shifter. Thus, Mp1, Mp2, and Mp4 are on to raise $V_{out} = V_{DDH}$, and n2 becomes V_{DD} to avoid overstress for Mn1, Mn2, Mp3, and Mp4. Similarly, Fig. 4(b) shows that when $S = V_{DD}$ and $V_{in} = V_{DD}$, Mn1, Mn2, and Mp3 are turned on to ground V_{out}

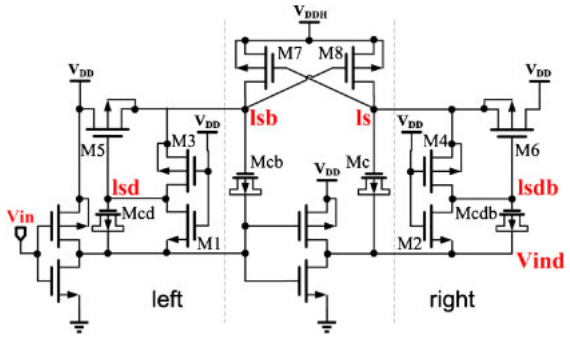

Fig. 5. (Color online) Level shifter circuit to provide the three control signals (lsd, ls, and V_{ind}) for the driver.

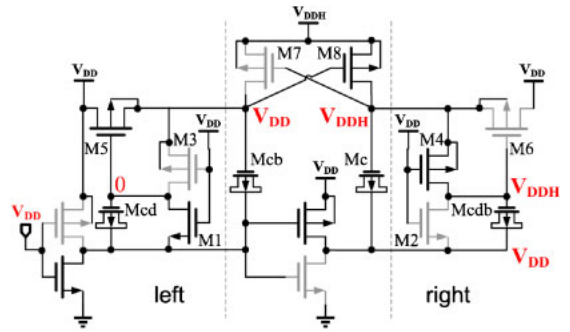

Fig. 6. (Color online) On/off state of the transistors of the level shifter when V_{in} is V_{DD}.

and n1 is set to V_{DD} to avoid overstress of the four PMOS transistors. Figure 4(c) illustrates the third case, that is, when $S = 0\,V$ and $V_{in} = V_{DD}$, Mp2 and Mn2 are off, so V_{out} is floated, which allows V_{out} to vary from 0 V to V_{DD} if it is driven by some other circuits.

3.2 Level shifter

The level shifter provides the control signals for the high-voltage driver, as shown in Fig. 5. If the voltage drops across the two MOS capacitors Mc and Mcb are V_{DD}, the cross-coupled PMOS structure can generate the signals at the nodes "ls" and "lsb", that vary between V_{DD} and V_{DDH}. Here, the right-hand side of the right dash line and the left-hand side of the left dash line are termed the right wing and the left wing, respectively. However, the voltage drops across Mc and Mcb may not be V_{DD} initially. For example, if the voltage drops are 0 V initially, after the first cycle of V_{in} changing from 0 V to V_{DD}, and back to 0 V, the drops are different. Thus, several cycles are needed to make the drops eventually equal to V_{DD}. Here, this process is named preconditioning.

With the help of the right and left wings, the voltage drops across Mc and Mcb can be set to V_{DD} at any time. This can be explained using Fig. 6, which shows the node voltages for $V_{in} = V_{DD}$. The black-lined transistors are "on", and the gray-lined transistors are "off". Since transistor M1 is on to make the PMOS transistor M5 transfer V_{DD} to "lsb", the voltage drop across Mcb is enforced to V_{DD}. Then, M8 and M4 are on for "ls" to have V_{DDH} and the voltage drops across both Mcb and Mcdb are V_{DD}. If the MOS capacitor

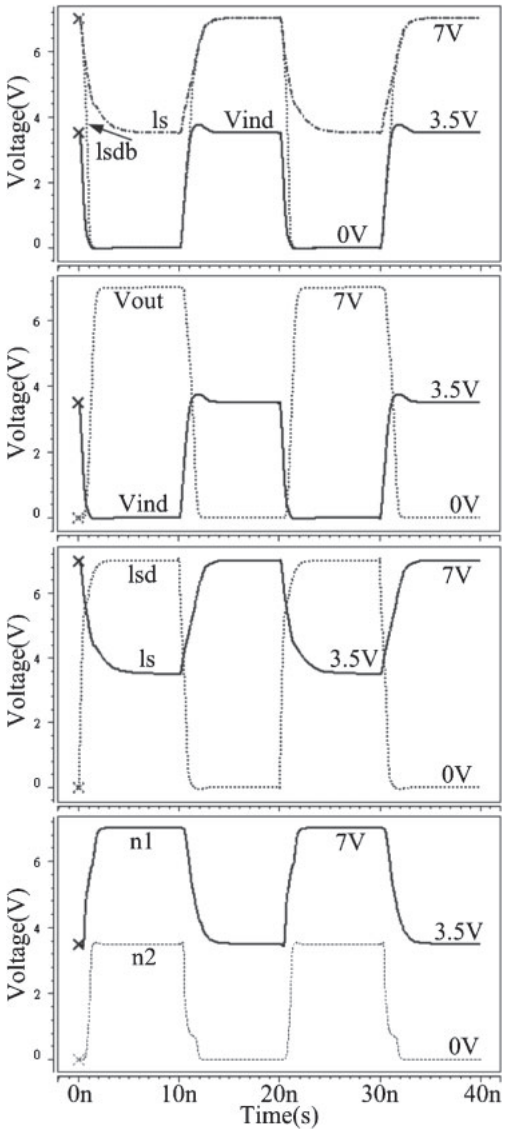

Fig. 7. Simulated waveforms of the node voltages for the driver with the output capacitance of 0.5 pF at 50 MHz.

Mcdb does not exit, because node "lsdb" is 0 V before $V_{in} = V_{DD}$, more leakage current may go through M6 just when V_{in} becomes V_{DD}. Thus, the role of Mcdb is to avoid charge leakage through M6 and speed up the node "ls" becoming V_{DDH}. Since the circuit is symmetric, the on/off conditions are reversed for $V_{in} = 0\,V$. Notably, the four MOS capacitors help provide the bias voltages of the nodes "lsd", "lsb", "ls", and "lsdb" for gates M5, M7, M8, and M6, respectively. Their sizes need not be large, so the capacitance values are tens of fF. Another function of the level shifter is to generate a large swing signal "lsd" that varies from 0 V to V_{DDH} for Mp3 of the high-voltage driver.

4. Simulation and Measurement Results

The post-layout simulated waveforms of the proposed level converter are shown in Fig. 7 with the output capacitance 0.5 pF at 50 MHz. In the figure, the input, internal, and output node voltage waveforms of the high-voltage driver are demonstrated in four panels. From the waveforms of the nodes, we can observe that the voltage difference between

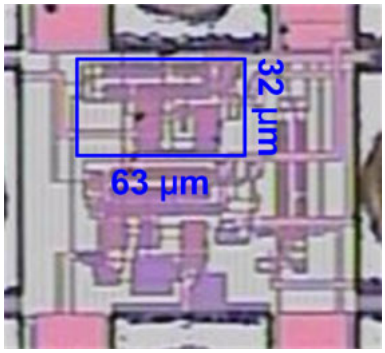

Fig. 8. (Color online) Micrograph of the proposed level converter circuit.

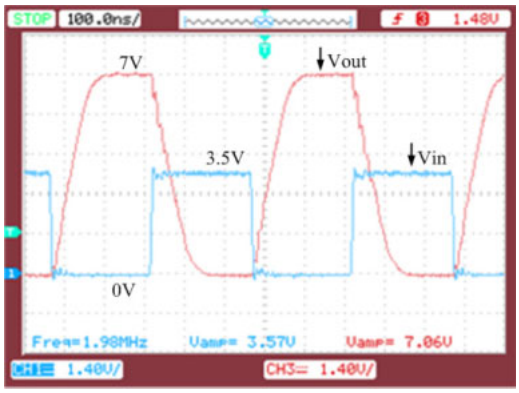

Fig. 9. (Color online) Measured input and output waveforms at 2 MHz.

any two nodes in any transistor is well controlled to avoid overstress at steady states. For example, in the first panel, V_{sg} of M6 and V_{sd} of M4 can be obtained by subtracting the waveform of "ls" from that of "lsdb". Similarly, $V_{gd} = V_{gs} = V_{gb}$ of Mcdb is generated by subtracting the waveform of "lsdb" from that of "V_{ind}".

The micrograph of the die for the proposed level converter is given in Fig. 8. The chip area of the proposed high-voltage-tolerant level converter circuit is 0.002 mm^2. The measured waveforms of the output and the input with $S = V_{DD}$ are demonstrated in Fig. 9. The output is successfully switched between 0 V and V_{DDH}. Note that the longer delay is due to the loading effect in the measurement environment. The delay time should be much shorter, if the level converter circuit is used within the chip.

To test the floated state with S varying between 0 V and V_{DD}, the output is connected to an external resistor with the other electrode biased at 1 V. The measured waveforms are shown in Fig. 10. It can be observed that the output gradually becomes 1 V when $S = 0$ V. Since the external resistance is large, the variation is also slow.

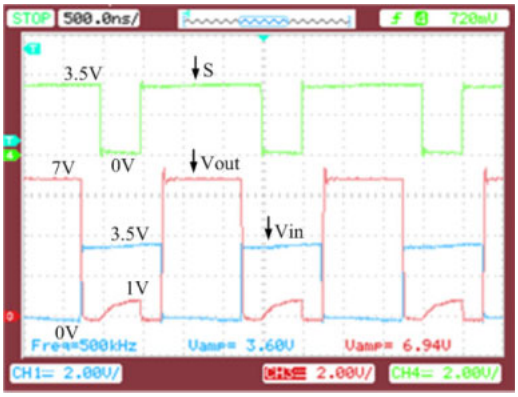

Fig. 10. (Color online) Measured waveforms with the floated output at 500 kHz.

5. Conclusions

The high-voltage tri-state level converter circuit without overstress in every transistor for embedded CMOS non-volatile memories was proposed and fabricated in the 0.35 μm CMOS process. The output stage of the driver only needs two transistors in series for pull-up or pull-down, which helps enhance driving ability. Moreover, since the bodies of NMOS transistors must be grounded, as many PMOS transistors as possible are utilized to avoid overstress. Furthermore, the proposed level shifter without "preconditioning" can produce 0 V to V_{DD} and 0 V to V_{DDH} control signals at the same time. It is shown that the proposed circuit is a good and reliable level converter circuit for embedded applications of $2 \times V_{DD}$ signal swings using the standard CMOS technologies.

Acknowledgments

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