A Bus-Based Static Volumetric Three-Dimensional Active Matrix Display With a One-Dimensional Connection

Wei-Liang Lin and Cheng-Yu Chung

***Abstract*—This study explores a bus-based static volumetric (SV) three-dimensional (3D) active matrix display (AMD) with a one-dimensional (1D) connection. The 1D connection enabled implementation by reducing the physical structure and electrical connection of the 3D display. In the bus-based display system, each light-emitting diode (LED) is turned on or off according to the frame rate of the video. A prototype design demonstrated a system with a controller chip size of 1.1 mm×0.9 mm manufactured by a 0.35 μm CMOS process, an LED chip size of 1.0 mm×1.0 mm, and a four-wire bus of 4.4 mm in width and 1.1 mm in thickness.**

***Index Terms*—Active matrix display (AMD), bus-based control, integrated circuit, static volumetric three-dimensional AMD (SVAMD), volumetric 3D display.**

I. Introduction

THREE-DIMENSIONAL (3D) display systems can be divided into two types: 1) autostereoscopic and 2) non-autostereoscopic. A viewer of an autosterescopic 3D display system does not need to wear specific glasses [1]. A volumetric 3D display system belongs to the autostereoscopic type. In a volumetric 3D display system, the display image space and the display objects are identical in size [2]. Two types of volumetric 3D displays are available; that is, swept-volume and static. Both are commercially available products with millions of voxels [3]–[6]. A voxel is a display lighting element. Static displays have the advantage of not containing moving mechanical parts. A volumetric 3D display cannot compete with a commercial 3D display, which is based on a two-dimensional (2D) method, regarding performance and cost. However, almost half of a sphere view angle from a volumetric 3D display is advantageous. Furthermore, a commercial 3D display "tricks" a brain into perceiving a 3D image, which causes fatigue. Therefore, volumetric 3D displays receive attention for specific applications, such as medical images, air traffic control, and games.

Current mainstream static volumetric systems use crystals as the image spaces, with sizes as large as 19 mm × 18 mm × 100 mm [4]. However, it is difficult to manufacture a display space with either length, width, or depth, larger than 1 m. An intuitive static volumetric 3D active matrix display (SVAMD) is a type of static volumetric display that was previously proposed; however, it remained mostly in the concept phase with few implementations, because of an inability to fulfill several requirements [2], [6]. Still, there is a commercial available product based on a stack of LCD panels with limited view angles [6]. An SVAMD is composed of light sources in a 3D space. The unit lighting source and connections must be substantially small to be successful; therefore, an LED with its controller, called a voxel cell, was used in this study. Figs. 1 and 2 show two voxel cells of different sizes in a display. The differing colors of the cells were used to create a 3D illusion, but in reality, the cells are identical. It was assumed that the system with the smaller cell exhibited superior performance. Current LED chips can be

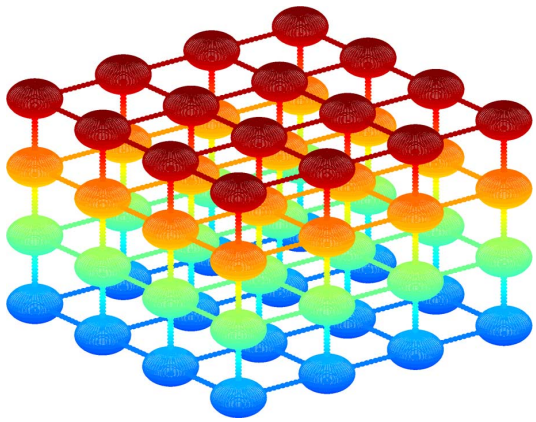

Fig. 1. An SVAMD with a larger cell size.

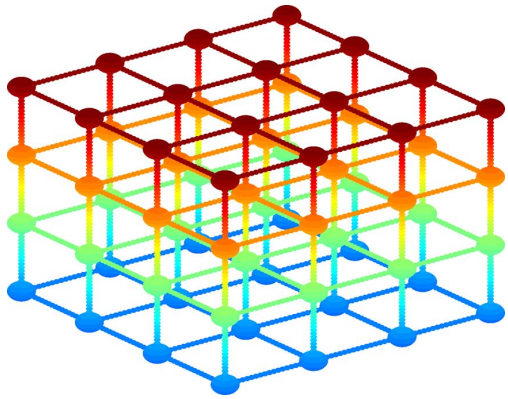

Fig. 2. Another SVAMD with a smaller cell size.

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as small as 0.25 mm×0.25 mm, and any controlling device must not be considerably larger in size. A smaller or even nonexistent global physical and electrical connection is crucial for reducing light path obstruction. Most important, the display must be easy to implement. If the dimensions of a voxel cell and the connections are not sufficiently small, the requirement can be met by extending the distance between voxel cells. Compared with crystal based static volumetric displays, an SVAMD is natural to large scale applications, such as large lanterns in an Asian Lantern Festival or parades at night.

This study proposes a bus-based 1D connection SVAMD to enable the implementation, and demonstrates a realization based on modern semiconductor technology.

Bus-based lighting systems are common. A recent U.S. patent provides methods and systems that can address each light with an Ethernet-based protocol [7]. The disadvantage is that large package space is required to include such an integrated circuit in a voxel cell. One U.S. patent uses an inter-integrated circuit (I2C) protocol with four wires, and requires an extra high-frequency generator to adjust pulse width modulation (PWM) generators for controlling the voxel cell [8]. Another U.S. patent uses a common bus with three wires to communicate with controllers [9]; however, each controller requires its own stable non-precision clock generator. All of these patents have a similar disadvantage; that is, the controllers have a large form factor. This study focused on simplifying the design of the controller to reduce the form factor. The authors did not find the chip sizes and off-chip passive components from the relevant documents, and used only the implemented functions to estimate that the proposed controller chip was smaller.

The remainder of this paper is organized as follows. Section II explains the manner in which a bus-based system with only four global connection nets reduces the connection of a related SVAMD and makes the SVAMD easy to implement; Section III provides a description of the proposed bus-based system; Section IV presents the details of a prototype and includes a demonstration; Section V provides a limitation discussion; and finally, Section VI offers a conclusion.

II. An SVAMD With a 1D Connection

Fig. 3 depicts an SVAMD with a possible global connection similar to the column-row arrangement of a conventional liquid crystal display (LCD) panel [2]. Two $N^{0.5}$ global nets were required to connect to a graphics engine in which control signals are generated, where N is the number of total cells. Each cell requires a control circuit similar to an LCD panel, in which each pixel has a thin-film transistor to turn a liquid crystal cell on or off. Producing such a system is a complex process. $N^{1/3}$ layers of 2D sheets must be produced and fixed with a constant distance. Each of the $2N^{0.5}$ global nets requires a connection.

Fig. 4 depicts the global connection of a proposed bus-based SVAMD that reduces the $2\mathrm{N}^{0.5}$ distinguished global nets to a constant number of four by embedding an additional receiving circuit into the original switch with each LED.

Each line in Fig. 4 is composed of four global nets. Because humans have horizontal vision, Z-direction thin columns have a less obstructive effect. A manufacturer can produce a long general purpose Z-dimensional string of cells with automatic assembly techniques, and customize X–Y-dimensional arrangement by weaving, as illustrated in Figs. 5 and 6. It is assumed that this bus-based SVAMD is considerably easier to produce.

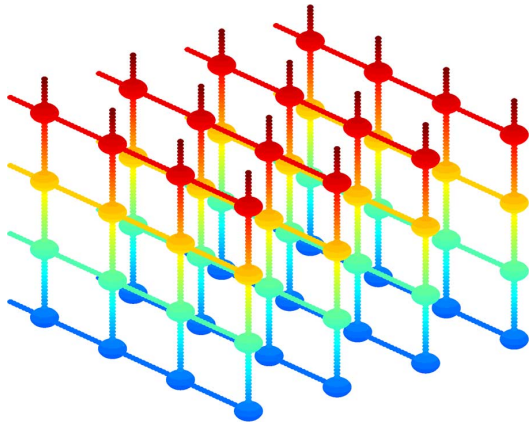

Fig. 3. Column-row style connections in 3D space.

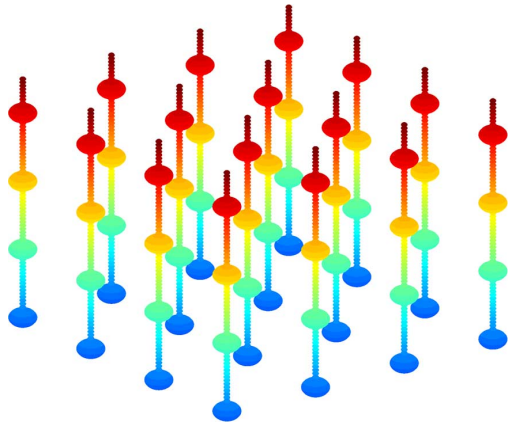

Fig. 4. Bus-based connection in a 3D space.

III. Details of the Proposed System

A. Signaling Protocol

The proposed signaling protocol is based on the persistence of vision to simplify the control algorithm, thereby reducing the required usage area on the chip. The bus signaling method is source synchronization [10]. The signaling functions as follows—a designed signal is placed into the bus, and each voxel cell listens for its own address. Once its own address is received, the specific cell turns on for a frame period.

B. Refresh Rate and Dimension Specification

Assume that there are 1024 cells. Each address with a head and a tail bits uses 12 bits, and the refresh/frame period is 42 ms, as that in a contemporary theatrical film. The most demanding situation is that in which every light is on, which requires (12 bits×1024 cells) cycle to fulfill the task within a period. This indicates 12 × 1024/(42 ms) = 293 kHz clock rate. With the same frame rate as that in a contemporary theatrical film, the system can easily create movie effects.

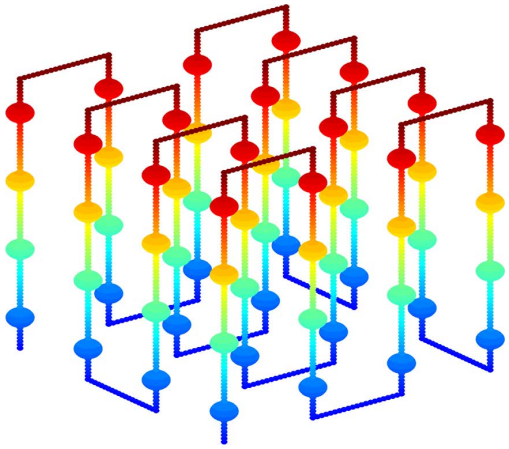

Fig. 5. All cells can be connected into one long string of cells.

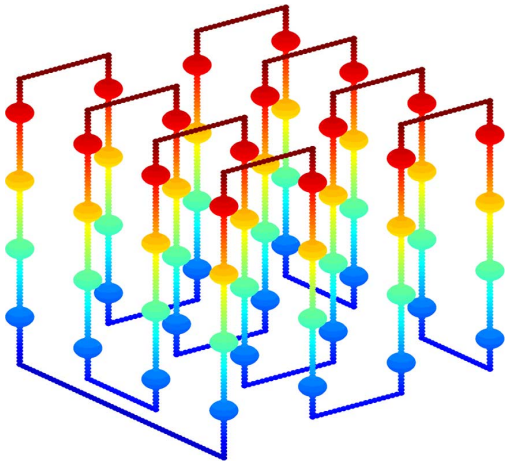

Fig. 6. The string becomes a loop to improve reliability.

C. System Block Diagram

The bus-based system block diagram with each cell connected in a 1D layout is illustrated in Fig. 7. The limitation of 1024 cells originates from the challenges of the current requirement of the total numbers of cells and the signaling over a long distance.

A simulation of the transmission lines was performed using the circuit shown in Fig. 8. Each control cell was substituted with an equivalent 10 pF capacitance. All of the used wires are 18 AWG twisted wires with an impedance of 76 Ω. A total of 1024 control cells were assumed, and each control cell was attached to the bus with a set of 5-cm-long stubs. One stub was attached to the signal wire which was either DATA or CLK, and the wire's stubs were separated by a 10-cm distance in the bus. A termination resistor of 45 Ω terminated the bus. The value did not equal 76 Ω because the wire impedance was changed by the periodic connections of the 10-pF capacitance loads. The control signal generator drove the bus with randomly generated 3.3 V and 0 V with transition intervals of 100 ns. Consequently, the CLK rate was overstrained at 10 MHz compared to the system-specified 293 kHz range. Four eye diagrams from various portions of the bus are shown in Figs. 9–12. The eyes were open and had heights of at least 0.2 V. Therefore, with a proper design, transmitted digital data can be recovered.

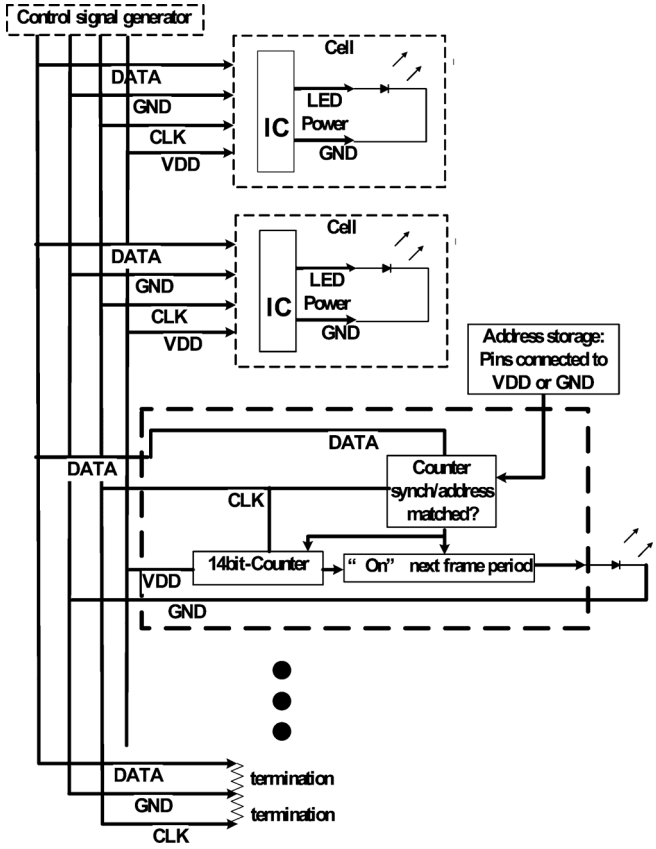

Fig. 7. Bus-based lighting system with a detailed controller.

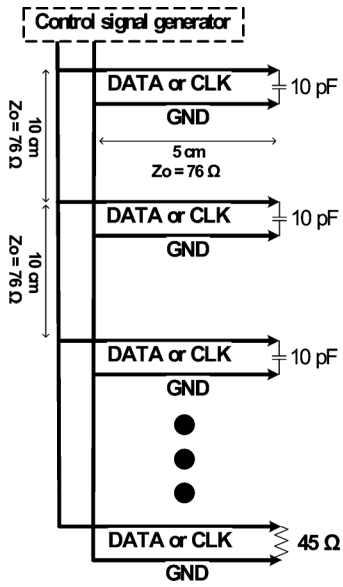

Fig. 8. Circuit diagram for the transmission line simulation.

Furthermore, the timing budget between the clock and data for the source synchronous system was a half-clock cycle [10]. When the clock rate was 293 kHz, the timing budget was 1.7 μs. This timing budget alleviated the data recovery circuit.

D. Controller Block Diagram

In the bus, the data transmission format is a header, followed by a message. The message is either a 14 bit-counter reset mes-

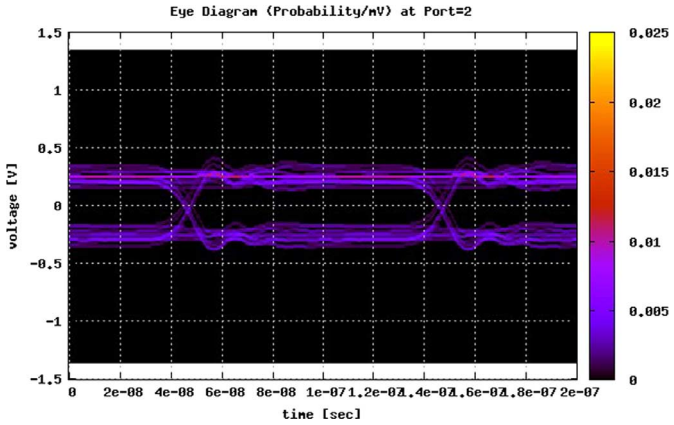

Fig. 9. Eye diagram of the 1024th cell node at the end of the bus.

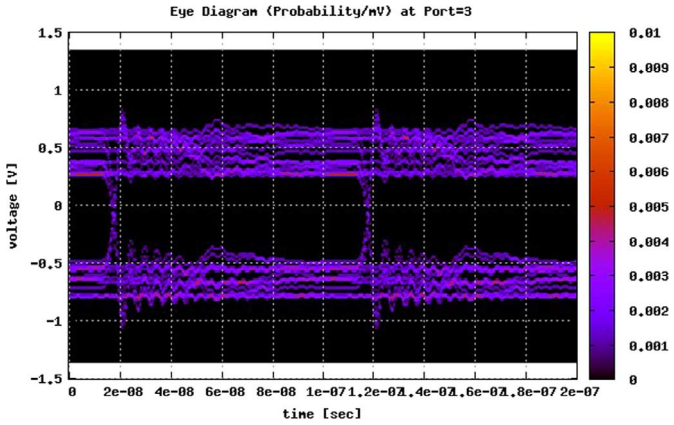

Fig. 10. Eye diagram of the 35th cell node.

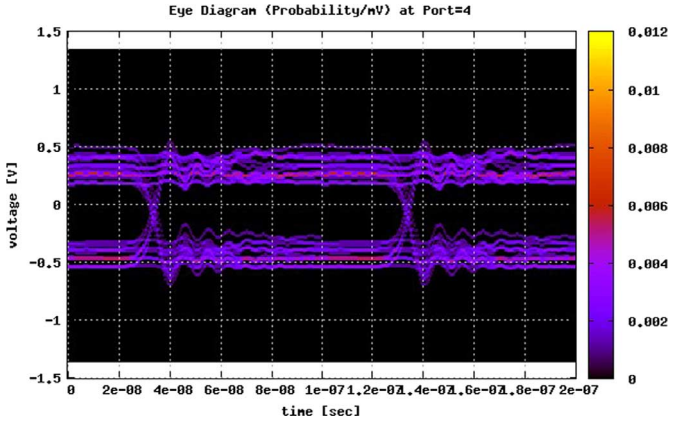

Fig. 11. Eye diagram of the 288th cell node.

sage or an address message. Fig. 7 also illustrates the block diagram of a controller. The 14 bit-counter records the time of a frame, and the 14 bit-counter reset message synchronizes the frame boundary of each cell. A recognized address message signals that the cell will be in the "on" status in the following frame period (42 ms). With a 293 kHz clock rate, the 14 bit-counter sends an overflow signal every $2^{14}/293\text{k} = 56$ ms to signal a frame period. Therefore, the clock rate must be slightly faster in the implementation. Consequently, the frame rate will be

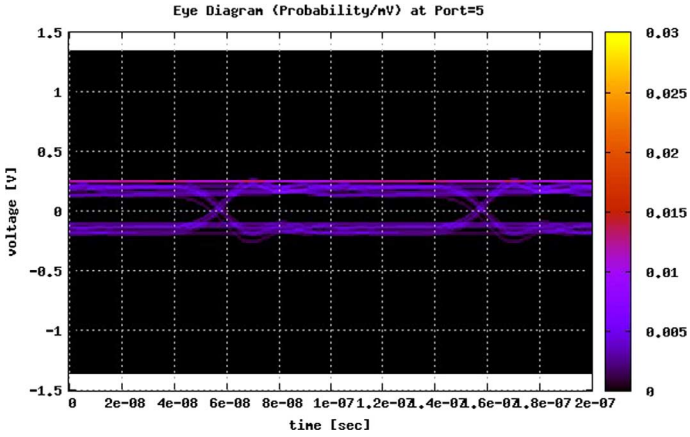

Fig. 12. Eye diagram of the 960th cell node.

faster than required. Currently, the cell address is set through pad bonding.

E. Power Rail Consideration

A low power LED may consume only 5 mA current; however, 5-A current deserves special consideration with 1024 LEDs. A solution is to connect thick power and ground nets in the bends from outside the system. For example, 15 bends are shown in Fig. 5.

F. Form Factor Consideration

Ideally, both the LED and controller chips must be placed on the four nets directly to reduce the voxel cell form factor. Therefore, the controller must not use any off-chip component. Another problem is that a controller address is set through pad bonding, and the controller chip area may be limited by the number of on-chip pads. A possible solution is to include an on-chip ROM.

IV. The Prototype

A controller was designed and taped-out, and the authors created the prototype by using a limited number of chips, as follows:

A. Control Signal Generator

A field-programmable gate array (FPGA) provided CLK, DATA, VDD, and GND voltages. Controllers and LED's were attached to the four-wire-bus at 2.4 cm intervals.

B. Controller

The controller chip size was 1.1 mm$\times$0.9 mm, and was manufactured by a 0.35 μm CMOS process, as shown in Figs. 13 and 14. In addition to the four global nets and one LED power net, additional pads were used for address setting. In this prototype, only eight bits of address were used, which limited the cell number to 256. Circuits for setting flip-flop initial condition, CLK and DATA signal conditioning, and electrostatic discharge (ESD) purposes were included on the chip to reduce the total form factor because off-chip passive components were not

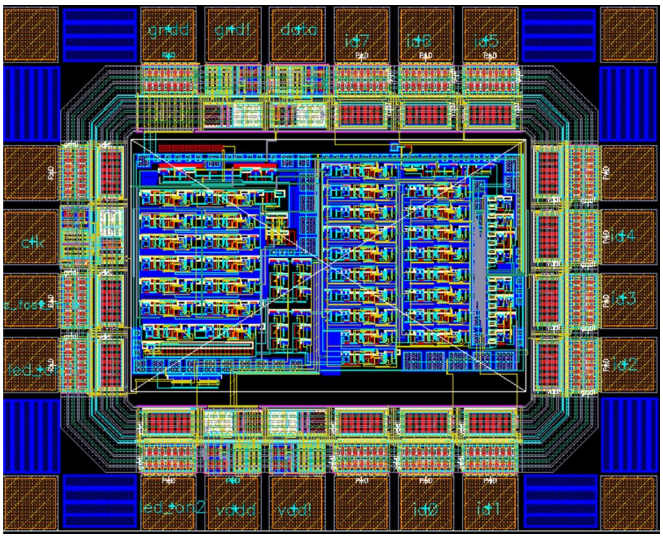

Fig. 13. Controller chip layout.

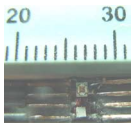

Fig. 14. Controller and LED chips glued to the four-wire bus but before bus bonding connection. There is a rule above.

used, as shown in Fig. 14. Because a large area is used by digital circuits, the chip area can be further reduced by using more advanced processes.

For a single controller, the power consumption was measured as 1.4 mW during standby, and 68.6 mW with a 3.3 V $V_{\rm dd}$ current of 20.8 mA when the attached LED was activated. The activated LED consumed a current of 20.5 mA, or equivalently, it emitted a radiant power between 16 and 22 mW, according to the data sheet of the InGaN blue LED. Radiant power is a measurement of brightness. Human eyes could easily see the activated LED from meters away. The controller operated correctly up to a clock rate of 3 MHz, which was sufficient for the system's required 293 kHz range. The 3-MHz rate was limited by the driving FPGA.

When 256 controllers were connected to a single bus, the standby power was 0.3 W. The 256 activated controller/LED pairs had a total $V_{\rm dd}$ current of 5.3 A, and the power consumption was 18 W. Therefore, the system with 256 controller/LED pairs was practical for power consumption.

C. Final System and Demonstration

Fig. 14 shows the system placement of a controller and an LED with four wires before bonding the wire connections. The size of each LED is 1.0 mm × 1.0 mm. The width and the thickness of the four-wire bus are 4.4 and 1.1 mm, respectively. Three voxel cells are connected to the bus, as shown in Figs. 15–22. The required action is to count from 0 to 7, assuming that each cell is one binary digit. The figures demonstrate that the three voxel cells can be turned on and off arbitrarily. The second bit cell has a lower light strength because of an over-thick protective glue cover.

Fig. 15. System with count zero.

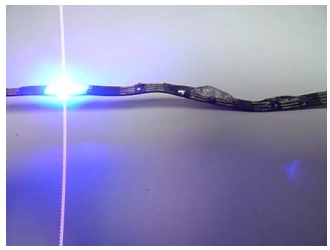

Fig. 16. System with count one.

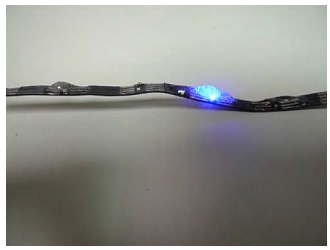

Fig. 17. System with count two.

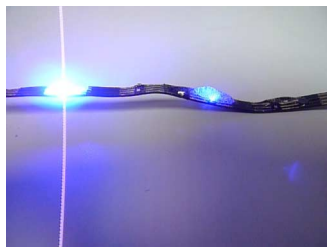

Fig. 18. System with count three.

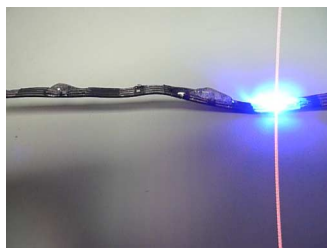

Fig. 19. System with count four.

D. Bonding Yield Improvement

It is difficult to bond the pads of a controller and its companion LED to the four wires when setting the chip address because the bonding planes of "bonding from" and "bonding to" are not at the same level. The controller chip was redesigned

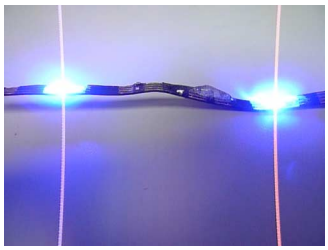

Fig. 20. System with count five.

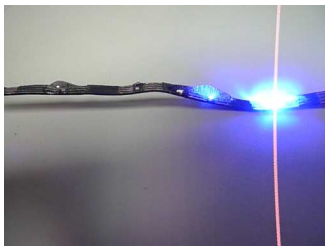

Fig. 21. System with count six.

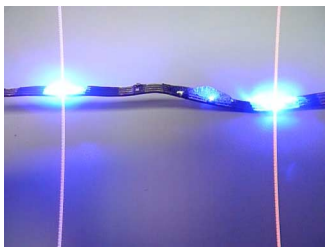

Fig. 22. System with count seven.

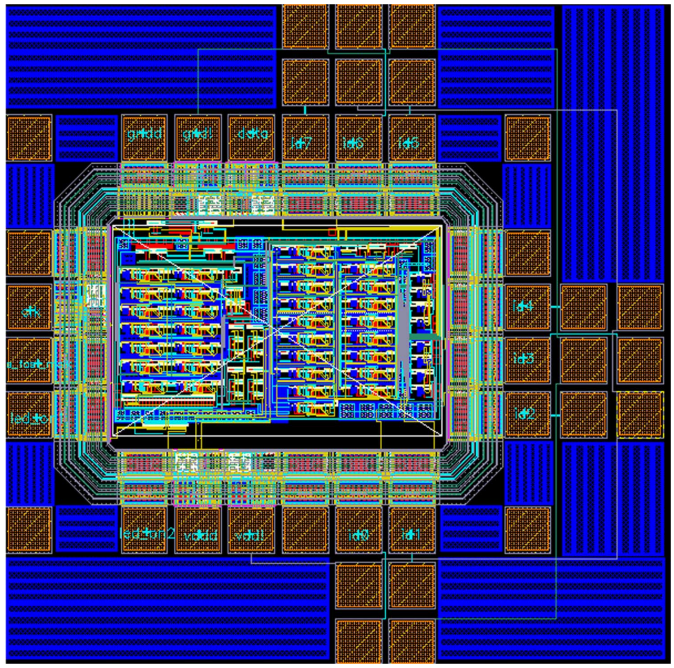

Fig. 23. Controller chip layout with on-chip address assignment through bonding traces.

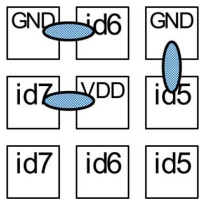

Fig. 24. Three bonding traces set id5, id6, id7 to 0, 0, 1, respectively.

to ensure that each address setting pad neighbored both the VDD and GND pads, similar to the eight three-layer stacking pads shown in Fig. 23. The resulting address setting through bonding traces is easier because the bonding can target between an address pad and a neighboring VDD/GND pad and result in shorting of the two pads without connecting to the four wire bus, as shown in Fig. 24.

V. Limitations and Applications

Although the proposed system eases the construction of a 3D SVAMD, several limitations were observed, as follows.

A. Cell and Wire Dimensions

The first limitation originates from the cell and wire dimensions. The vision blocking effect is not negligible, and renders such a system realistic only when the cell-cell distance is sufficiently large compared with the cell/wire dimensions. Consequently, the resulting SVAMD is large compared with crystal-based static volumetric 3D displays [4], and can be complementary to them. Further research is required to determine the proper dimensions.

B. Cost

Each voxel cell requires a controller and an LED. A system with $100\times100\times100$ voxel cells is costly when considering only the required number of cells. Therefore, it is not suitable for household usage in the current stage.

C. Display Contents

New investments on the proper contents are required because the display resolution lags from the current 3D art.

D. Applications

Considering these limitations, display arts, such as those in commercial outdoor displays and games, are the most likely applications.

VI. Conclusion

This paper proposes a bus-based 3D SVAMD constructed through a 1D connection to reduce global connections and enable implementation. A system based on the persistence of vision was designed, the related controller was manufactured, and a prototype was demonstrated. The near future objectives are to improve the yield of cell attaching, simplify the method of assigning an address to a controller cell, reduce the four-wire bus width, and subsequently produce a larger system.

Acknowledgment

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