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An Enhanced PMOS Charge Pump for Low Supply Voltage Applications

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1. Introduction

The charge pump circuit is a DC-DC voltage converter, to generate a positive voltage that exceeds the supply voltage. It has been extensively applied to flash memories, EEPROM, LCD displays, and so on. The conventional schemes are based on the Dickson structure using NMOS transistors[1]. However, threshold voltage and body effect degrade the performance as the stage number is increased.

Racape *et al.*[2] proposed a PMOS charge pump (CP), which can reduce the influence due to threshold voltages, keep low voltage difference between any two electrodes in a transistor, and can be implemented using a low-cost twin-well CMOS process. However, the boosted gate voltages are degraded significantly for lower supply voltage or higher output current. That results in lower output voltages. Another simple CP[3] can avoid this drawback, but higher voltage differences in transistors may cause reliability problems. In this paper, a simple two-phase clock scheme is proposed to increase the overdrive voltage of gates without reliability issues.

2. Analysis of Driving Capability

Figure 1(a) shows one stage of the PMOS charge pump[2] with four-phase clock waveforms whose amplitudes vary from 0 to V_{DD}. Every stage of the PMOS charge pump consists of six transistors, a pair of boosting capacitors, C_1 and C_2, and a pair of auxiliary capacitors, C_{a1} and C_{a2}. V_{in} is V_{DD} for the first stage and is connected to V_{out} of the previous stage. For the first stage, the voltages at nodes 1 and 2 vary from V_{low} to $2V_{DD}$. V_{low} can be expressed as $V_{in}+V_t-V_{DD}/\left(1+C_{par}/C_{ai}\right)$, where C_{ai} (i=1 to 2) is the auxiliary capacitance and C_{par} is the total parasitic capacitance at node 1 or node 2. In normal operation, the supply voltage has to exceed $2V_t(1+C_{par}/C_{ai})$.

The theoretical boosted output voltage of an N-stage positive charge pump is $V_{boost}=(N+1)V_{DD}-I_{out}R_{out}$, where I_{out} is the current delivered to the output and R_{out} is the output resistance. When the resistance of the MOS transistors is taken into account, R_{out} can be written as[4]

$$R_{out}=\frac{N}{2fC_i}\coth\left(\frac{T_{on}}{r_{on}C_i}\right) \quad (1)$$

where C_i (i=1 to 2) denotes the pumping capacitance, f is the clock frequency, T_{on} is half of the period, and $r_{on}\cong L/\mu C_{ox}WV_{ov}$. V_{ov} is the overdrive voltage. For Racape's charge pump, it is given as

$$V_{ov}=V_{DD}-V_{low}-V_t-I_{out}R_{out} \quad (2)$$

It implies lower supply voltage or larger output current results in lower V_{ov} and, therefore, higher r_{on} and R_{out}, as well as lower V_{boost}.

3. The Enhanced PMOS Charge Pump

A two-phase clock scheme for Racape's charge pump to enhance driving capability is presented in Fig. 1(b). Notably, the four-phase clocks are not required. According to Fig. 1(b), two auxiliary clocks ϕ_{1a} and ϕ_{2a} are generated from two out-of-phase clocks ϕ_1 and ϕ_2 by a pair of level shifters. Note that many different level shifters can be used. Here, a simple version is used in this paper. One level shifter has three transistors. When ϕ_1 is low and ϕ_2 is high, transistors N_1 and P_1 are turned on. At this moment, ϕ_{1a} goes to low and charge is transferred from V_{DD} to node A. Then, ϕ_1 switches to high and ϕ_2 goes to low, transistors N_1 and P_1 are turned off and transistor P_2 is turned on to make ϕ_{1a} become $2V_{DD}$. The operation of the auxiliary clock ϕ_{2a} is similar to that of clock ϕ_{1a} but with a 180° phase difference. Since the voltages at node 1 and node 2 are varied from 0 to $2V_{DD}$, according to Eqn. (2), the overdrive voltages of M_1 and M_4 are increased to $V_{DD}-V_t-I_{out}R_{out}$, as shown in Fig. 2 for V_{DD} = 1.8V and I_{out} = 0. It is worth noting that the voltage differences between any two electrodes are still less than V_{DD}. In addition, the supply voltage of the proposed method can be reduced from $2V_t(1+C_{par}/C_{ai})$ to $V_t(1+C_{par}/C_{ai})$.

4. Simulation and Measurement Results

These two different two-stage charge pumps were simulated using 0.35μm CMOS technology. The charge pumps were designed using the same clock frequency, and transistor sizes, as well as the pumping capacitance and the auxiliary capacitance of 30pF and 0.5pF, respectively.

In Fig. 3, the boosted output voltages of Racape's and the proposed charge pumps are shown using post-layout simulations. The proposed charge pump has higher boosted voltage than that of Racape's charge pump with more than 30% of voltage gain.

Figure 4 compares the performance of Racape's and our proposed charge pumps at frequencies of 10MHz and 12MHz with V_{DD} = 1.8V and different loading currents. In general, the proposed circuit has higher boosted voltages than Racape's charge pump, since the proposed pump has higher overdrive voltages. That indicates the proposed charge pump can be operated at lower supply voltages.

Figure 5 is the chip microphotograph of the proposed charge pump with area about 1.538mm^2. The measured boosted waveform at a frequency of 10MHz and a supply voltage of 1.8V is demonstrated in Fig. 6. The voltage gain is about 98%. The measured boosted voltages of the proposed charge pump for different supply voltages without loading current are shown in Fig. 7. More than 97% of voltage gain is achieved when supply voltage is higher than 1.4V. Figure 8 demonstrates the agreement between the

simulated and measured boosted voltages for different supply voltages and loading currents. Figure 9 shows the measured power efficiencies of the proposed charge pump for different loading currents and frequencies at a supply voltage of 1.8V. The maximum efficiencies for 10MHz and 8MHz are 56.8% and 59.7%, respectively.

5. Conclusions

The proposed two-phase PMOS charge pump fabricated using 0.35μm twin-well CMOS technology with area of 1.538mm^2 achieves higher voltage gain and power efficiency than those of Racape's PMOS charge pump. With the new clock scheme, the voltage differences between any two electrodes are still less than V_{DD}. The measured voltage gains of the proposed charge pump can be more than 97% for V_{DD} higher than 1.4V, and more than 30% of voltage gain is enhanced in comparison to Racape's charge pump.

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References

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2) E. Racape, and J.-M. Daga, *Proc. of IEEE European Conf. on Solid-State Circuits*, 2005, p. 77.
3) C.-P. Hsu and H. Lin, *Intl. Conf. Solid State Devices and Materials* (*SSDM*), 2008, p. 1002.
4) G. van Steenwijk, K. Hoen, and H. Wallinga, *Proc. of IEEE European Conf. on Solid-State Circuits*, 1993, p. 118.

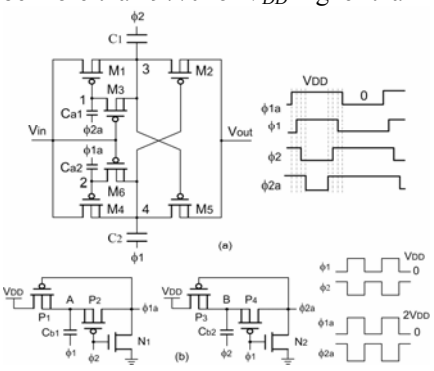

Fig. 1 (a) One-stage Racape's charge pump as described in ref. 2 (b) Proposed clock scheme.

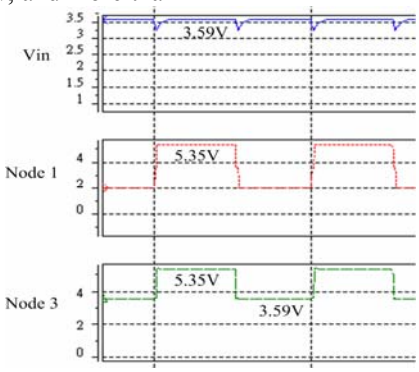

Fig. 2 Simulated waveforms in the second stage of the proposed charge pump.

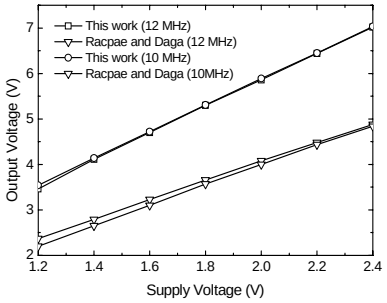

Fig. 3 Simulated boosted voltages of the two-stage charge pumps with I_{out} = 0 for various frequencies and supply voltages.

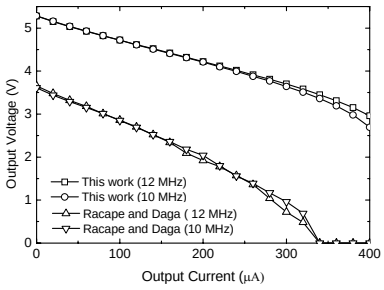

Fig. 4 Comparison of simulated boosted voltages of the two-stage charge pumps for different loading currents with V_{DD} = 1.8V

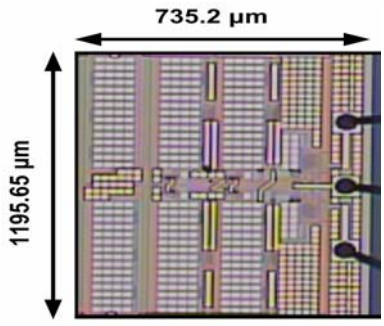

Fig. 5 Microphotograph of the proposed two-stage PMOS charge pumping circuit.

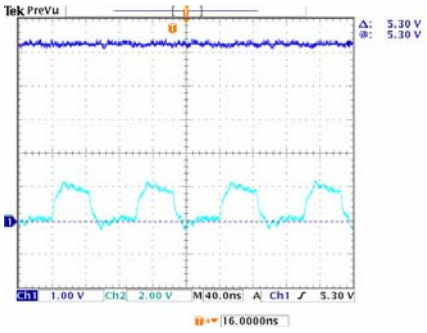

Fig. 6 Measured waveforms of the proposed PMOS charge pump with I_{out} = 0 at a frequency of 10 MHz and V_{DD} = 1.8V.

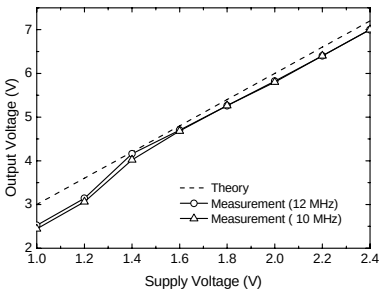

Fig. 7 Measured boosted voltages of the proposed charge pump are very close to the maximal theoretical values for I_{out} = 0.

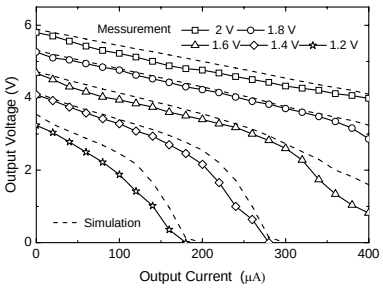

Fig. 8 Comparison of boosted voltages between measurement and simulations for various I_{out} at a frequency of 10MHz.

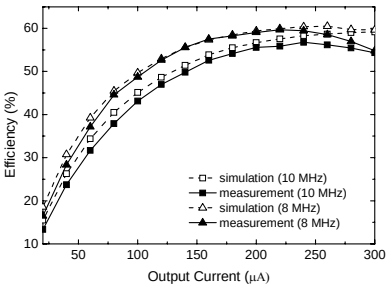

Fig. 9 Comparison of power efficiencies between measurement and simulations for various I_{out} at a supply voltage of 1.8V.