Investigation of Low Cost Consumer Electronic System Using 1066-Mb/s DDR2 Interface Design

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Abstract

Low cost is always the favorite feature of consumer electronics. The purpose of this paper is to study the possibility of low-cost design for DDR2-1066 memory interface. The S-parameters simulations of the PCB, DDR2 controller and SDRAM packages were performed using the electromagnetic field solvers up to 3 GHz. Those broadband S-parameters were integrated with the chip SPICE models in the SPICE simulator for transient analyses. The results indicated that DDR2 command and control routing topology with zero series termination on the PCB and the controller using Level-7 drive strength encapsulated in the 2-layer PBGA package achieved 915-ps eye-aperture time, 507-ps signal skew, 2.14-V overshoot, and -0.37-V undershoot.

1. Introduction

As the multimedia products have been rapidly pushed to increase their functions, such as today digital LCD-TV, that requires higher data bandwidth to process the de-interlacing, noise reduction, H.264, MPEG4,…etc. in real time. The data rate of DDR2 memory has been raised from 800 Mb/s to 1066 Mb/s to satisfy the consumer electronics with high data bandwidth requirements without the eager request for the next generation of high cost memory interface, such as DDR3 SDRAM. From the system cost point of view, using the wirebonding BGA package rather than the flip-chip BGA package, the 2-layer BGA package rather than the 4-layer BGA package, less routing area and components on the PCB, and cheap components, such as DDR2 SDRAM, can enhance the product competitiveness, but the system performance must be maintained. Some papers have been proposed on the DDR2 topology design or component optimization for power saving or cost reduction [1]-[4]. However, their applications are up to 800 Mb/s only. The purpose of this paper is to investigate if the low-cost system design could conform to 1066 Mb/s DDR2 memory requirements. In this study, the transmission channel model is based on the S-parameters extracted from the BGA packages and PCB and is analyzed in frequency domain. Next, the channel S-parameters are integrated with the chip SPICE models and simulated using HSPICE with different damping resistors and drive strengths. Finally, the optimized command and control routing topology without any damping resistor and termination voltage is achieved for DDR2 1066 Mb/s applications.

2. DDR2 routing topology

There are two types of command and control routing topology. Fig. 1(a) shows DDR2 parallel terminated memory topology with R_T and V_{TT} (termination voltage, 0.9V). Fig. 1(b) shows DDR2 series terminated memory topology. Routing the DDR2 command and control signals with series termination can achieve less layout area, power saving and cost saving for the de-coupling capacitors and termination regulator, such as LP2996 [5]. According to those benefits, the routing topology with the series termination with R_d is investigated if the DDR2 command and control performance can meet DDR2-1066 requirements.

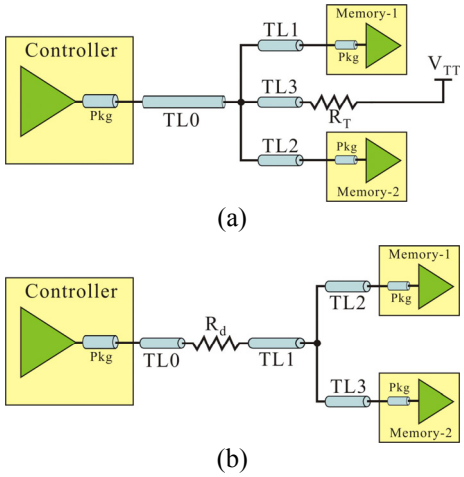

Figure 1. DDR2 command and control routing topology for two ranks of x16 SDRAMs in the 4-layer PCB. (a) Single parallel termination with R_T and V_{TT}. (b) Series termination with R_d.

3. Transmission channel model

The DDR2 SDRAM is encapsulated with a JEDEC standard package, a FBGA84 package [6]. The Ansoft

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HFSS was used to extract the S-parameters of FBGA84 packages with 34 lumped ports including the power net. A multimedia SoC fabricated by TSMC 65nm with the DDR2 memory controller is encapsulated with the conventional PBGA package. The two and four layers of PBGA package were evaluated for their system performance. Ansoft SIwave was used to extract the S-parameters of the 4-layer PCB integrated with the DDR2 controller in the PBGA package including the power delivery network (DDRV) as illustrated in Fig. 2. The DDRV net is supplied by a 1.8 V low dropout (LDO) regulator in the PCB. Fifty-six de-coupling capacitors, from 0.01 to 470 µF, were added between the DDRV net and ground. Their corresponding simulation configuration is listed in Table 1. Those parameters were cascaded in Ansoft Designer for calculating the final S-parameters with 51 lumped ports as illustrated in Fig. 3.

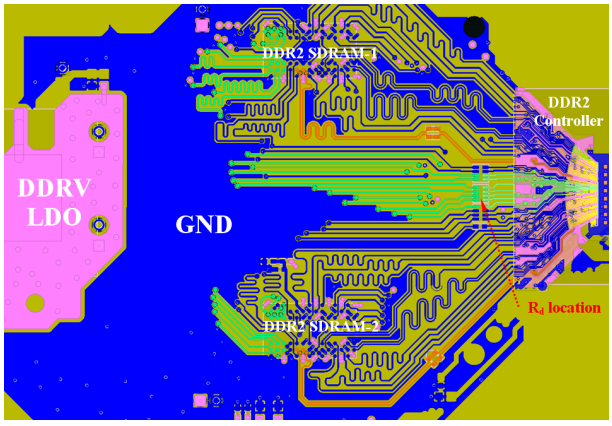


Figure 2. Modeling of the address lines (green) and power/ground nets for the controller package and 4-layerL PCB in SIwave.

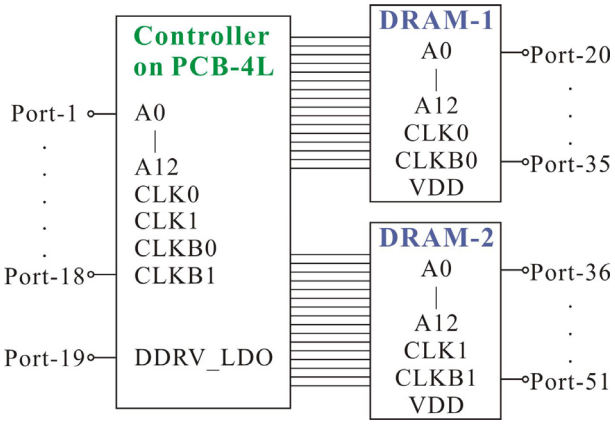


Figure 3. Transmission channel model with cascaded S-parameters for the controller PBGA package, 4-layer PCB, and DDR2 SDRAM package.

Table 1. Configuration of chip, package, and PCB

Controller Package	Package type/size/ball pitch	PBGA/31 mm x 31 mm/1 mm
	Substrate via/Wire diam.	0.2 mm / 0.9 mil
	Package stack-up: PP1/Core/PP2 thickness	4-L: 50/300/50 µm; 2-L: 0/450/0 µm
	Trace thick./width/space	4-L: 22/50 /60 µm; 2-L: 25/50 /60 µm
	Dielectric properties (D_k/D_f)	BT: 4.2/0.012, Mask: 4.1/0.031, Mold: 3.7/0.005
DDR2 SDRAM	Package type/Size	FBGA84 (1-layer)/12.5 mm x 10 mm
	Memory size	16M x 16
	Trace thick./width/space	10 µm/40 µm/40 µm
	Wire diameter/Ball pitch	0.8 mil/0.8 mm
	Core substrate/Bottom mold thickness, D_k/D_f	Substrate: 200 µm, D_k/D_f = 4.7/0.014 Mold: 0.15 mm, D_k/D_f = 4.1/0.01
	SPICE model	u48b (Micron)
PCB	Layers/Trace width, space	4/5, ≥15-mil
	Mask/Copper thickness	0.4/1.34 mils
	PCB stack-up	4.5 (PP1)/47 (Core)/4.5 (PP2) mils
	Dielectric properties	Core: D_k/D_f = 4.4/0.02 Mask: D_k/D_f = 3.4/0.03

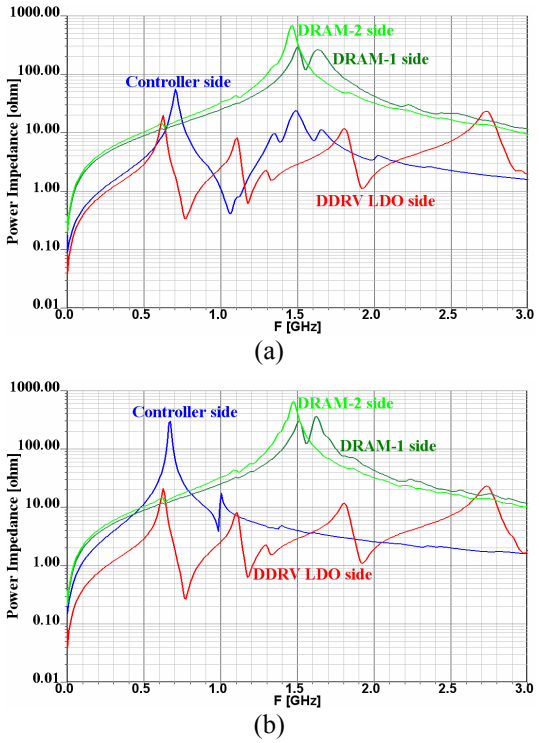


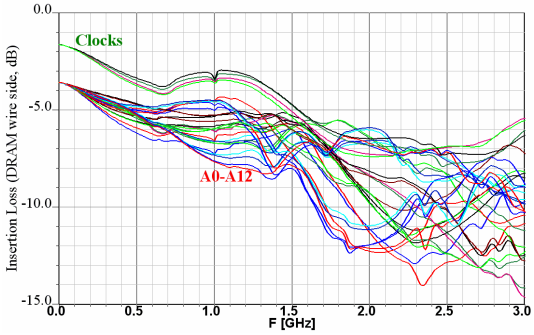
Figure 4. Power (DDRV) impedance of DDR2 transmission channel model. (a) 4-layer PBGA, and (b) 2-layer PBGA packages.

4. Performance analysis in frequency domain

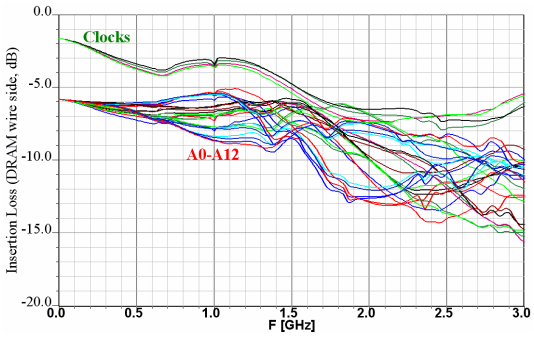
High-speed digital signals are broadband in frequency domain. S-parameters are usually used for the accurate system simulation. Furthermore, the power delivery network (PDN) modeling also affects the accurate timing and voltage margins in time domain. The simulated power impedances of DDR2 transmission channel model are shown in Fig. 4. Since additional power and ground

layers were added in the 4-layer PBGA package which contains a decoupling capacitor, the power impedance at the controller wire side of 4-layer PBGA package is less than that of 2-layer PBGA package. Less signal skew and larger eye open can be expected.

Fig. 5 shows the channel insertion loss for the 2-layer PBGA package. We can observe that the larger the damping resistor (R_d) is, the larger the signal insertion loss is. Thus, the overshoot and undershoot caused by the reflective waveforms will be degraded. Note that the differential clocks are directly terminated by a 100 Ω resistor near the DRAM side. Therefore, the channel insertion loss is about -1.5 dB for each clock pair at DC.



(a)



(b)

Figure 5. Insertion loss of DDR2 transmission channel model with 2-layer PBGA package. (a) R_d = 0 Ω, and (b) R_d = 22 Ω.

5. Performance analysis in time domain

The system channel S-parameters, the DDR2 controller SPICE model, and the DDR2 SDRAM encrypted SPICE mode [7] were integrated in the HSPICE for transient analysis from 10 ns to 320 ns. The Level-12 drive strength and full driving were assigned for the DDR2 controller and the SDRAM, respectively. The input pattern (voltage high or low, 1.876-ns bit time) for each address input buffer is random. The different controller package types, 2-layer and 4-layer PBGA packages, with different R_d, 0, 10, 22, and 50 Ω, were simulated. Fig. 6 shows the simulated eye-diagrams overlaid with all address signals, A0-A12. Their measured timing and voltages are summarized in Table 2. Note that x/y denotes the value in DRAM-1/DRAM-2. The system channel with the 4-layer PGBA package suffers less signal skew and has larger eye open (or aperture time) except with R_d = 50 Ω. Since the damping resistor (R_d) can effectively attenuate the reflective waveforms, less overshoot and less undershoot can be achieved. However, overmuch R_d, such as 50 Ω, may induce negative effects including larger signal skew and smaller eye open. That is due to overmuch damping resistor also degrading the signal amplitude excessively. If the damping resistors should be removed, i.e. R_d = 0 Ω, for further cost saving and less routing area, one can adjust the controller driving strength with a weaker level to achieve better timing and voltage margins. Table 3 lists the eye diagram measurement of 2-layer PBGA package with different drive strengths. The weak driving strength achieves less overshoot and undershoot, but suffers the smaller eye open. Because the maximum peak amplitude allowed for overshoot and undershoot is 0.5V [6], the controller drive strength with Level-7 in the 2-layer PBGA package is recommended for the final system verification.

Table 2. Eye diagram measurement for different R_d with fixed controller drive strength (Level-12).

PKG Type	R_d (Ω)	Aperture Time (ps)	Max. Skew (ps)	Max. Over-shoot (V)	Max. Under-shoot (V)
PBGA-2L	0	975/969	786/793	2.44/2.45	-0.78/-0.78
	10	950/935	701/745	2.25/2.24	-0.59/-0.58
	22	927/929	596/592	2.14/2.14	-0.38/-0.37
	50	603/602	915/903	2.01/2.01	-0.22/-0.20
PBGA-4L	0	1350/1340	351/343	2.24/2.24	-0.47/-0.45
	10	1200/1220	359/341	2.13/2.13	-0.36/-0.35
	22	911/948	399/374	2.07/2.07	-0.27/-0.26
	50	511/503	968/970	1.99/1.97	-0.16/-0.17

Table 3. Eye diagram measurement of 2-layer PBGA package and R_d = 0 Ω with different drive strengths.

Driving Level	Aperture Time (ps)	Max. Skew (ps)	Max. Over-shoot (V)	Max. Under-shoot (V)
6	899/903	534/554	2.09/2.09	-0.28/-0.26
7	915/933	506/507	2.14/2.13	-0.37/-0.36
8	948/941	492/486	2.18/2.18	-0.46/-0.46
12	975/969	786/793	2.44/2.45	-0.78/-0.78

6. Conclusion

Design of DDR2 memory interface in the consumer electronic system using series termination without termination voltage is demonstrated. Co-simulation of chip-package-board models with channel S-parameters was done in frequency and time domains to analyze system performance. The chip drive strength can reduce overshoot and undershoot caused by impedance mismatch. Since not all damping resistors can achieve less signal skew and larger eye open, we suggest that

using co-simulation to determine the damping resistance first, and then fine-tune the chip drive strength for the better timing and voltage margins.

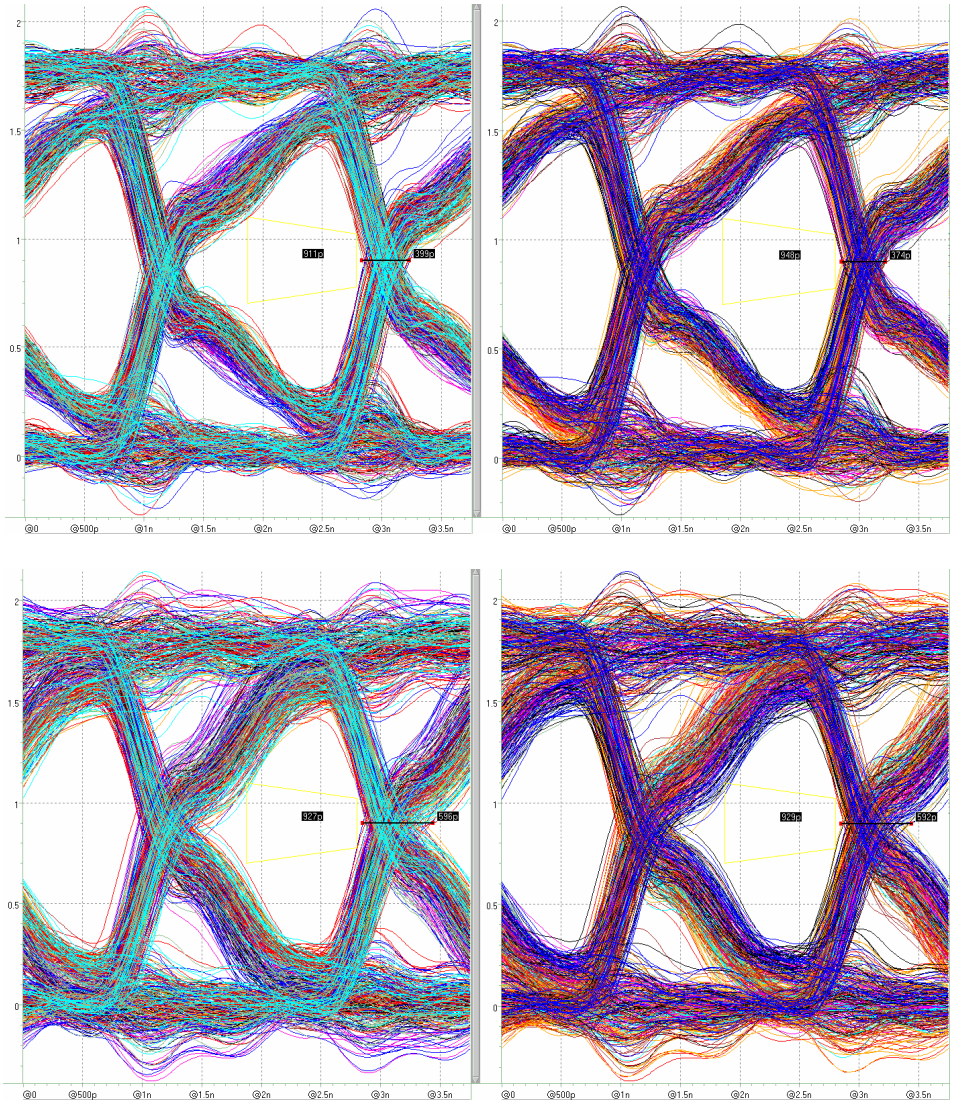


Figure 6. Simulated eye-diagrams overlaid with all address signals and R_d = 22 Ω using (a) 4-layer PBGA, and (b) 2-layer PBGA packages. Note that the left figure is for DRAM-1 and another is for DRAM-2.

Acknowledgments

The authors would like to acknowledge Chip Implementation Center (CIC) of National Applied Research Laboratories (NARL) of Taiwan for the support in chip design. This work was supported by National Science Council of Taiwan (NSC 96-2221-E-005-091 and NSC 96-2220-E-005-005).

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