Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 1002-1003

F-7-2

A PMOS Charge Pump for Low Supply Voltages

Chien-pin Hsu and Hongchin Lin

Dept. of Electrical Engineering, National Chung-Hsing University, Taichung, Taiwan
Phone: 886-4-284-0688 ext. 250 e-mail: hclin@dragon.nchu.edu.tw

1. Introduction

Charge pump circuits have been extensively adopted in flash memories, EEPROM and LCD displays to generate voltages that are higher than the supply voltage or lower than ground voltage. The most popular schemes are based on the Dickson structure using NMOS transistors [1]. However, the threshold voltage and body effect degrades the performance of the Dickson charge pump when the number of stages is increased.

Many charge pumps, such as four-phase charge pumps [2], voltage doublers [3] in Fig. 1, as well as the recent PMOS based charge pump [4] in Fig. 2, can minimize the influence due to threshold voltages. However, the current drivability at lower supply voltages may be degraded. In addition, except the last one, these circuits require more guard ring area due to triple-well CMOS technology. Therefore, if only PMOS transistors are used for the positive charge pumps, N-wells are very easy to be isolated using smaller guard ring area. Even twin-well processes can also be appropriate for implementation.

Unlike Racape's pump [4], which requires a four-phase clock generator and six PMOS transistors per stage, the proposed pump only needs four PMOS transistors per stage with two-phase clocks using simple auxiliary transistors.

2. The Proposed PMOS Charge Pump

The proposed PMOS charge pump circuit and the clock waveform are shown in Figs. 3(a) and (b). The circuit has two pumping branches, the top branch and bottom branches, to transfer charges to the output (V_{out}), alternatively. The first stage is from V_{DD} to node A/E. The body electrodes are tied to node A or E for the top or the bottom branch, respectively. The second to fourth stages are from A/E to B/F, B/F to C/G, C/G to D/H. The output stage of the proposed charge pump contains two cross connected transistors, M_{o1} and M_{o2}.

The two auxiliary clocks δ_1 and δ_2 can be easily generated from clocks ϕ_1 and ϕ_2 as shown in Fig. 3(b). When ϕ_1 is low and ϕ_2 is high during time t_1, transistor M_{a2} is turned off and M_{a1} and M_{b1} are on. Therefore, δ_1 goes to low and charge is transferred from V_{DD} to node 1. Then, ϕ_2 goes low at time t_2, M_{b1} and M_{a1} are off, but M_{a2} is on to make δ_1 rise to $V_{DD} - \Delta V$ due to node 1. At the time interval t_3, ϕ_1 switches to high. M_{a1} and M_{b1} are still off, and M_{a2} is on, so δ_1 jumps from $V_{DD} - \Delta V$ to $2(V_{DD} - \Delta V)$. The operation of t_4 is similar to that of t_2. The operation of clock δ_2 is similar to that of clock δ_1 with 180° phase difference. Note that the time intervals t_2 and t_4 are much smaller than the clock cycle. Fig. 3(b) is not scaled for t_2 and t_4.

3. Simulation and Measurement Results

The three four-stage charge pumps were simulated using 0.18μm CMOS technology. These charge pumps were designed using the same pumping capacitance, clock frequency, and the optimized transistor size for the maximum output voltages. The pumping capacitances and the output capacitance are 5pF and 10pF, respectively.

Figure 4 depicts the simulated output voltages for different output loading currents and supply voltages at a frequency of 10MHz. The output voltages are decreased almost linearly when the output currents are increased. These agree with the theoretical expected values.

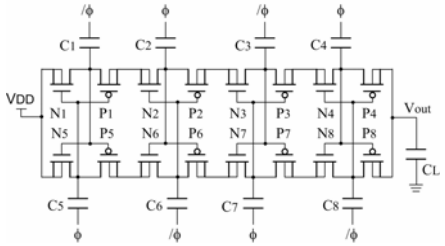

Fig. 1 Four-stage voltage doublers circuit in Ref. [3]

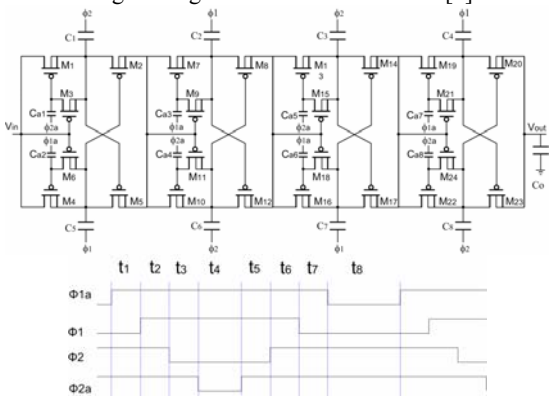

Fig. 2 Four-stage Racape's charge pump circuit in Ref. [4]

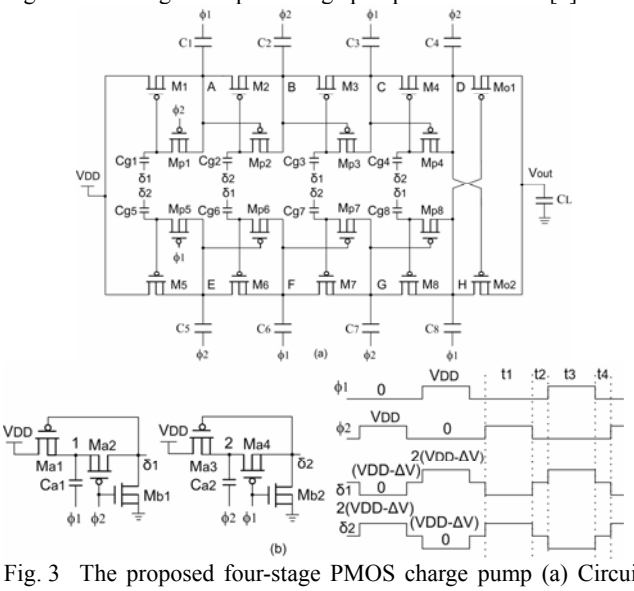

Fig. 3 The proposed four-stage PMOS charge pump (a) Circuit diagram (b) Clock patterns and the waveform generator

Figure 5 compares the performance of voltage doubler Racape's and our proposed charge pumps at a frequency of 10MHz with different loading currents and two supply voltages. In general, the proposed charge pump has higher output voltages than the other two charge pumps, since the proposed pump has higher overdrive voltages. That indicates the proposed charge pump can be operated at lower supply voltages.

Figure 6 shows the microphotograph of the test chip with area about 0.205mm^2. The 5pF MIM type pumping capacitors were selected for implementation. The gate boost capacitor and output capacitor were selected as 0.5pF and 10pF, respectively. The simulated and measured output voltages of the proposed charge pump for different supply voltages without loading current are shown in Fig. 7. The measured results are a little lower than the simulation results. It may be due to parasitic effects of pad capacitance and the packages. Figure 8 illustrates the simulated and measured outputs of the proposed charge pump for different current loading conditions at a supply voltage of 1.8V. The measured results are agreed well with the simulated results.

4. Conclusions

A two-phase PMOS charge pump is proposed and was implemented using standard 0.18μm CMOS process. The simulated and measured output voltages of the proposed charge pump are around 8.6V and 8.28V without loading current for V_{DD} = 1.8V and a frequency of 10MHz. The results show that the proposed four-stage charge pump has excellent loading current drivability and more than 90% of voltage gain even at low supply voltage of 1.0V.

Acknowledgements --- The authors would like to acknowledge Chip Implementation Center (CIC) of National Applied Research Laboratories (NARL) of Taiwan for the support in chip fabrication. This work was supported by National Science Council of Taiwan (NSC 96-2221-E-005-091 and NSC 96-2220-E-005-005).

References

[1] J. F. Dickson, *IEEE J. Solid-State Circuits*, vol.1, p. 374-378 (1976)

[2] H. Lin, and N. H. Chen, *Proc. of IEEE Int. Symp. on Circuits and Systems*, pp. 504-507 (2001)

[3] M.-D. Ker, S.-L. Chen, and C.-S. Tasi, *IEEE J. Solid-State Circuits*, vol. 41, pp. 1100-1107 (2006)

[4] E. Racape, and J.-M. Daga, *Proc. of IEEE European Conf. on Solid-State Circuits,* pp. 77-80 (2005)

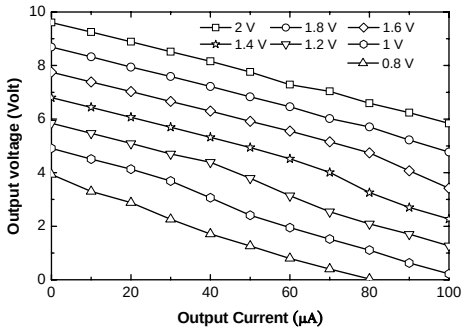

Fig. 4 Simulated output voltages of the proposed 4-stage charge pump for different loading currents and supply voltages

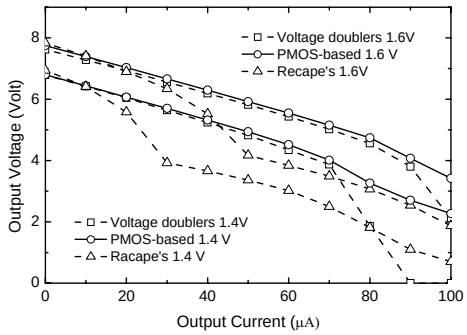

Fig. 5 Comparison of simulated output voltages of voltage doublers, Racape's, and the proposed four-stage charge pumps for different loading currents and supply voltages

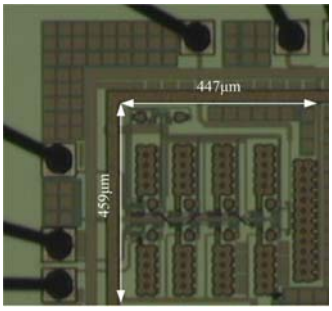

Fig. 6 Microphotograph of the proposed four-stage PMOS-based charge pump circuit

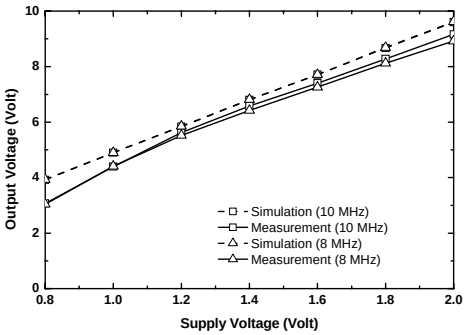

Fig. 7 Comparison of simulated and measured output voltages of the proposed four-stage PMOS charge pump at various supply voltages without load at 8MHz and 10MHz

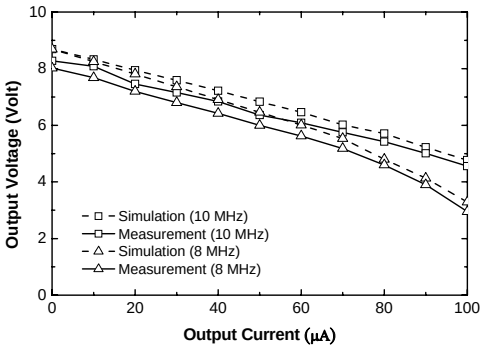

Fig. 8 Comparison of simulated and measured output voltages of the proposed four-stage PMOS charge pump for various loading currents at V_{DD} = 1.8V with 8MHz and 10MH