Design of Costless and Adjustable Inductors Embedded in Array Packages

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***Abstract* – High performance, costless and tunable embedded inductors for applications in system-in-package design are proposed. Square segmented spiral inductors in the chip pad area of the standard two-layer array packages provide multiple selections of adjustable inductances without penalty of signal routing density. The inductor performance was extracted using 3D electromagnetic field solvers and wideband circuit optimization. A 4 mm^2 spiral inductor can be achieved for inductance selection from 1nH through 12 nH. In this range, an inductor of 7.6 nH with maximum Q-factor 37 can be obtained and its performance is comparable to that of LTCC or MCM-D.**

***Index Terms* –** BGA, adjustable inductor, LTCC, MCM-D, Q-factor, insertion loss.

I. Introduction

The rapid growth of wireless communication applications, such as mobile phones, global positioning systems (GPS), wireless local networks (WLAN), increases the demands for low-cost, high-performance, multi-function, and compact radio-frequency front-end components. Integrating the passive components in the package not only realizes the compact structure, but also meets the low-cost requirement. Among the passive components, the inductor is the most investigated one because of its important role in the performance of RF/microwave circuits, such as voltage-controlled oscillators, filters, high-impedance RF chokes, and impedance matching networks [1]. Inductors integrated in the currently typical silicon processes will be difficult and costly to meet the high performance specifications for the future RF ICs, but high-quality inductors can be easily achieved using the system-in-package (SiP) approach such as low temperature co-fired ceramics (LTCC) or multi-chip module deposition (MCM-D) [2]. However, LTCC and MCM-D are the higher cost packages compared with the popular ball grid array (BGA) or land grid array (LGA) packages. Therefore, the BGA package with inductor structure is proposed.

Traditionally, the chip pad area in most array packages is used to assign the power or ground planes. In this paper, a novel design of segmented spiral inductor occupied a small portion of chip pad area in the conventional two-layer array packages is proposed as shown in Fig. 1. It would not affect the signal routing density and has no additional fabrication cost. A 1-mil thickness of conductive silver epoxy is added under the chip that makes a grounded layer to prevent the EM wave generated by the spiral inductor to influence the chip performance. The electrical analysis indicates the proposed method can realize an adjustable inductance with high Q-factor that meets the requirements of low-cost and high-performance at the same time.

Even though many studies were proposed to analyze the inductor performance [3] – [5], little investigation about the wideband equivalent circuit model was provided for the embedded inductors. In this paper, a wideband equivalent circuit model of the embedded spiral inductor to be employed in SPICE simulation was extracted using the 3D full-wave EM solver and circuit optimization.

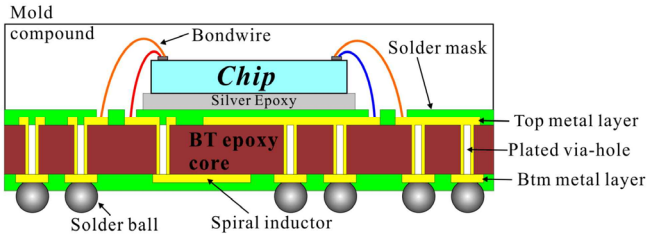

Fig. 1. Cross-sectional view of a spiral inductor embedded in a two-layer ball grid array package.

II. Inductor Design

Three types of spiral inductors with different trace widths of 50, 100, and 200 μm were designed on the bottom layer of the BGA packages. There are four turns with a constant trace pitch (width plus space) of 250 μm as illustrated in Fig. 2. The parameters of package and inductor are listed in Table I. D_k and D_f represent the dielectric constant and the loss tangent, respectively. The main body of segmented spiral inductor was laid out on the bottom layer of 2-layer package and surrounded by the ground ring as shown in Fig. 2(d). Eight plated via-holes are used to connect the connection traces on the top layer and the corresponding segmented inductors on the bottom layer. The 50-μm connection traces are selectable using wirebonding for different inductances. Those traces beneath the chip are connected using the shortest bondwires or multi-bondwires to minimize goldwires' inductance. Fig. 3 shows an example of a selectable inductance with two bondwires connecting two outer loops, Loop 1 and Loop 2. The spiral inductor designed in the chip pad area would not affect the signal layout density. The wire bonding between the selected connection traces is a part of wire bonding process of standard process of BGA packages, thus, the cost can be neglected.

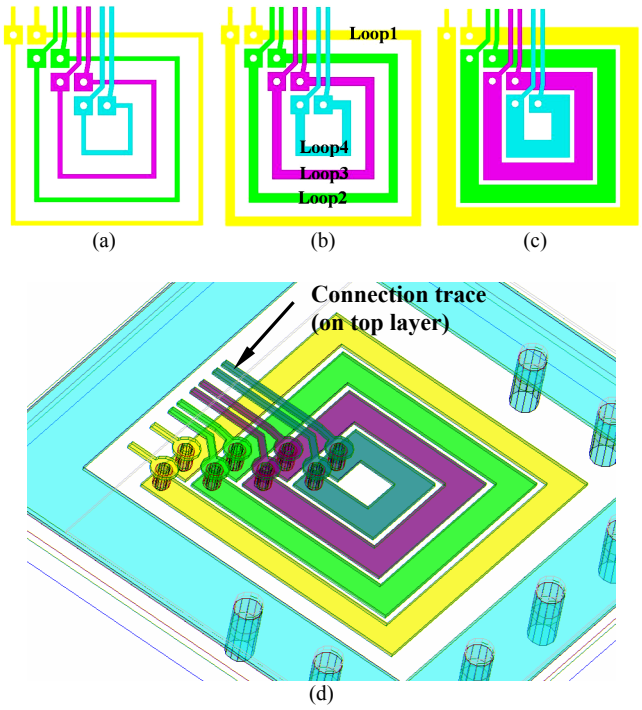

Fig. 2. Top view of spiral inductors with width (a) 50 µm (w50s200), (b) 100 µm (w100s150), (c) 200 µm (w200s50), and (d) 3D view of a segmented spiral inductor surrounded by the ground ring.

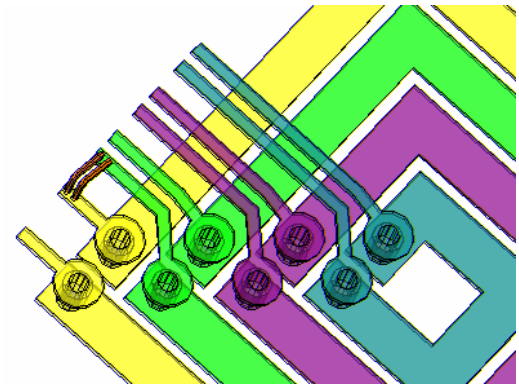

Fig. 3. An adjustable inductance with bondwires connected between Loop1 and Loop2.

TABLE I
PARAMETERS OF PACKAGE AND INDUCTOR

Item	Description
Package type / layers	BGA / 2
Spiral inductor: width/space (thickness)	50/200, 100/150, 200/50 µm (27 µm)
Spiral inductor size	2 mm × 2 mm
Mold thickness	0.53 mm (D_k = 3.8, D_f = 0.007)
Solder-mask thickness	40 µm (D_k = 4.1, D_f = 0.031)
BT core thickness	150 µm (D_k = 4.2, D_f = 0.012)
Via-hole dia./thickness	100/20 µm

III. ELECTRICAL ANALYSIS

A. *Extraction of Inductor Parasitics*

Ansoft Maxwell 3-D Quick Parameter Extractor was used to extract inductor parasitics for the three inductors. The location of ideal ground is 0.254 mm below the package. Table II summarizes parasitic parameters of the segmented inductors for different inductor types, where R_{ac} was computed at 100 MHz and L_{ac} and L_m are computed at high frequency. There are many combinations of loops to be selected for each type of inductor depending on applications. For the example of w100s150, inductance is ranging from about 1 nH through 12 nH with connection of one through four loops of segmented inductors. A 7.78 nH is achieved if Loop 1 is wire bonded to Loop 2 of inductor w100s150.

TABLE II
PARASITIC PARAMETERS EXTRACTED FROM DIFFERENT INDUCTOR TYPES

Type	Loop no.	R_{ac} (Ω)	L_{ac} (nH)	L_m (nH)	C_s (pF)
w50s200 (50 µm width)	Loop1	0.17	4.422	0.694	0.724
	Loop2	0.15	3.311	0.396	0.689
	Loop3	0.12	2.263	0.150	0.602
	Loop4	0.08	1.272	N/A	0.485
w100s150 (100 µm width)	Loop1	0.13	3.669	0.682	0.841
	Loop2	0.12	2.747	0.389	0.798
	Loop3	0.10	1.903	0.145	0.671
	Loop4	0.08	1.115	N/A	0.512
w200s50 (200 µm width)	Loop1	0.11	2.719	0.753	1.194
	Loop2	0.10	1.995	0.415	1.227
	Loop3	0.08	1.417	0.154	0.948
	Loop4	0.07	0.926	N/A	0.617

B. *Inductor Performance*

In order to calculate the effective inductance and quality factor of spiral inductors, Ansoft HFSS was utilized to extract their two-port S-parameters up to 6 GHz based on the package geometries and materials given in Table I. An ideal ground location is also 0.254 mm below the package. The S-parameters were then transformed into Y-parameters from which the inductance (L_{eff}) and Q factor can be calculated based on the following equations [6], respectively.

$$L_{eff} = \mathrm{Im}(1/Y_{11})/2\pi f$$

$$Q = \mathrm{Im}(1/Y_{11})/\mathrm{Re}(1/Y_{11})$$

where f is the signal frequency. The performance comparison of spiral inductor with different trace widths and connection types are shown in Figs. 4 and 5. Their corresponding inductance, maximum Q-factor, and self-resonance frequency (SRF) are summarized in Table III (Loop 1+2) and Table IV (Loop 1+2+3+4). Connecting all segmented loops gives larger inductance, but the Q-factor and the SRF are degraded. From Figs. 4 and 5, the inductor with less insertion loss indicates the better Q-factor and the higher SRF. This phenomenon is also

observed for w100s150 with different connections of segmented loops as shown in Fig. 6.

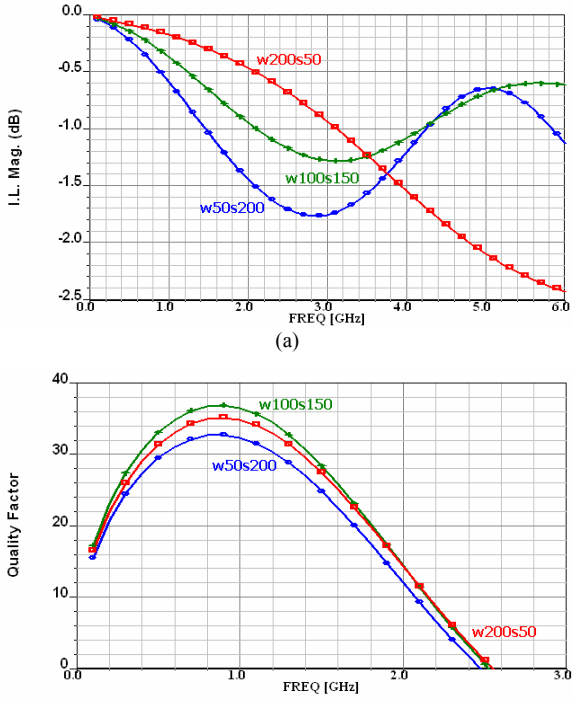

Fig. 4. Insertion loss (a) and quality factor (b) for inductors with Loop1 in series with Loop2 for w50s200 (blue), w100s150 (green), and w200s50 (red).

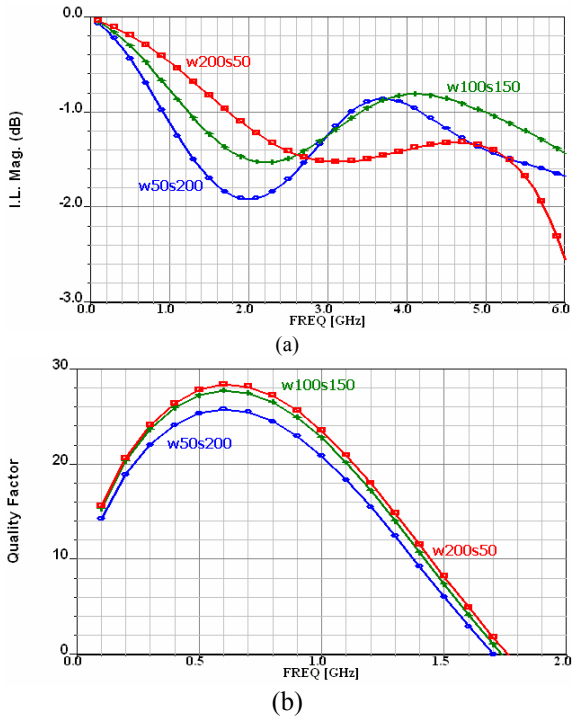

Fig. 5. Insertion loss (a) and quality factor (b) for inductors with all segmented loops connected for w50s200 (blue), w100s150 (green), and w200s50 (red).

TABLE III
INDUCTOR PERFORMANCE OF LOOP1+2

Inductor Type	L_{eff}		Q_{max}		SRF
	(nH)	(GHz)	value	(GHz)	(GHz)
w50s200	9.45	0.9	33	0.9	2.4
w100s150	8.04	0.9	37	0.9	2.5
w200s50	6.26	0.9	35	0.9	2.5

TABLE IV
INDUCTOR PERFORMANCE OF LOOP1+2+3+4

Inductor Type	L_{eff}		Q_{max}		SRF
	(nH)	(GHz)	value	(GHz)	(GHz)
w50s200	14.64	0.6	26	0.6	1.7
w100s150	12.65	0.6	28	0.6	> 1.7
w200s50	10.55	0.6	28	0.6	> 1.7

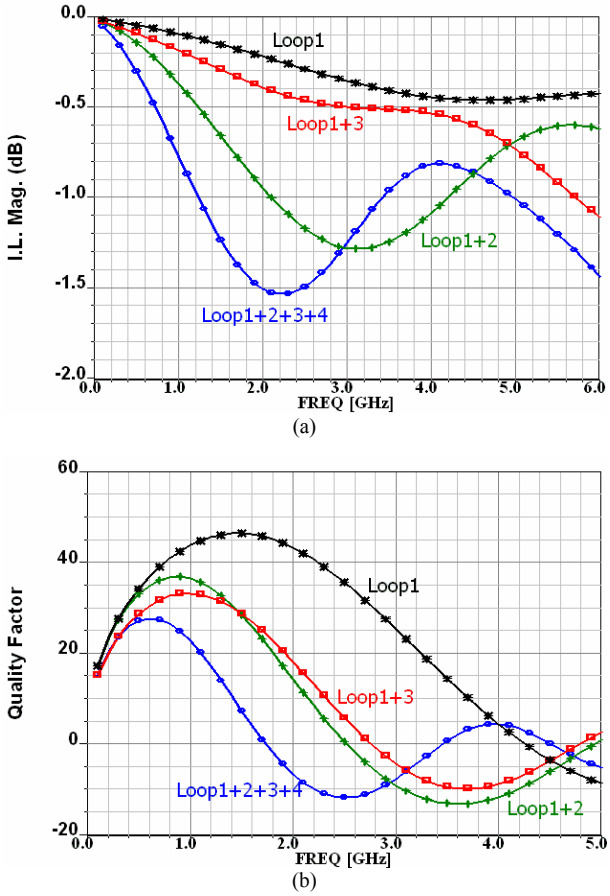

Fig. 6. Insertion loss (a) and quality factor (b) for inductors of w100s150 with Loop1 (black), Loop1+2+3+4 (blue), Loop1+2 (green), and Loop 1+3 (red).

C. *Wideband Equivalent Circuit Model*

The spiral inductor had better to be modeled as a distributed structure, but the model can be reduced to a lumped one for frequencies lower than the first self-resonance frequency [2]. The simple lumped model with fixed component values over the wideband up to the self-resonance frequency is useful for SPICE simulation. In order to have the better agreement, two sections of π-model cascaded in series, shown in Fig. 7, were

utilized for circuit optimization. Ansoft Harmonica and the two-port S-parameters of w100s150 with different loop connections were used to optimize those component values specified in Fig. 7. The initial component values assigned for circuit optimization were extracted from Sub-section A in Section III. The final optimized values are summarized in Table V. The optimized lumped inductance for Loop 1, Loop 1+3, Loop 1+2, and Loop 1+2+3+4 is 3.46, 5.56, 7.22, and 11.24 nH, respectively. They are slightly less than those inductances calculated from the equations defined in Sub-section B in Section III. From Fig. 6 and Table V, the larger product of the series inductance (L_S) and the capacitance to ground (C_1+C_2) gives a lower SRF, while the lower series resistance (R_S) and the capacitance to ground produce a better Q-factor. The lower R_S also results in a lower insertion loss. The impedances (Z_0) of Loop 1 and Loop 1+3 calculated from $\sqrt{L_S/(C_1+C_2)}$ are about 62 Ω, which is close to 50 Ω, and thus, have the lower insertion loss and the better Q-factor.

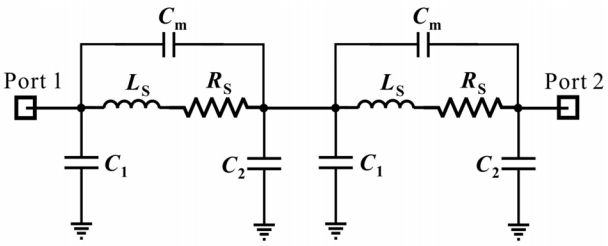

Fig. 7. Wideband equivalent circuit model of spiral inductor.

TABLE V
SUMMARY OF OPTIMIZED COMPONENT VALUES ON ONE SECTION OF π-MODEL

Connection type	Bandwidth (GHz)	L_S (nH)	R_S (Ω)	C_1 (pF)	C_2 (pF)	C_m (pF)	Z_0 (Ω)
Loop 1	4.2	1.73	0.05	0.22	0.23	0.000	62.2
Loop 1+3	2.8	2.78	0.16	0.32	0.41	0.001	61.6
Loop 1+2	2.5	3.61	0.17	0.31	0.33	0.004	74.7
Loop 1+2+3+4	1.7	5.62	0.28	0.40	0.56	0.011	76.3

The inductor coil width is the most significant layout parameter to achieve maximum quality factor [3]. The minimum trace width for conventional BGA substrate is about 45μm, which is quite wider than that of LTCC or MCM-D. However, the performance of the proposed design is still comparable to that of LTCC or MCM-D. For example, Loop 1+2 (w100s150) in Table V with 7.22 nH and Q-factor 37 (shown in Table III) is comparable to Type 3-D, N = 2, Ls = 7.6 nH, Qmax = 36 for LTCC-based inductors in Table 10.6 of Ref. [2] and "split 3", N = 2.5, Ls = 2.5 nH, Qmax = 25 for inductors using MCM-D layers post-processed on top of chip passivation in Figure 10.31 of Ref. [2]

IV. CONCLUSIONS

The spiral inductor embedded in the conventional two-layer array package that makes use of the chip pad area was presented in this paper. Selectable and tunable inductances with high Q-factors were also demonstrated without penalty of signal layout density. The differences of the inductances extracted from the 3D electromagnetic field solvers and the wideband circuit optimization are very small. The self-resonance frequency may be improved using lower dielectric constant materials and lower loss tangent of the solder mask.

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