Electrical Design and Manufacturing Evaluation for Multiple Exposed Pads (M-pad) Leadframe Package

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Abstract

The technology trend in the consumer electronics can be summarized as more functionalities in a smaller geometry with low cost. The conventional exposed pad low-profile quad flat pack (E-pad LQFP) is a low cost solution for multimedia chips, but its disadvantages are limited pin count and worse electrical characteristics. In order to increase their pin utilization rate and electrical characteristics for high-speed applications, an innovative leadframe package, named multiple exposed pads (M-pad) LQFP, is proposed. The M-pad LQFP package utilizing the two-stage etching methodology would not change the standard manufacturing processes of leadframe packages significantly in both the leadframe supplier and the assembly house. The parasitics of power net and S-parameters of high-speed differential signals were extracted using 3D electromagnetic field solvers. The simulated power parasitics of M-pad LQFP is much lower than those of E-pad LQFP and BGA packages. The simulated differential S-parameters of M-pad LQFP also show less signal loss compared with those of E-pad LQFP. By bonding all power and ground wires to their dedicated exposed pads, the leads which are originally bonded to the corresponding power and ground wires can be used as the spared leads for the other signals, or they can be just removed to reduce the lead numbers and thus the size and cost of the M-pad leadframe package.

Introduction

Since the first working integrated circuit (IC) was invented in 1958 [1], the leadframe packages have been served as the IC encapsulation for almost a half century. The leadframe packages are always treated as a low-level application due to their limited pin count and worse electrical characteristics. After the exposed pad (E-pad) leadframe packages were developed, the exposed die-pad can serve as a grounding pad where all the digital and analog ground pads on the chip can be bonded onto the exposed die-pad. Therefore, the leads that are originally bonded to the respective digital and analog ground pads on the chip can be used for the other purposes. However, for some system-on-chips (SoC) with mixed signal designs, the high-speed digital ground noises may adversely affect the analog signal paths. The proposed multiple exposed pads (M-pad) leadframe package that splits the unique exposed pad of conventional E-pad leadframe package into several exposed pads is beneficial for high-speed SoC applications. Since the photochemical machines are popularly used in package assembly of bump chip carrier (BCC), thin array plastic package (TAPP), and non-leaded bump array (NBA) [2]-[4], it makes the two-stage etching methodology possible to fabricate the M-pad leadframe package. In this paper, the manufacturing processes of M-pad leadframe package are evaluated including delamination and mold flush. The 3D electromagnetic field solvers were also used to extract their parasitics and differential S-parameters up to 30 GHz. The analysis shows that the M-pad leadframe package has excellent electrical characteristics that are suitable for high-speed and mixed signaling applications.

Package Structures

The conventional E-pad LQFP package, as shown in Fig. 1, which has only one exposed die-pad for bonding all digital and analog ground wires from the chip. Fig. 2 shows the M-pad structure like the original E-pad split into several independent exposed pads, which are not supported by leads, held by the molding compound after package assembly. Those exposed pads can be designed as different digital/analog power and ground planes, or high-speed signal pads for wire bonding. Fig. 3 illustrates another application for system in package (SiP) that includes two chips and one pair of high-speed differential wires bonded onto their corresponding exposed pads. Due to shorter bondwires, the better electrical characteristics will be expected. Mounting passive components, such as decoupling capacitors, between pads is applicable in the package. Both the E-pad and M-pad LQFP packages are made of copper alloy, such as C7025 or A42, with the same inner/outer lead pitch, lead thickness (0.127 mm), down-set and package thickness, as well as encapsulated with the same molding compound. Since the die-pad size in M-pad leadframe package is still larger than the die size, its thermal characteristics is similar to that of E-pad leadframe package.

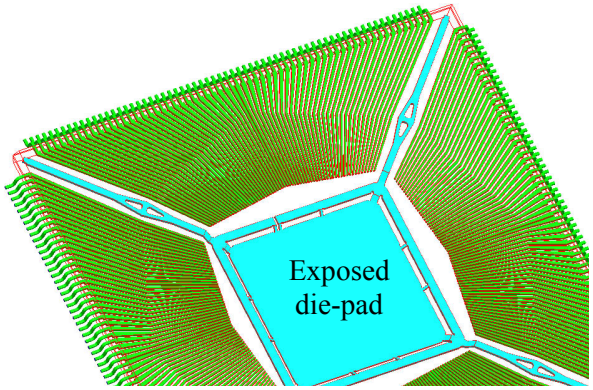
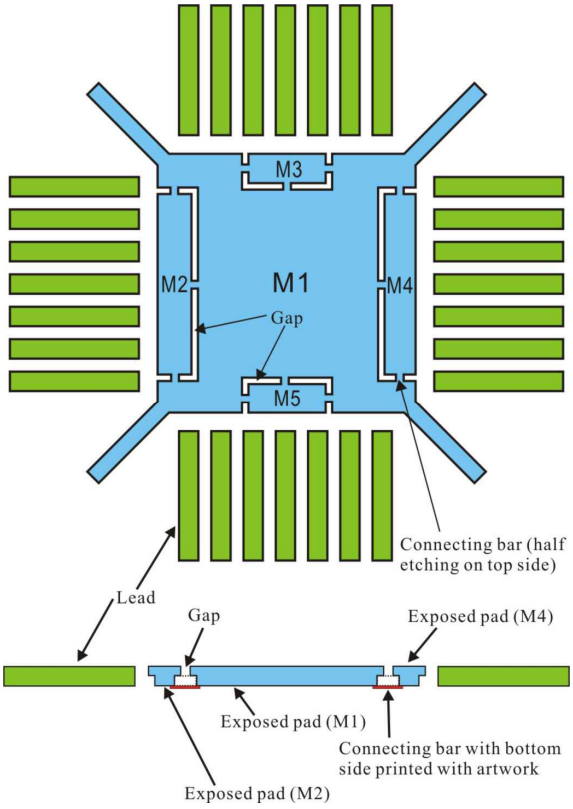
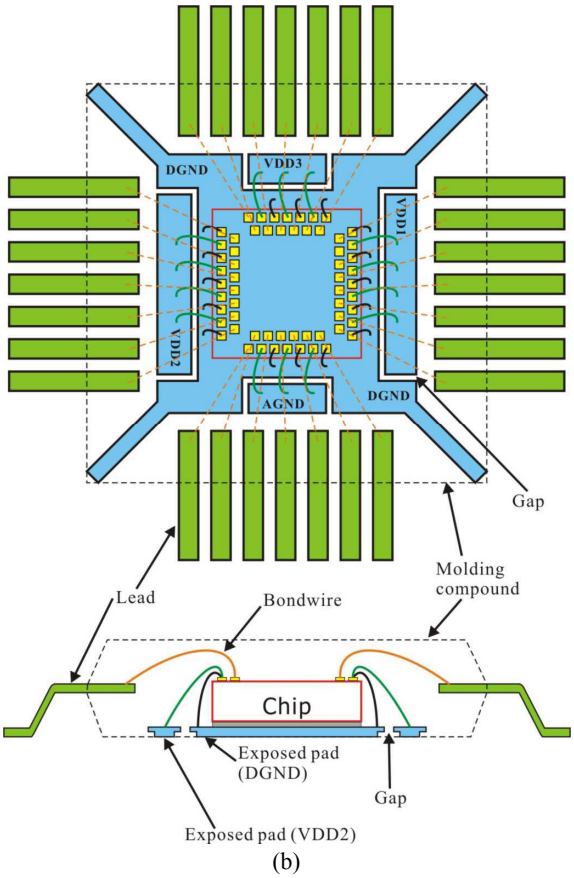


Fig. 1. Conventional E-pad LQFP package with only one exposed die-pad.



(a)



(b)

Fig. 2. M-pad leadframe package top and cross-sectional views (a) before assembly and down-set, (b) after assembly processes.

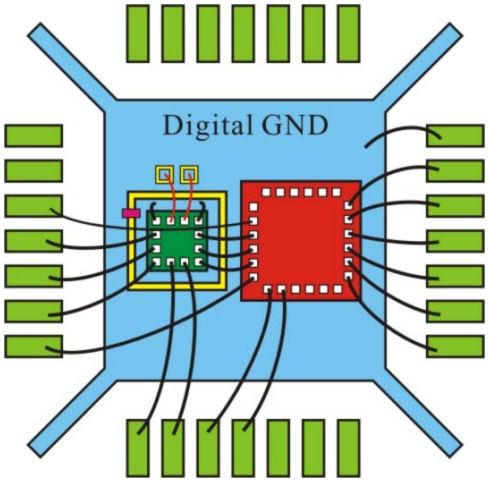


Fig. 3. SiP application using M-pad leadframe package.

Manufacturing Evaluation

The M-pad leadframe can be fabricated with the stamping or etching technologies. However, the etching method is recommended because the half-etching can be adopted to design the reverse T-shaped mold lock, as shown in Fig. 2(b), which can improve the package reliability and delamination. The bottom side of each exposed pad can be etched with a ringed groove which can prevent mold resin bleed-out during package assembly. Fig. 2(a) illustrates that the bottom connecting bars are printed with the artwork or photoresist in the leadframe supplier. The conventional leadframe package assembly process can be used as shown in Fig. 4, until "Solder Plating." After the package is plated with tin (Sn) except the connecting bars, the molded package with exposed leadframe is protected and resistant to corrosion. Then, the artwork or photoresist on the bottom side of connecting bars is removed. The connecting bars (about 2.5 mils thickness) are etched away in the photochemical machine and each exposed pad is electrically isolated. If the process of printing the artwork or photoresist on the bottom side of connecting bars is not carried out in the leadframe supplier, the artwork printing shall be completed before "Solder Plating" in assembly house. Because the most manufacturing processes are the same with those in the leadframe vendor and assembly house, the expected cost would be between the conventional E-pad leadframe and BGA packages.

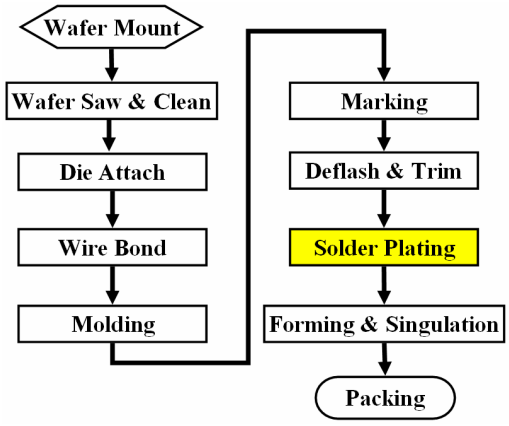


Fig. 4. Conventional assembly process for leadframe package.

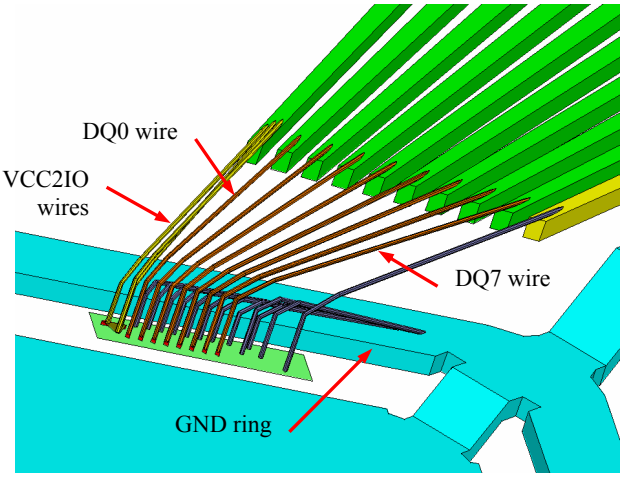
Electrical Design and Simulation

The package behavior is like a low pass filter (LPF) that will filter out high-frequency components of high-speed signals. Lower parasitic inductance and capacitance in the package will relax the LPF effect. The most popular solution to reduce inductance in package is to bond multiple gold-wires for power or ground nets. Fig. 5(a) illustrates an example of a power net (VCC2IO) in the E-pad LQFP256 package with triple gold-wires adjacent to the high-speed signal, DQ0. According to the simulated S-parameters shown in Fig. 5(b), the power net (VCC2IO) couples more noise (about 2 dB) from DQ0 compared to the other signals with single gold-wire. Triple gold-wires reduce the power inductance, but they couples more noise from the adjacent high-speed signals and results in less efficient power delivery. Separating the power net from the high-speed nets can reduce the signal to power coupling. It can be implemented by using the M-pad structure as depicted in Fig. 6. There are 8 leads and 18 gold wires designed for the power delivery system of DDR SDRAM controller in the conventional E-pad LQFP256 package. A larger inductance is expected due to its longer gold-wires and leads compared to the M-pad LQFP with only 18 shorter gold wires bonding onto the dedicated exposed pad without any lead for interconnection. The Ansoft Maxwell 3-D Quick Parameter Extractor was used to extract power parasitics in some packages and the results are summarized in Table 1. The results indicate that M-pad leadframe package has the smallest resistance of 4.08 mΩ and the smallest inductance of 0.165 nH among all of the leadframe and BGA packages except BGA465 package bonding with 65 wires for VCC2 net. With the shortest electrical path, gold-wire length plus 0.127-mm thickness of exposed pad, the M-pad leadframe package achieves very low parasitics. Thus, less IR drop and power impedance can be expected

TABLE I
COMPARISON OF POWER PARASITICS BETWEEN DIFFERENT PACKAGES

Package Type	Layer No.	Net Name	Wire Count	Lead/Ball Count	R_{dc} (mΩ)	L_{dc} (nH)
E-pad LQFP256	N/A	DVDD2	18	8	13.34	3.751
M-pad LQFP256	N/A	DVDD2	18	0	4.08	0.165
BGA388	2	DVDD2	12	5	21.09	4.126
BGA465	4	VCC2IO	65	18	3.36	1.530
BGA680	4	VDD18	36	10	8.18	1.690
BGA680	4	VDD33	45	11	5.21	0.939

S-parameters are helpful for evaluating high-speed signal losses in frequency domain. A less insertion loss is preferred, meanwhile a less return loss and coupling must be preserved. To avoid reflection in the BGA package, a straightforward solution is to reduce the effects of impedance discontinuity including the bonding wires, via-holes, and solder balls [5]. Larger signal loss is always occurred in the LQFP package due to only one metal layer in the package that is hard to control the lead impedance, and thus causes larger reflection and coupling. Fig. 7(a) shows the electrical design for two pairs of differential net including the shorter gold-wires (1.3 to 1.5 mm) bonding onto their corresponding exposed signal pads. Without using the leads for signal transmission in the package, a less reflection and coupling will be expected. The differential traces routed on the top layer of PCB are 15.7-mm long, 1.34-mil thickness, 5-mil width, and 6-mil space. The PCB has four metal layers with 0.4-mil solder-mask thickness and 4.5-mil prepreg (PP) thickness, and their differential impedance is about 93 Ω with the ground layer in the PCB was located 0.15 mm below the package. The S-parameters of the 8-port structure were obtained using Ansoft HFSS up to 30 GHz. The dielectric Dk/Df (dielectric constant/loss tangent) for molding compound, solder mask and FR-4 epoxy in PCB are 4.4/0.01, 3.5/0.03, and 4.4/0.02, respectively. The results indicate that the M-pad leadframe package achieves very low insertion loss, -0.6 dB at 5 GHz and -1.1 dB at 10 GHz. Fig. 7(b) shows no resonance indicating EMI would be less. Fig. 8 demonstrates the comparison of differential S-parameters between M-pad and E-pad LQFP up to 10 GHz based on the same transmission line length. The insertion loss of E-pad LQFP is -2.3 dB at 5 GHz and a resonance is occurred at around 5.2 GHz, where the insertion loss is increased to -3.5 dB.



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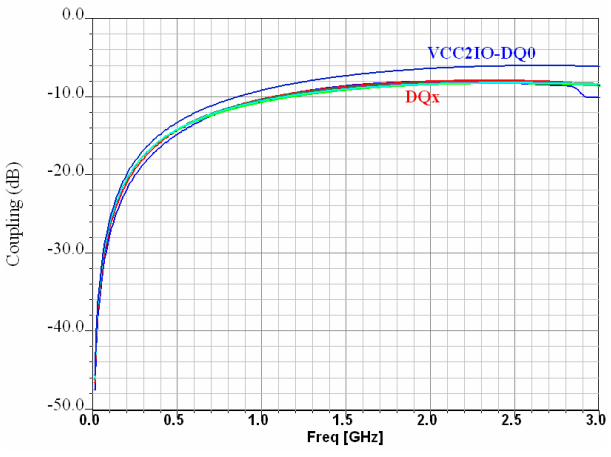
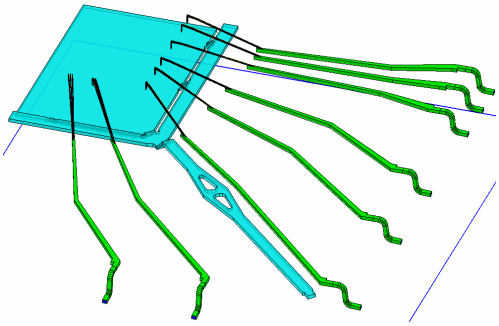


(b)

Fig. 5. E-pad LQFP256 package. (a) 3-D view of wire portion showing triple gold-wires bonding for VCC2IO. (b) Simulated S-parameters for near end coupling at wire side.



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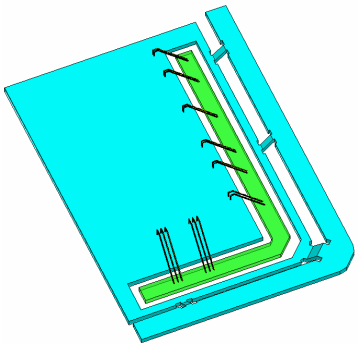
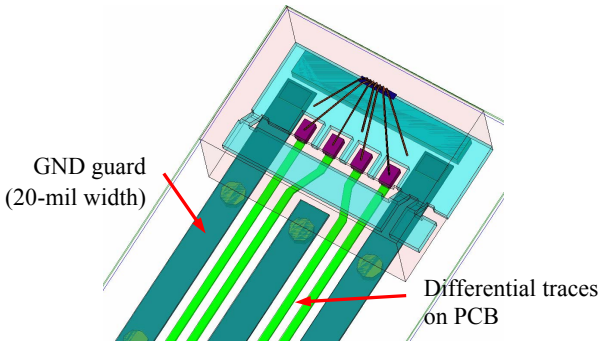


(b)

Fig. 6. Power delivery system for DDR SDRAM in leadframe package. (a) Conventional E-pad LQFP with 8 leads and 18 gold wires, and (b) M-pad LQFP with 18 shorter gold wires and a dedicated exposed power pad.



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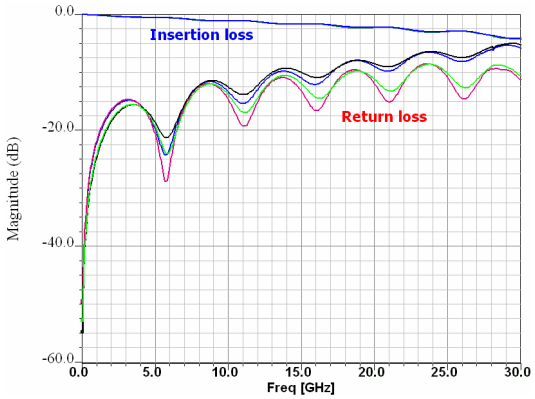

(b)

Fig. 7. Electrical design of high-speed differential pairs in M-pad leadframe package. (a) 3-D view of package plus differential traces surrounded by the ground guards on PCB. (b) Simulated insertion and return loss.

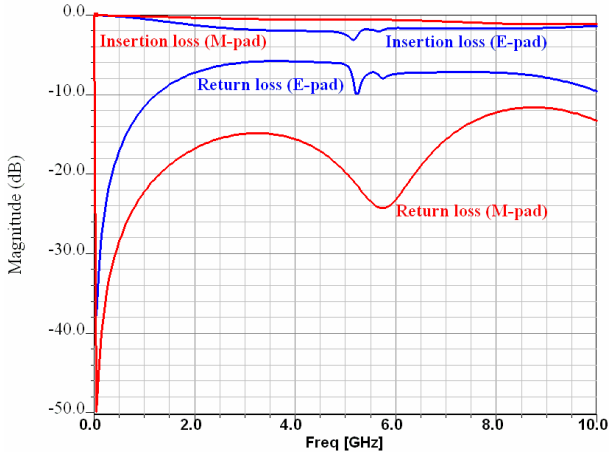

Fig. 8. Simulated differential S-parameters of E-pad LQFP with 5.3-mm trace on the PCB and M-pad LQFP with 15.7-mm trace on the PCB.

Conclusions

The cost effective M-pad leadframe package was evaluated without changing the conventional leadframe manufacturing and assembly processes significantly. Smaller power parasitics and signal loss can be achieved for high-speed applications due to shorter electrical paths in the package. With implementation of the M-pad structure in the leadframe package, it is no longer a low-level package. It could be a versatile package and contributes the consumer electronic market for another half century!

Acknowledgments

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