Analytical Models of Output Voltages and Power Efficiencies for Multistage Charge Pumps

Chien-Pin Hsu and Hongchin Lin

***Abstract*—Accurate analytical models of the output voltage and the power efficiency of voltage doublers and PMOS charge pumps are derived using dynamic charge transfer waveforms and charge balance methods, respectively. Since the on-resistance of switching devices and the parasitic capacitance can be estimated precisely, the proposed models are more accurate than the other existing models. The model-generated values agree well with simulations and measurements for these two charge pumps using 0.18 μm CMOS technology. The expressions for the output voltages prove that the PMOS charge pump can provide more output current without a significant increase in the sizes of transistors. Finally, the design methodology that is based on these models is developed to determine the transistor sizes, capacitance, and number of stages for the maximum power efficiency.**

***Index Terms*—Analytical model, charge pump, design methodology, output voltage, power efficiency.**

I. Introduction

CHARGE pump circuits are widely applied to flash memories and electrically erasable programmable read-only memory (EEPROM) to provide voltages higher than the supply voltage so as to program or erase memory cells. Most of the charge pumps are based on the Dickson structure using MOS transistors as switches [1]. However, the threshold voltage and body effect degrades the performance of the charge pump when the number of stages is raised. Various charge pump topologies [2]–[11] have been proposed to minimize the influence of body effect and threshold voltage. Thus, the voltage gain of these charge pumps can be increased and the output voltages of these circuits are nearly proportional to the number of stages. Four-stage charge pumps, such as the voltage doubler [8] and the PMOS charge pump [11] as illustrated in Figs. 1 and 2, respectively, are two simple high-performance charge pumps that benefit from the bodies of the charge transfer transistors that are connected to their source/drain electrodes.

The output voltage of an N-stage voltage doubler and PMOS charge pumps based on the assumption of zero turn-on resistance of the switching transistors can be expressed as [1]

$$V_{\text{out}} = V_{\text{DD}} + N\left(\frac{C}{C + C_{\text{top}}}\right)V_{\text{DD}} - \frac{NI_o}{2f(C + C_{\text{top}})} \quad (1)$$

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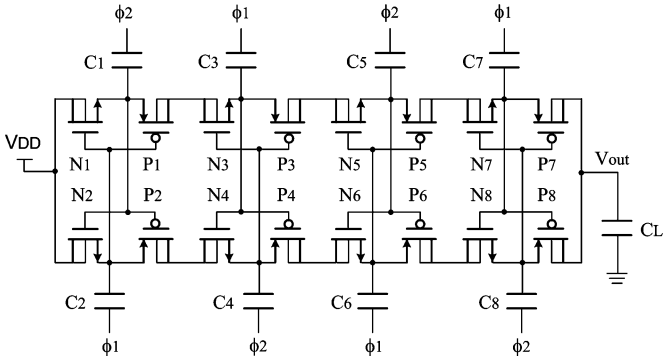
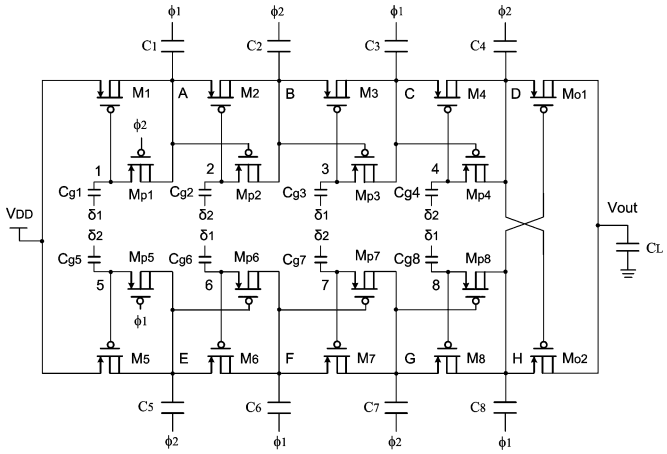
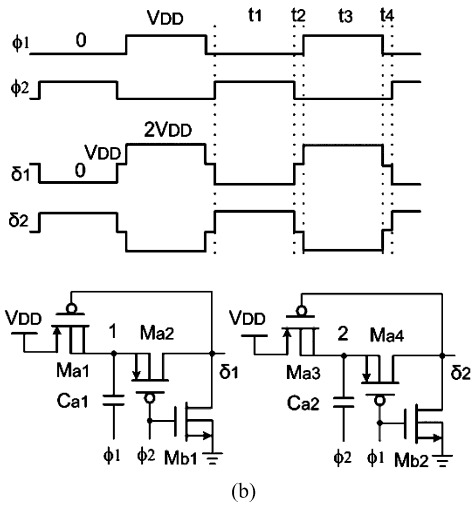


Fig. 1. Four-stage voltage doubler circuit.



(a)



(b)

Fig. 2. Four-stage PMOS charge pump. (a) Circuit diagram. (b) Clock patterns and waveform generators.

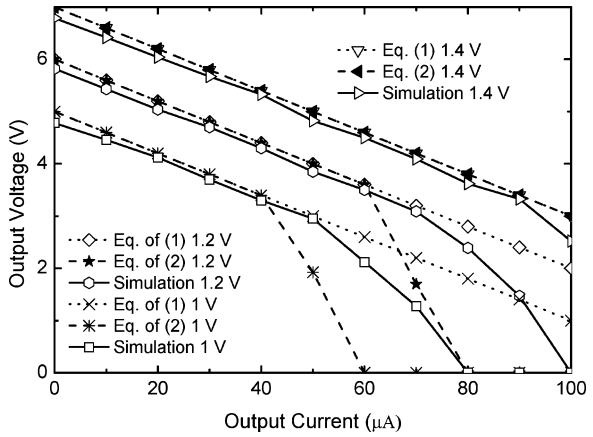


Fig. 3. Comparison between (1), (2), and the simulated results of the four-stage voltage doubler at 10 MHz.

where C is the pumping capacitance, $C_{\rm top}$ is the switch-node parasitic capacitance, $V_{\rm DD}$ is the supply voltage, I_o is the output current, and f is the clock frequency. However, in low voltage or high output current applications, the on-resistance of switching transistors is increased and may not be neglected due to the low $V_{\rm gs}$ of switching transistors. By including the on-resistance in (1), the output voltage has been reported as [3]

$$V_{\rm out} = V_{\rm DD} + N\left(\frac{C}{C+C_{\rm top}}\right)V_{\rm DD} - \frac{NI_o}{2f(C+C_{\rm top})}\coth\left(\frac{1}{2fR_{\rm ON}C}\right) \quad (2)$$

where $R_{\rm ON} = L/\mu C_{\rm ox}WV_{\rm ov}$ and $V_{\rm ov}$ is the overdrive voltage of the switching transistors that varies dynamically. It may be approximated as $V_{\rm gs} - |V_t| - I_o/2fC$, where $V_{\rm gs}$ is assumed to be the initial $V_{\rm gs}$ when the switch is just turned on. Obviously, accurately determining $V_{\rm ov}$, and thus $R_{\rm ON}$, is difficult. The simulated output voltages of a four-stage voltage doubler versus the output current are plotted in Fig. 3. The output voltages are decreased nonlinearly as the output current is high. In this situation, $R_{\rm ON}$ is nonlinear [12] and may be over- or underestimated, since the switching transistor tends to work in the triode region, but close to the saturation region. Hence, $V_{\rm out}$ cannot be precisely predicted by (1) and (2).

Recently, Hu and Chang [13] proposed an output voltage model by the charge transfer waveforms for charge-pump gain-increase circuits. The authors assumed zero on-resistance of the charge transfer transistors. However, as supply voltages trend lower or loading current trends higher, the development of output voltage models that consider the more accurate on-resistance of transistors becomes important. Moreover, the charge transfer voltage waveforms of various charge pumps are different due to the various gate bias conditions. This implies that (2) cannot accurately estimate the output voltage. In this investigation, output voltage models for the voltage doubler [8] and the PMOS charge pump [11] are formulated based on the voltage waveforms of each pumping stage. The aspect ratio of the switching transistors in both charge pumps can be set to optimize the design.

Similar to the transistor sizes, the power efficiency of charge pumps has become an important issue in recent years due to the low power requirement. Two methods for analyzing the power efficiency are available. One is energy conservation [3] and the other one is charge balance [14]. In the energy-conservation approach, the energy that is provided by the power supply equals the energy that is delivered to the load plus the energy loss. In the charge-balance method, the charge that is transferred from the previous stage is the same as that transferred to the next stage. The power efficiency can be improved either by increasing the output voltage to increase the output power, or by using silicon on insulator (SOI) process to reduce power loss [15]. Much effort has been made in the analysis and optimization of the power efficiency of Dickson charge pump and voltage doubler [14]–[16]. In this paper, the power efficiency models for the voltage doubler and the PMOS charge pumps are derived by considering more parasitic capacitance effects.

The proposed models were verified by simulation and measurements using 0.18 μm CMOS technology. An optimization of the design methodology employing these models for the PMOS charge pump is also presented. A similar design strategy can also be applied to the voltage doubler or the other charge pumps.

The rest of this paper is organized as follows. The output voltage models for the voltage doubler and the proposed PMOS charge pumps are derived in Section II. Section III presents power efficiency models for both charge pumps. Section IV demonstrates the agreements between models, simulation, and measurements. On the basis of the output voltage and the power efficiency models, an optimized design strategy is presented in Section V. Conclusions are finally drawn in Section VI.

II. Analytical Models of Output Voltages

Before formulation of the output voltages, the operations of the proposed PMOS charge pump [11] are briefly introduced. The four-stage PMOS charge pump and its clock waveforms are shown in Fig. 2(a) and (b), respectively. The circuit has two pumping branches, the upper branch and the lower branch, which alternately transfer charges to the output ($V_{\rm out}$). In Fig. 2(a), we observed each stage of the proposed PMOS charge pump is composed of a pair of pumping capacitors referred as C_i and C_{i+4}, a pair of auxiliary capacitors referred as $C_{\rm gi}$ and $C_{\rm gi+4}$, a pair of PMOS switches referred as M_i and M_{i+4}, and a pair of auxiliary transistors referred as $M_{\rm pi}$ and $M_{\rm pi+4}$. The output stage comprises two cross-connected transistors, M_{o1} and M_{o2}. The pumping capacitors and the auxiliary capacitors are driven by two nonoverlapping clocks, ϕ_1 and ϕ_2, and two auxiliary clocks, δ_1 and δ_2, respectively. According to Fig. 2(b), two auxiliary clocks δ_1 and δ_2 can be easily created from clocks ϕ_1 and ϕ_2. The highest voltages at δ_1 and δ_2 are close to $2V_{\rm DD}$.

During time t_1, clocks ϕ_1 and δ_1 are low, ϕ_2 is high, and δ_2 rises to $2V_{\rm DD}$. Transistors M_1, M_3, M_6, M_8, and M_{o1} are turned on to transfer charges from $V_{\rm DD}$ to C_1, node B to C_3, node E to C_6, node G to C_8, and node D to C_L, respectively. Meanwhile, the auxiliary transistors M_{p2}, M_{p4}, M_{p5}, and M_{p7} are turned on to keep M_2, M_4, M_5, and M_7 OFF. In a very short

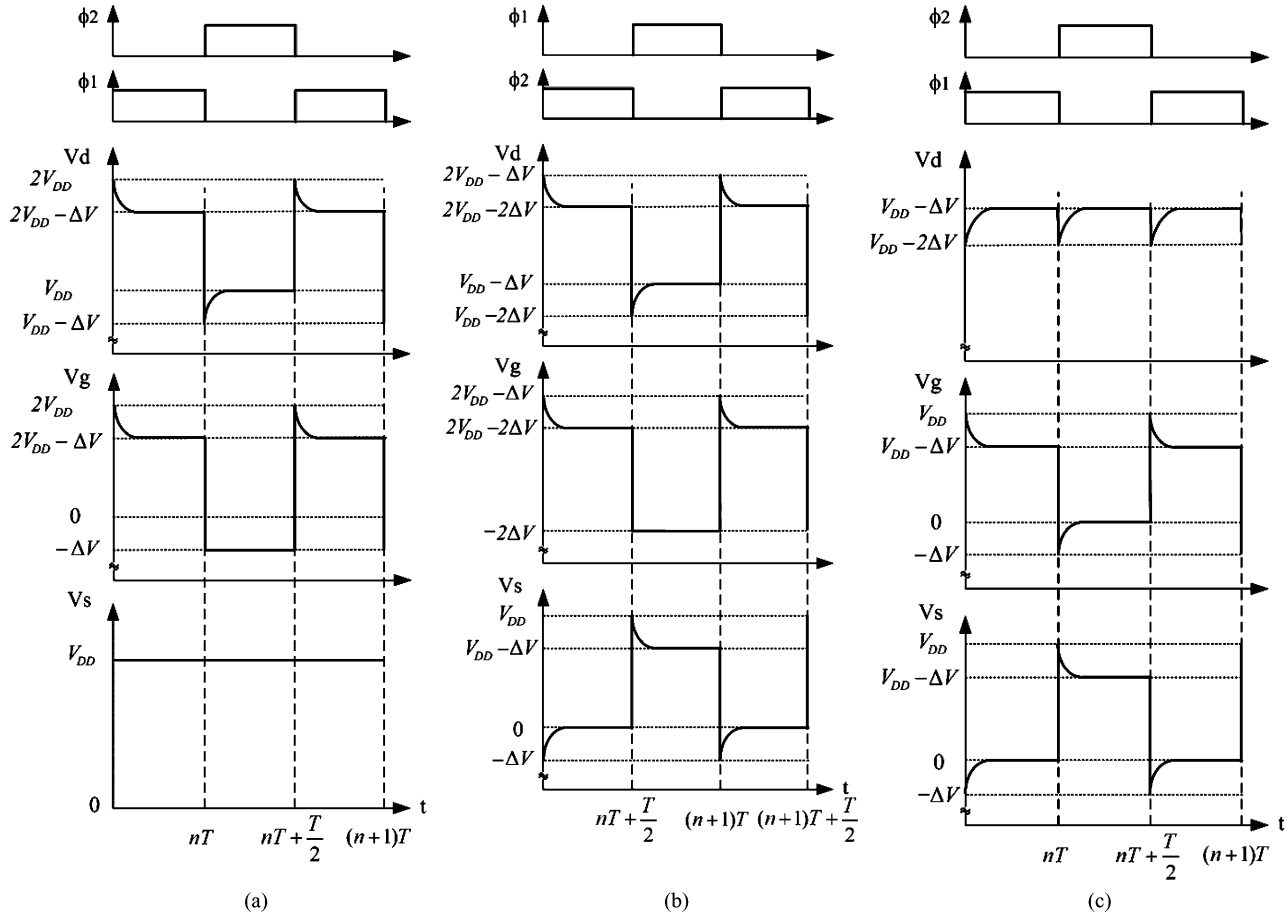


Fig. 4. Node voltage waveforms of the PMOS charge pump for (a) input stage, (b) inner stage, and (c) output stage.

period t_2, according to Fig. 2(b), ϕ_2 drops to zero and δ_2 drops to $V_{\rm DD}$ at the same time, so all transistors M_i are all turned off. The operations in time interval t_3 resemble those in t_1 with the roles of devices interchanged. The operation of time interval t_4 is identical to that of time interval t_2.

To derive the output voltage models, the PMOS charge pump shown in Fig. 2 is divided into the input stage, inner stages, and the output stage according to the charge transfer behaviors. The input stage is from $V_{\rm DD}$ to node A/E, and the first to third inner stages are from A/E to B/F, B/F to C/G, and C/G to D/H, respectively. The output stage comprises two cross-connected transistors, M_{o1} and M_{o2}. The derivation is based on the following assumptions.

1) Compared with the pumping capacitance, the small parasitic capacitance at each pumping node can be neglected.
2) Only one charge transfer branch, the upper or lower one, is considered in derivation of charge transfer characteristics.

A. Voltage Model of Input Stage for the PMOS Charge Pump

The node voltage waveforms of transistor M_1 shown in Fig. 2(a) are shown in Fig. 4(a). Notably, in Fig. 2(b), t_2 and t_4 are much shorter than t_1 and t_3, so t_1 and t_3 are assumed to be equal to one half of one period (T/2) in the following derivation. At time interval $[nT,\ nT + (T/2)]$, clocks ϕ_1 and δ_1 are low, and the charges are transferred from $V_{\rm DD}$ to C_1 and the drain voltage V_d of transistor M_1 is increased from $V_{\rm DD} - \Delta V$ to $V_{\rm DD}$, where $\Delta V = I_o/2fC(C = C_1)$. At the same time, the voltages V_g and V_s are held at constant values of $-\Delta V$ and $V_{\rm DD}$, respectively.

The current that flows through transistor M_1 and the pumping capacitor C_1 can be expressed as follows using the equation for the PMOS transistor in the triode region:

$$I = k_{p3}\left\{\left[(V_s - V_g) - V_{t3}\right](V_s - V_d) - \frac{1}{2}(V_s - V_d)^2\right\} \quad (3)$$

where $k_{p3} = \mu_p C_{\rm ox} W/L$ and V_{t3} are the process parameters including the W/L factor and the absolute value of the threshold voltage of the high-voltage PMOS transistor, respectively.

Substituting $V_s = V_{\rm DD}$ and $V_g = -\Delta V$ into (3) yields

$$\frac{C dV_d}{dt} = \frac{1}{2}k_{p3}(V_{\rm DD} - V_d)(V_{\rm DD} + V_d + 2\Delta V - 2V_{t3}). \quad (4)$$

Integrating (4) with respect to t and varying V_d from $V_{\rm DD} - \Delta V$ to V_d yields the output voltage of the input stage of the PMOS charge pump as follows:

$$V_d = -V_{\rm DD} + 2V_{t3} - 2\Delta V + \frac{2(V_{\rm DD} + \Delta V - V_{t3})}{1 + [\Delta V/(2V_{\rm DD} + \Delta V - 2V_{t3})]e^{-(k_{p3}/C)(V_{\rm DD} + \Delta V - V_{t3})t}}. \quad (5)$$

B. Voltage Model of Inner Stages for the PMOS Charge Pump

The corresponding node voltage waveforms of transistor M_2 shown in Fig. 2(a) are shown in Fig. 4(b). In the time interval $[nT + (T/2), (n+1)T]$, ϕ_2 and δ_2 are low, and the charges stored in C_1 are transferred to C_2 in a very short period. The voltage V_d of transistor M_2 is increased from $V_{\rm DD} - 2\Delta V$ to $V_{\rm DD} - \Delta V$ by charging, and the source voltage V_s is reduced by discharging from $V_{\rm DD}$ to $V_{\rm DD} - \Delta V$. Simultaneously, the voltage V_g falls to $-2\Delta V$ because the clock δ_2 switches to low. From Fig. 4(b), we conclude that since $V_s + V_d = 2V_{\rm DD} - 2\Delta V$, the voltage V_s can be expressed as a function of V_d as

$$V_s = 2V_{\rm DD} - 2\Delta V - V_d. \tag{6}$$

Substituting $V_g = -2\Delta V$ and (6) into (3) yields

$$\frac{CdV_d}{dt} = 2k_{p3}(V_{\rm DD} - \Delta V - V_d)(V_{\rm DD} + \Delta V - V_{t3}). \tag{7}$$

Integrating (7) with respect to t and varying V_d from $V_{\rm DD} - 2\Delta V$ to V_d yields the output voltage V_d of the inner stage of the PMOS charge pump as follows:

$$V_d = V_{\rm DD} - \Delta V(1 + e^{-2(k_{p3}/C)(V_{\rm DD} + \Delta V - V_{t3})t}). \tag{8}$$

C. Voltage Model of Output Stage for the PMOS Charge Pump

The output stage of the proposed charge pump comprises two cross-connected transistors, M_{o1} and M_{o2}, to charge output capacitor C_L alternately. The corresponding node waveforms of transistor M_{o1} shown in Fig. 2(a) are shown in Fig. 4(c). At time $t = nT$, ϕ_2 is high, transistor M_{o1} is turned on and the charge stored in C_4 is transferred to C_L. If the output capacitance C_L is large enough, the output voltage is held at $V_{\rm DD} - \Delta V$. Then, V_d may drop to $V_{\rm DD} - 2\Delta V$ at the end of time $t = nT + (T/2)$ because clock ϕ_2 switches to low. As plotted in Fig. 4(c), the source voltage V_s is reduced from $V_{\rm DD}$ to $V_{\rm DD} - \Delta V$ by discharging, and the gate voltage V_g falls to $-\Delta V$ at the beginning of time $t = nT$. It then rises to 0 V by charging before $t = nT + (T/2)$. Since $V_s + V_d \cong 2V_{\rm DD} - 2\Delta V$ and $V_d - V_g \cong V_{\rm DD} - \Delta V$, both voltages V_g and V_s can be expressed in terms of V_d as follows:

$$V_g = V_d - V_{\rm DD} + \Delta V \tag{9}$$

$$V_s = 2V_{\rm DD} - 2\Delta V - V_d. \tag{10}$$

Substituting (9) and (10) into (3) with k_{p3} and V_{t3} replaced by k_p and V_{tp}, respectively, gives

$$\frac{CdV_d}{dt} = 2k_p(V_{\rm DD} - \Delta V - V_d)(2V_{\rm DD} - 2\Delta V - V_d - V_{tp}). \tag{11}$$

Integrating (11) with respect to t and varying V_d from $V_{\rm DD} - 2\Delta V$ to V_d yields the drain voltage V_d of the output stage of the PMOS charge pump as follows:

$$V_d = (2V_{\rm DD} - 2\Delta V - V_{tp}) - \frac{V_{\rm DD} - \Delta V - V_{tp}}{1 - [\Delta V/(V_{\rm DD} - V_{tp})]e^{-2(V_{\rm DD} - \Delta V - V_{tp})(k_p/C)t}} \tag{12}$$

where $k_p = \mu_p C_{\rm ox} W/L$ and V_{tp} are the process parameters including the W/L factor and the threshold voltage of the low-voltage PMOS transistor, respectively.

An N-stage proposed PMOS charge pump has one input stage, one output stage, and (N–1) inner stages. Adding (5), (12), and $(N-1) \times (8)$ yields a complete expression for the output voltage of the PMOS charge pump as follows:

$$\begin{aligned} V_{\rm outp} &= NV_{\rm DD} + 2V_{t3} - V_{tp} - (N+3)\Delta V \\ &\quad - (N-1)\Delta V e^{-2(k_{p3}/C)(V_{\rm DD} + \Delta V - V_{t3})t} \\ &\quad + \frac{2\,(V_{\rm DD} + \Delta V - V_{t3})}{1 + [\Delta V/(2V_{\rm DD} + \Delta V - 2V_{t3})]e^{-(k_{p3}/C)(V_{\rm DD} + \Delta V - V_{t3})t}} \\ &\quad - \frac{V_{\rm DD} - \Delta V - V_{tp}}{1 - [\Delta V/(V_{\rm DD} - V_{tp})]e^{-2(V_{\rm DD} - \Delta V - V_{tp})(k_p/C)t}}. \end{aligned} \tag{13}$$

For the special case, if $t = T/2$ is very long, then all of the exponential terms approach zero. Substituting $\Delta V = I_o/2fC$ into (13) allows $V_{\rm outp}$ to be simplified to $V_{\rm outp} = (N+1)V_{\rm DD} - \frac{NI_o}{2fC}$, which is the same as (1) with $C_{\rm top} = 0$.

With the similar procedures given before, the voltage models of the input stage, inner stage, and the output stage of voltage doublers are also derived in the Appendix. The output voltage model of an N-stage voltage doublers can be formulated as

$$\begin{aligned} V_{\rm outd} &= \left(2N + \frac{5}{3}\right)V_{\rm DD} - \left(2N + \frac{2}{3}\right)\Delta V - NV_{tp} - \frac{2}{3}V_{tn} \\ &\quad - \frac{(N-1)\,(V_{\rm DD} - \Delta V - V_{tp})}{1 - [\Delta V/(V_{\rm DD} - V_{tp})]e^{-2\left(V_{\rm DD} - \Delta V - V_{tp}\right)(k/C)t}} \\ &\quad - \frac{(2/3)(V_{\rm DD} - \Delta V - V_{tn})}{1 - [3\Delta V/\{2(V_{\rm DD} + (\Delta V/2) - V_{tn})\}]e^{-(V_{\rm DD} - \Delta V - V_{tn})(k_n/C)t}} \\ &\quad - \frac{V_{\rm DD} - \Delta V - V_{tp}}{1 - [\Delta V/(V_{\rm DD} - V_{tp})]e^{-2\left(V_{\rm DD} - \Delta V - V_{tp}\right)\left(t_p/C\right)t}}. \end{aligned} \tag{14}$$

III. Compact Models of Power Efficiencies

The power efficiency of a charge pump can be defined as the output power P_o divided by the input power P_i as

$$\eta = \frac{P_o}{P_i} = \frac{V_{\rm out} I_o}{V_{\rm dd} I_{V_{\rm DD}}} \tag{15}$$

where I_o is the output current and $I_{V_{\rm DD}}$ is the current draw from the power supply. Here, we assume that transistors are ideal switches and use the charge balance method to analyze the power efficiency of the voltage doubler and the PMOS charge pump. Ideal switches are assumed because, from a design perspective, the power efficiency must be maximal when the charge transfer transistors have almost zero on-resistance. Notably, the output voltage models that are derived in Section II are used to determine the transistor sizes to prevent overdesign.

Fig. 5 shows the charges distribution of the four-stage PMOS charge pump at time intervals t_1 and t_2. The charges distribution at t_3 and t_4 are similar to those of t_1 and t_2, respectively. The transistor symbols with black lines indicate that the transistors are ON, while those with gray lines mean that the transistors are OFF. The charges can be transferred only if the transistors are ON. ΔQ indicates the charges transferred to the pumping capacitor

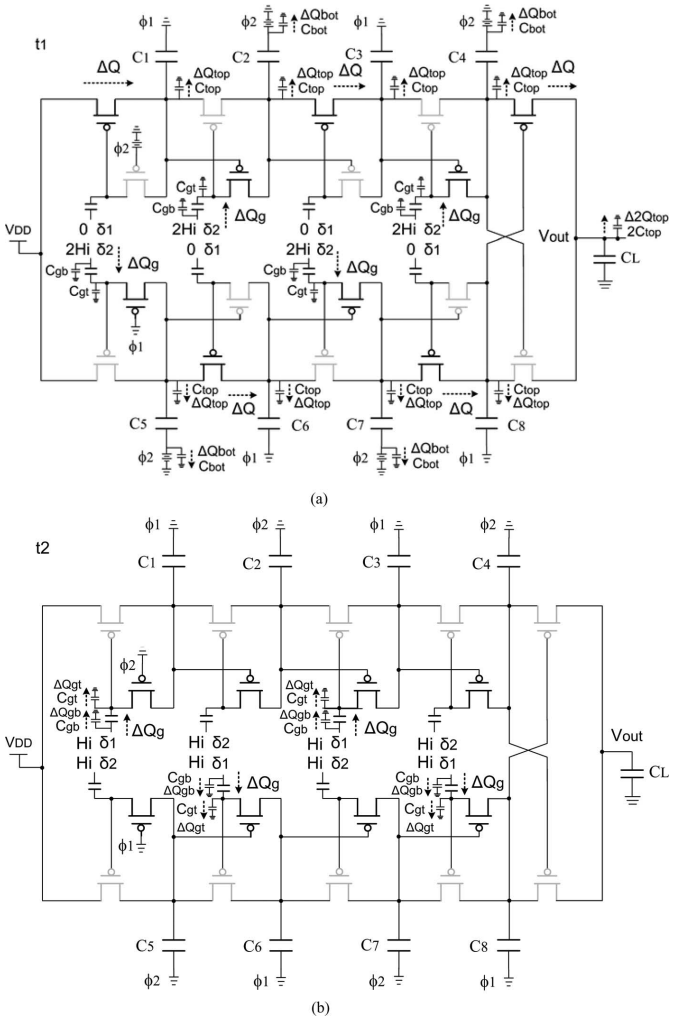


Fig. 5. Illustration of charge transfer for the PMOS charge pump at time (a) t_1 and (b) t_2.

by power supply or clocks during t_1. $\Delta Q_{\rm bot}$ and $\Delta Q_{\rm top}$ labeled in Fig. 5(a) indicate the charge losses because of the bottom-plate and top-plate parasitic capacitances ($C_{\rm bot}$ and $C_{\rm top}$) of the pumping capacitors, respectively. Here, C_L is assumed to be equal to $C_i + C_{i+4}$, so $2\Delta Q_{\rm top}$ is the charge losses due to the top-plate parasitic capacitance at the output node. Similarly, the charge transferred to the auxiliary capacitor (C_g) is ΔQ_g, and the charge losses due to the bottom-plate and the top-plate parasitic capacitors (C_{gb} and C_{gt}) of the auxiliary capacitor are ΔQ_{gb} and ΔQ_{gt}, respectively. All of the switches, except some auxiliary transistors, are OFF in t_2, as revealed in Fig. 5(b). Hence, the charges provided by the power supply and the clocks from t_1 to t_4 can be written as

$$\Delta Q_{t1} = \Delta Q_{t3} = 5\Delta Q + 4\Delta Q_{\rm bot} + 10\Delta Q_{\rm top} + 4\Delta Q_g + 4\Delta Q_{gb} + 4\Delta Q_{gt} \tag{16}$$

$$\Delta Q_{t2} = \Delta Q_{t4} = 4\Delta Q_g + 4\Delta Q_{gb} + 4\Delta Q_{gt}. \tag{17}$$

The total charges provided by the power supply and the clocks in one clock cycle are $\sum \Delta Q_{t\,i}$, where $i = [1, 4]$

$$\Delta Q_t = 10\Delta Q + 8\Delta Q_{\rm bot} + 20\Delta Q_{\rm top} + 16\Delta Q_g + 16\Delta Q_{gb} + 16\Delta Q_{gt}. \tag{18}$$

Since the charge pump has two branches, charges transfer to the output occurs twice in one clock cycle (T). The total current consumption can be obtained from (18) by converting charge into current using a multiplication factor of 1/2 as

$$I_{V_{\rm DD}} = 5I_o + 4I_{\rm bot} + 10I_{\rm top} + 8I_g + 8I_{gb} + 8I_{gt}. \tag{19}$$

This expression can be extended to N stages as follows:

$$I_{V_{\rm DD}} = (N+1)I_o + NI_{\rm bot} + 2(N+1)I_{\rm top} + 2NI_g + 2NI_{gb} + 2NI_{gt}. \tag{20}$$

The currents that charge or discharge the bottom-plate and the top-plate parasitic capacitors have the following relationships [15]:

$$I_{\rm bot} = 2C_{\rm bot}V_{\rm DD}f \tag{21}$$

$$I_{\rm top} = \frac{C_{\rm top}}{C + C_{\rm top}}I_o \tag{22}$$

where $C_{\rm bot}$ denotes the bottom-plate parasitic capacitance of C_i.

Similarly, $I_{gb} = 2C_{gb}V_{\rm DD}f$ and $I_{gt} = I_gC_{gt}/(C_g + C_{gt})$ can be derived for the bottom-plate and the top-plate parasitic capacitances of the auxiliary capacitors C_g, respectively, and I_g indicates the current that charges the auxiliary capacitor.

Substituting (21), (22), I_{gb}, and I_{gt} into (20), the power efficiency η can be expressed as (23), shown at the bottom of this page.

Since the bottom-plate and the top-plate parasitic capacitances $C_{\rm bot}$ and $C_{\rm top}$ are nearly proportional to the pumping capacitance C, the relations of $C_{\rm bot} = \alpha C$ and $C_{\rm top} = \beta C$ are adopted. Similarly, C_{gb} and C_{gt} are also fractions of the auxiliary capacitance C_g, so that $C_{gb} = \alpha_g C_g$ and $C_{gt} = \beta_g C_g$. Moreover, since the pumping capacitance is more than an order of magnitude larger than the auxiliary capacitance, $C_g = \gamma C$ can be assumed, and thus, $I_g \cong \gamma I_o$. Therefore, (23) can be recast as (24), shown at the bottom of this page.

$$\eta = \frac{V_{\rm DD} + [1/(1+\beta)](V_{\rm outp} - V_{\rm DD})}{V_{\rm DD}\left[(N+1) + (2NC_{\rm bot}V_{\rm DD}f/I_o) + [2(N+1)C_{\rm top}/(C + C_{\rm top})] + 2N(I_g/I_o) + 4N(C_{gb}V_{\rm DD}f/I_o) + 2N[I_gC_{gt}/(C_g + C_{gt})I_o]\right]}. \tag{23}$$

$$\eta = \frac{V_{\rm DD} + [1/(1+\beta)](V_{\rm outp} - V_{\rm DD})}{V_{\rm DD}\left[(N+1) + (2N\alpha CV_{\rm DD}f/I_o) + [2(N+1)\beta/(1+\beta)] + 2N\gamma + 4N(\alpha_g C\gamma V_{\rm DD}f/I_o) + 2N\{\gamma\beta_g/(1+\beta_g)\}\right]}. \tag{24}$$

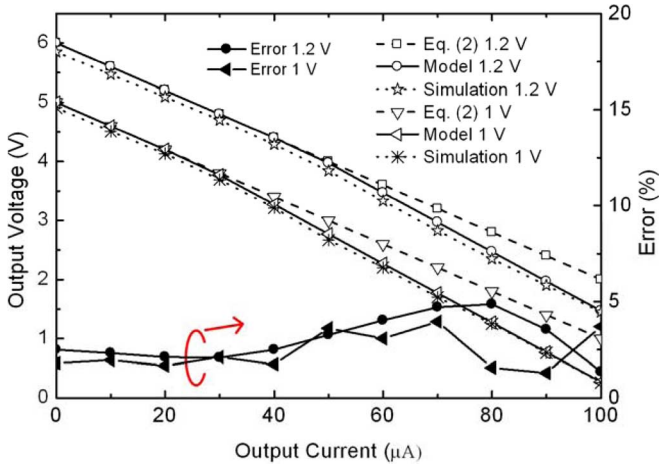


Fig. 6. Comparison of output voltages between (2), the proposed model and simulation for the four-stage PMOS charge pump with $f = 10$ MHz.

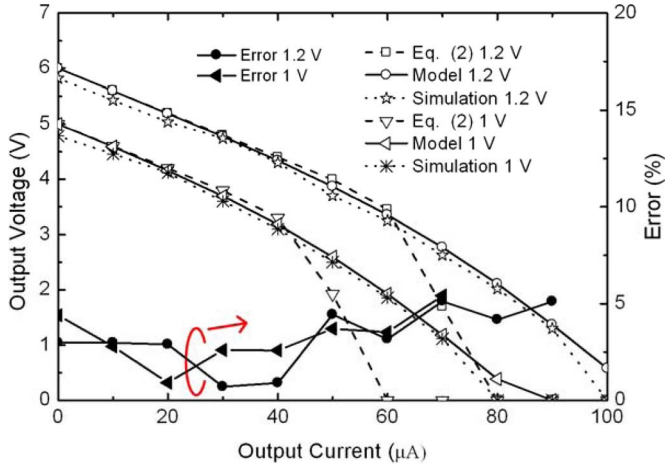


Fig. 7. Comparison of output voltages between (2), the proposed model and simulation for the four-stage voltage doubler with $f = 10$ MHz.

With the similar procedure given before, the power efficiency for the voltage doubler can also be derived as

$$\eta_d = \frac{V_{\mathrm{DD}} + [1/(1+\beta)](V_{\mathrm{outd}} - V_{\mathrm{DD}})}{V_{\mathrm{DD}}\left[(N+1) + \{2N\alpha C V_{\mathrm{DD}} f / I_o\} + \{2(N+1)\beta/(1+\beta)\}\right]}. \tag{25}$$

IV. Simulation and Measurement Results

To verify the accuracy of the proposed output voltage models, the four-stage voltage doubler and the proposed PMOS charge pumps were designed using the 0.18 μm CMOS technology with threshold voltages of 0.44, -0.495, and -0.73 V for NMOS, PMOS, and high-voltage PMOS transistor, respectively. Likewise, the process parameters k_n, k_p, and k_{p3} extracted from SPICE simulations are 3.362, 0.998, and 0.872 mA/V^2, respectively. Both charge pumps used the same transistor sizes, clock frequency, and pumping capacitance for comparison. The pumping and output capacitances of 5 and 10 pF, respectively, were chosen for both pumps, and the auxiliary capacitors in the PMOS charge pump were 0.5 pF.

The nominal conditions of the following figures are a loading current of 50 μA, a supply voltage of 1.8 V, and a clock frequency of 10 MHz, except where otherwise specified. Figs. 6 and 7 compare the simulated output voltages, voltages obtained using the proposed voltage model, and the voltage obtained from (2) versus output current at various supply voltages for the PMOS charge pump and the voltage doubler, respectively. The proposed voltage model and (2) are mostly consistent with the simulated results at low output currents, at which the output voltages linearly decrease as the output current increases. However, for a higher loading current and a lower supply voltage, since the on-resistance of the switching device is nonlinear, the output voltages decline nonlinearly. The proposed model takes into account the accurate on-resistance, such that the errors between the simulated results and the proposed models are always less than 5%.

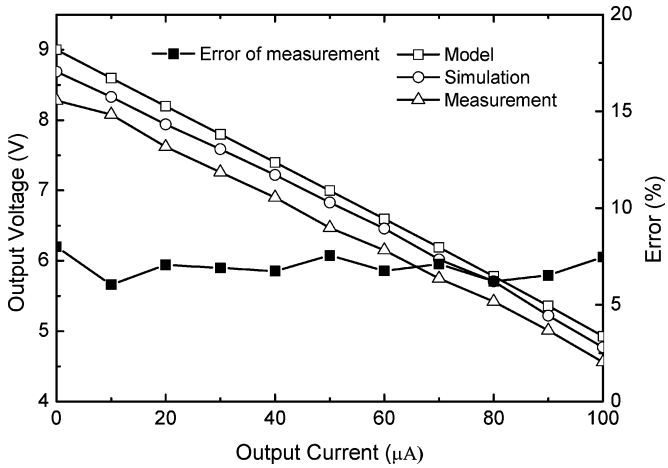


Fig. 8. Measured output voltages versus loading current are close to the model and simulation for the four-stage PMOS charge pump with $f = 10$ MHz and $V_{\mathrm{DD}} = 1.8$ V.

In Fig. 8, the measured output voltages agree with the simulated results and the results of the model for the four-stage PMOS charge pump. The differences between the measurements and the results of the model are less than 8%. Fig. 9 shows the agreement between the measurements, simulated results, and the results of the voltage model for the four-stage PMOS charge pump with various frequencies. If the parasitic capacitances at each pumping nodes are considered in (13), then the errors between the voltage models and the measurements are expected to be reduced.

Fig. 10 plots the theoretical and simulated efficiencies of both four-stage charge pumps versus frequency with a pumping capacitance of 30 pF and a loading current of 200 μA. The power efficiency is maximal at 8 MHz. The parameters α and β for the voltage doubler and the PMOS charge pump, based on the extracted postlayout parasitic parameters, are 0.1 and 0.04, and 0.1 and 0.012, respectively. The parameters α_g and β_g for the proposed charge pump are 0.1 and 0.08, respectively. From (24)

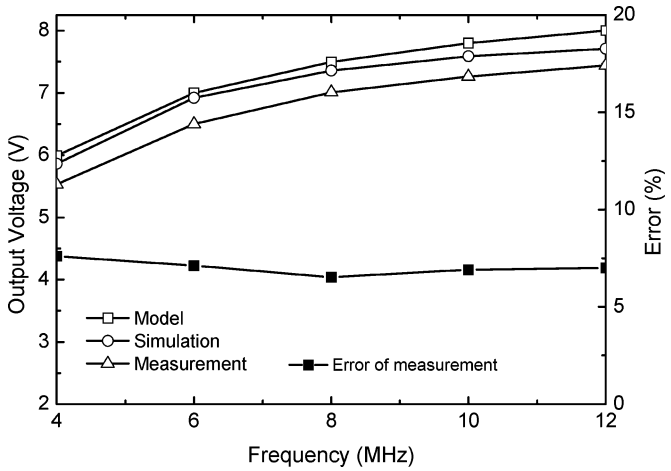


Fig. 9. Measured output voltages versus frequency are correlated well with the model and simulation for the four-stage PMOS charge pump with a loading current of 50 μA and $V_{\rm DD} = 1.8$ V.

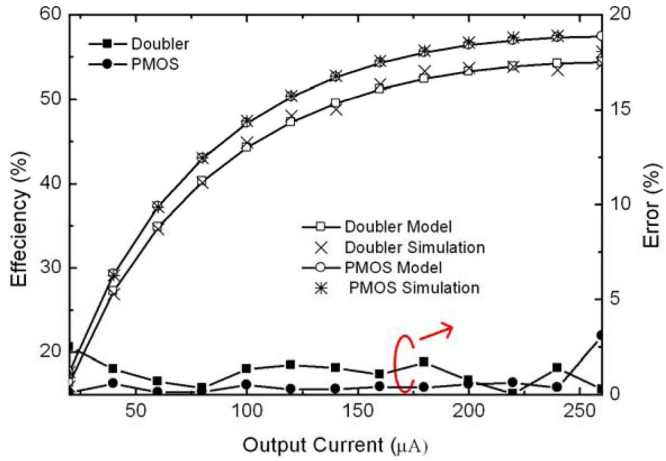


Fig. 11. Comparison of power efficiency between the model and simulation for both four-stage charge pumps as functions of loading current with $V_{\rm DD} = 1.8$ V and $C = 30$ pF.

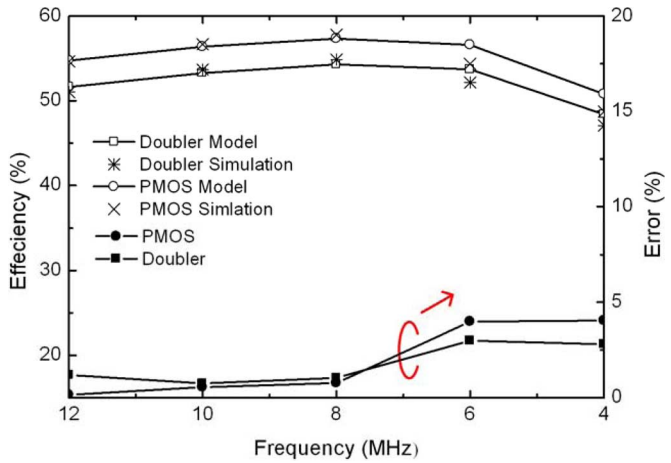


Fig. 10. Comparison of power efficiency between the model and simulation for both four-stage charge pumps for different frequencies with a loading current of 200 μA, $V_{\rm DD} = 1.8$ V, and $C = 30$ pF.

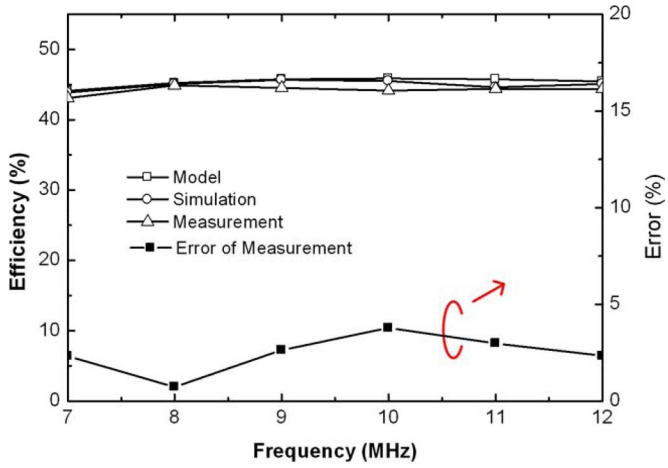


Fig. 12. Measured power efficiency versus frequency closely correspond to the model and simulation for the four-stage PMOS charge pump with a loading current of 50 μA, $V_{\rm DD} = 1.8$ V, and $C = 5$ pF.

and (25), the voltage doubler has a higher theoretical efficiency. However, since the on-resistance of the switching devices of the PMOS charge pump is smaller, the power efficiency of the proposed charge pump is slightly higher than that of voltage doubler. Fig. 11 plots the power efficiencies of both four-stage charge pumps as functions of output load with a pumping capacitance of 30 pF. The maximum simulated efficiencies for the voltage doubler and the PMOS charge pump are 54.5% and 57.5%, respectively.

Fig. 12 plots the measured power efficiency as a function of frequency under a load of 50 μA. The measured results agree well with the simulation and the model. The measured maximum power efficiency is about 45% at 8 MHz. Fig. 13 plots the theoretical and measured power efficiencies of the four-stage PMOS charge pump as functions of output current for 12 and 10 MHz under the nominal condition. Since 5 pF pumping capacitors were used to reduce the cost of chip fabrication, the power efficiencies are lower than those shown in Fig. 11. The

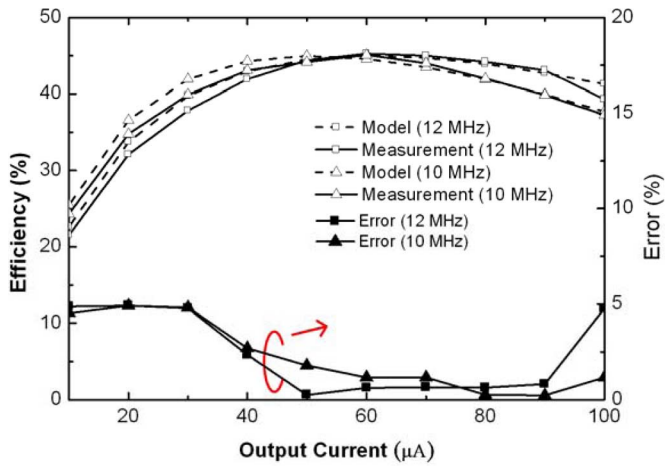
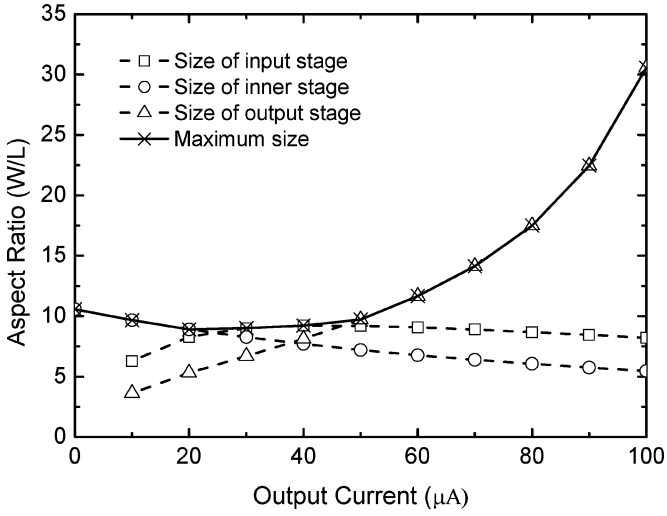
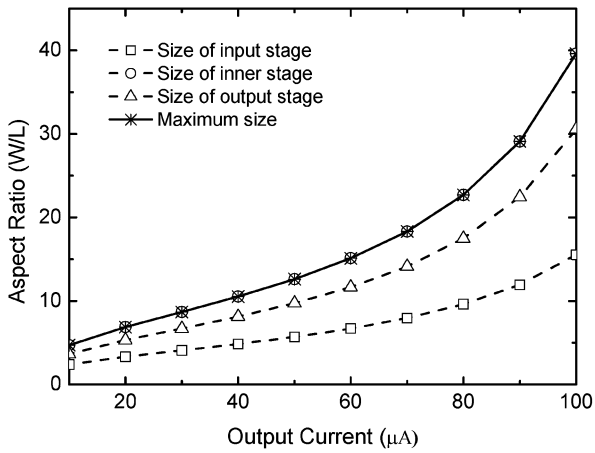


Fig. 13. Comparison of power efficiencies between model and measurements of the four-stage PMOS charge pump as functions of loading current with $V_{\rm DD} = 1.8$ V, $C = 5$ pF, and frequencies of 10 and 12 MHz.



(a)



(b)

Fig. 14. Aspect ratio (W/L). (a) PMOS charge pump. (b) Voltage doubler.

maximum measured efficiency was around 45% at a loading current of 60 μA. Solid symbols indicate the errors of the power efficiency between the model and measurements.

V. Design Methodology

In the design of charge pump circuits, maximum power efficiency is desired. The output voltages in (13) and (14) should approach that given by (1). To satisfy this requirement, the sizes of the transistors in the charge pump must be sufficiently large without overdesign. The exponential terms multiplied by their coefficients can be reasonably set to be 0.01 for $f = 10$ MHz and $C = 5$ pF. The aspect ratios (W/L) of the PMOS charge pump and the voltage doubler are shown in Fig. 14(a) and (b), respectively. The W/L ratios of the voltage doubler increased exponentially with the output current. However, those of the PMOS charge pump are not varied significantly, except the output stage, which is the same as the voltage doubler.

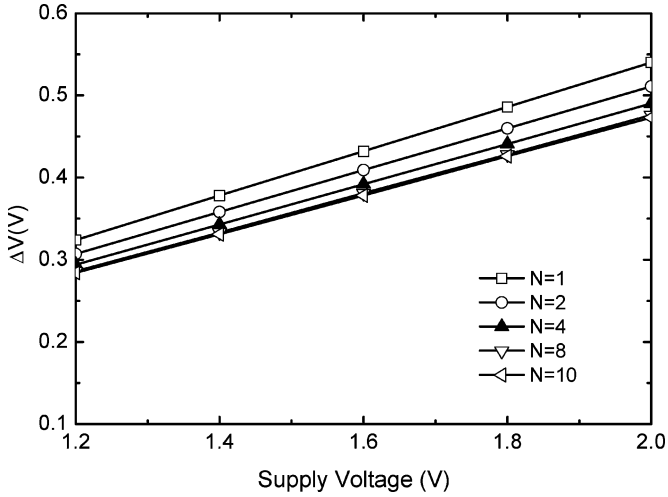


Fig. 15. Optimized factor ΔV plotted as functions of supply voltage for different stage numbers at a loading current of 50 μA and a clock frequency of 10 MHz.

If the exponential terms in (13) approach to zero, (24) can be rewritten as

$$\eta V_{\rm DD} = \frac{A - B\Delta V}{D + E/\Delta V} \tag{26}$$

where $\Delta V = I_o/2fC$ represents the optimized factor. Thus, the higher loading current leads to the higher product of pumping capacitance and clock frequency. The other parameters are

$$A = V_{\rm DD} + \frac{N}{1+\beta} V_{\rm DD} \tag{27}$$

$$B = \frac{N}{1+\beta} \tag{28}$$

$$D = N(2\gamma + 1) + 1 + \frac{2(N+1)\beta}{1+\beta} + 2N\frac{\gamma\beta_g}{1+\beta_g} \tag{29}$$

$$E = N(\alpha + 2\alpha_g\gamma)V_{\rm DD}. \tag{30}$$

These parameters can be assumed to be constant because $V_{\rm DD}$ is usually determined by the system. The others are parasitic effects, except for the number of stages N, which is an integer and can be determined later.

The optimized factor ΔV can be obtained by taking the derivative of (26) with respect to ΔV and setting the derivative to zero. The resulting ΔV can be expressed as

$$\Delta V = -\frac{E}{D} \pm \sqrt{\frac{E^2}{D^2} + \frac{AE}{BD}}. \tag{31}$$

Since ΔV must be positive, the positive sign in (31) must be selected.

According to Fig. 15, the optimized factor ΔV increased with the supply voltage for the PMOS charge pump. The required pumping capacitor and frequency for a given output load can be selected after the optimized factor is determined. For example, substituting an optimized factor of about 0.441 in Fig. 15 into (26) for $V_{\rm DD} = 1.8$ V and $N = 4$ yields a maximum power efficiency η of 46%, which agrees with the peak value in Fig. 13. Fig. 15 also indicates a small variation of the optimized factor

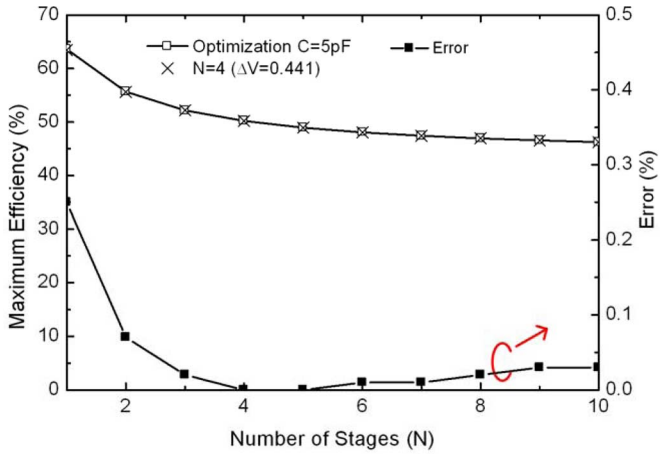


Fig. 16. Maximum power efficiency versus stage number nearly overlapped by using the actual optimized factor and the optimized factor of $N = 4$ with $C = 5$ pF.

with the number of stages. Interestingly, the optimized factor varies only slightly with the numbers of stages for the given parameters. Therefore, if the optimized factor is obtained by setting $N = 4$ for N-stage charge pumps, then the discrepancy in the maximum power efficiency is always less than 0.2% for $V_{\rm DD} = 1.8$ V, as shown in Fig. 16.

To design the optimized power-efficient PMOS charge pump, the optimized factor $\Delta V = I_o/2fC$ was first calculated using (31) for a given $V_{\rm DD}$ with $N = 4$. For example, $\Delta V = 0.441$ for $V_{\rm DD} = 1.8$ V in Fig. 15. Next, according to the required output current, *fC* is determined, and the transistor sizes are then determined using (13). Finally, the number of stages N is obtained by using (1) for the required $V_{\rm out}$. However, N is usually computed as a real number. Since N must be an integer, one of the two integers that are just higher and lower than the computed N should be the optimized number of stages. For instance, if $V_{\rm out} = 6$ V and the loading current is 50 μA, the sizes of the transistors in the PMOS charge pump are 10, as shown in Fig. 14(a), then $N = 3.13$ is determined. The possible choices are $N = 3$ and $N = 4$. Substituting these two integers into (1) yields two ΔV values, which are input into (26) to find the maximum power efficiency. In this example, $\Delta V = 0.3832$ and $\Delta V = 0.7374$ for $N = 3$ and $N = 4$, respectively. The corresponding values of η are 51.84% and 46.62%. Therefore, $N = 3$ is adopted and the pumping capacitance is 6.524 pF for a loading current of 50 μA and a clock frequency of 10 MHz.

VI. Conclusion

Analytical output voltage models for the voltage doubler and the PMOS charge pump were formulated using dynamic charge-transferred waveforms. Since the on-resistance of the switching devices can be precisely predicted, the proposed models are more accurate than any others. The accuracy of the voltage models was verified by simulation for both pumps and measurements for the PMOS charge pump using the 0.18 μm CMOS technology. The discrepancies are less than 5% and 8% in comparison to simulation and measurements, respectively. Note that the output voltage expressions can be used to explain why the PMOS charge pump can provide higher output current without increasing the transistor sizes significantly.

Compact models of power efficiency for both charge pumps were derived by including parasitic capacitance effects. The models were also verified by simulation and measurements made by using the 0.18 μm CMOS technology. The errors between the model and measurements of the four-stage PMOS charge pump are less than 5%. Finally, a design methodology is presented, in which the output voltage model is applied to determine the transistor sizes, and the optimized factor is used to determine the pumping capacitance, the clock frequency, and the number of stages that maximize power efficiency.

Appendix

The similar formulation procedure discussed in Section II for the output voltages of the voltage doubler is given here for references.

A. Voltage Model of Input Stage for Voltage Doubler

The corresponding node waveforms of transistor N_2 shown in Fig. 1 are plotted in Fig. 17(a). When clock ϕ_1 is low in time interval $[nT,\ nT + (T/2)]$, the voltages V_s and V_g of transistor N_2 are increased from $V_{\rm DD} - \Delta V$ to $V_{\rm DD}$ by charging and decreased by discharging from $2V_{\rm DD}$ to $2V_{\rm DD} - \Delta V$, respectively. The current that flows through transistor N_2 and the pumping capacitor C_1 is given by the equation for the NMOS transistor in the triode region

$$I = k_n \left\{ \left[(V_g - V_s) - V_{tn} \right] (V_d - V_s) - \frac{1}{2}(V_d - V_s)^2 \right\} \tag{A1}$$

where $k_n = \mu_n C_{\rm ox} W/L$ and V_{tn} are the process parameter with W/L factor and the threshold voltage of the NMOS transistor, respectively. From Fig. 17(a), we conclude that since $V_s + V_g = 3V_{\rm DD} - \Delta V$, the voltage V_g can be expressed as a function of V_s as

$$V_g = 3V_{\rm DD} - \Delta V - V_s. \tag{A2}$$

Substituting (A2) and $V_d = V_{\rm DD}$ into (A1) yields

$$\frac{C dV_s}{dt} = \frac{3}{2} k_n (V_{\rm DD} - V_s) \left(\frac{5}{3} V_{\rm DD} - V_s - \frac{2}{3} V_{tn} - \frac{2}{3} \Delta V \right). \tag{A3}$$

Integrating (A3) with respect to t and varying V_s from $V_{\rm DD} - \Delta V$ to V_s yields the output voltage V_s of the input stage of the voltage doubler as follows:

$$V_s = \frac{5}{3} V_{\rm DD} - \frac{2}{3} V_{tn} - \frac{2}{3} \Delta V - \frac{(2/3)(V_{\rm DD} - \Delta V - V_{tn})}{1 - [3\Delta V / \{2(V_{\rm DD} + (\Delta V/2) - V_{tn})\}] e^{-(k_n/C)(V_{\rm DD} - \Delta V - V_{tn})t}}. \tag{A4}$$

B. Voltage Model of Inner Stages for Voltage Doubler

Each inner stage of the voltage doubler consists of two NMOS transistors and two PMOS transistors. The charge transfer

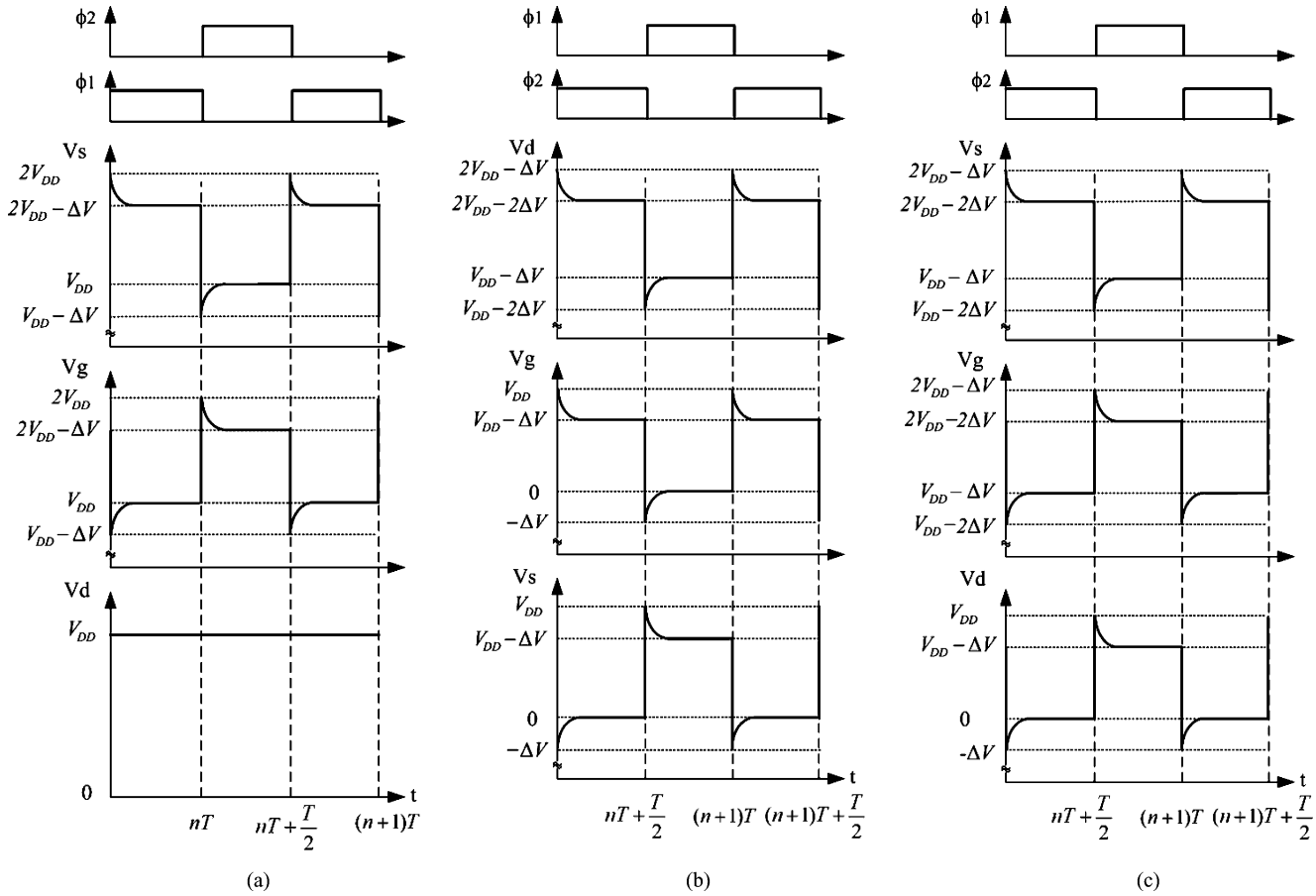


Fig. 17. Node voltage waveforms of the voltage doubler for (a) input stage, (b) PMOS transistor of the inner stage, and (c) NMOS transistor of the inner stage.

through the PMOS transistor of the voltage doubler is analyzed first, and the NMOS transistor is considered as an ideal switch. The reverse situation will be given later. The corresponding node voltage waveforms of transistor P_2 shown in Fig. 1 are shown in Fig. 17(b). In time interval $[nT + (T/2), (n{+}1)T]$, ϕ_1 is high, transistor P_2 is turned on, and the charges stored in C_2 are transferred to C_4. As plotted in Fig. 17(b), the voltage V_s of transistor P_2 is decreased by discharging from $V_{\rm DD}$ to $V_{\rm DD} - \Delta V$ and V_d is increased from $V_{\rm DD} - 2\Delta V$ to $V_{\rm DD} - \Delta V$ by charging. Meanwhile, the voltage V_g falls to $-\Delta V$ at $t = nT + (T/2)$, and then charges to 0 V before $t = (n+1)T$. From Fig. 17(b), we conclude that since $V_s + V_d = 2V_{\rm DD} - 2\Delta V$ and $V_d - V_g = V_{\rm DD} - \Delta V$, both voltages V_g and V_s can be expressed as functions of V_d as follows:

$$V_g = V_d - V_{\rm DD} + \Delta V \tag{A5}$$

$$V_s = 2V_{\rm DD} - 2\Delta V - V_d. \tag{A6}$$

Substituting (A5) and (A6) into (3) with k_{p3} and V_{t3} replaced by k_p and V_{tp}, respectively, gives

$$\frac{C dV_d}{dt} = 2k_p(V_{\rm DD} - \Delta V - V_d)(2V_{\rm DD} - 2\Delta V - V_d - V_{tp}). \tag{A7}$$

Integrating (A7) with respect to t and varying V_d from $V_{\rm DD} - 2\Delta V$ to V_d yields the output voltage V_d of the PMOS transistor of the inner stage for the voltage doubler as follows:

$$V_d = (2V_{\rm DD} - 2\Delta V - V_{tp}) - \frac{V_{\rm DD} - \Delta V - V_{tp}}{1 - [\Delta V/(V_{\rm DD} - V_{tp})]e^{-2(V_{\rm DD} - \Delta V - V_{tp})(k_p/C)t}}. \tag{A8}$$

If the operation of the NMOS transistor is considered, when ϕ_1 is high and ϕ_2 switches to low in Fig. 1, transistor N_4 is turned on. Charge is transferred from C_2 to C_4. The voltages V_d and V_g of transistor N_4 are discharged from $V_{\rm DD}$ to $V_{\rm DD} - \Delta V$ and $2V_{\rm DD} - \Delta V$ to $2V_{\rm DD} - 2\Delta V$, respectively, and the voltage V_s is increased by charging from $V_{\rm DD} - 2\Delta V$ to $V_{\rm DD} - \Delta V$. The corresponding charge transfer waveforms are shown in Fig. 17(c). From Fig. 17(c), we conclude that since $V_s + V_d = 2V_{\rm DD} - 2\Delta V$ and $V_s + V_g = 3V_{\rm DD} - 3\Delta V$, the voltages V_d and V_g can be expressed as functions of V_s as follows:

$$V_g = 3V_{\rm DD} - V_s - 3\Delta V \tag{A9}$$

$$V_d = 2V_{\rm DD} - 2\Delta V - V_s. \tag{A10}$$

Substituting (A9) and (A10) into (A1) yields

$$\frac{C dV_s}{dt} = 2k_n(V_{\rm DD} - \Delta V - V_s)(2V_{\rm DD} - 2\Delta V - V_s - V_{tn}). \tag{A11}$$

Integrating (A11) with respect to t, then varying V_s from $V_{\rm DD}-2\Delta V$ to V_s, yields the source voltage V_s of the NMOS transistor of the inner stage of the voltage doubler

$$V_s=(2V_{\rm DD}-2\Delta V-V_{tn})-\frac{V_{\rm DD}-\Delta V-V_{tn}}{1-[\Delta V/(V_{\rm DD}-V_{tn})]e^{-2(V_{\rm DD}-\Delta V-V_{tn})(k_n/C)t}}. \tag{A12}$$

The differences between (A8) and (A12) are the process parameters and the threshold voltages. The equivalent process parameter k of transistors P_2 and N_4 connected in series may be equivalent to $k_nk_p/(k_n+k_p)$. The absolute values of the threshold voltage of the PMOS and the NMOS transistors in the inner stages are assumed to be equal to simplify the formula. Substituting k into (A8), the output voltage $V_{\rm inner}$ of the inners stages for voltage doubler can be expressed as

$$V_{\rm inner}=(2V_{\rm DD}-2\Delta V-V_{tp})-\frac{V_{\rm DD}-\Delta V-V_{tp}}{1-[\Delta V/(V_{\rm DD}-V_{tp})]e^{-2(V_{\rm DD}-\Delta V-V_{tp})(k/C)t}}. \tag{A13}$$

C. Voltage Model of Output Stage for Voltage Doubler

It should be noticed that the output stage of the voltage doubler is the same as that of the PMOS charge pump. An N-stage voltage doubler has one input stage, one output stage, and (N–1) inner stages. Adding (A4), $(N-1)\times$ (A13), and (12) yields a complete expression for the output voltage of the voltage doubler as follows:

$$V_{\rm outd}=\left(2N+\frac{5}{3}\right)V_{\rm DD}-\left(2N+\frac{2}{3}\right)\Delta V-NV_{tp}-\frac{2}{3}V_{tn}-\frac{(N-1)(V_{\rm DD}-\Delta V-V_{tp})}{1-[\Delta V/(V_{\rm DD}-V_{tp})]e^{-2(V_{\rm DD}-\Delta V-V_{tp})(k/C)t}}-\frac{(2/3)(V_{\rm DD}-\Delta V-V_{tn})}{1-[3\Delta V/2(V_{\rm DD}+(\Delta V/2)-V_{tn})]e^{-(V_{\rm DD}-\Delta V-V_{tn})(k_n/C)t}}-\frac{V_{\rm DD}-\Delta V-V_{tp}}{1-[\Delta V/(V_{\rm DD}-V_{tp})]e^{-2(V_{\rm DD}-\Delta V-V_{tp})(k_p/C)t}}. \tag{A14}$$

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