A p-Channel Metal–Oxide–Semiconductor Field-Effect Transistor Charge Pump for Low Supply Voltages

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Received September 25, 2008; accepted December 2, 2008; published online April 20, 2009

In this paper, we propose a positive two-phase p-channel metal–oxide–semiconductor field-effect transistor (PMOSFET) charge pump with two auxiliary clocks to boost the gate biases of the switching transistors for low-supply-voltage applications. Owing to the effective boosting of the overdrive voltage of the charge transfer transistors, the proposed four-stage charge pump has high driving capacity and achieves a voltage gain of more than 90% with no load at a supply voltage of 1 V. The proposed charge pump was implemented using 0.18 μm standard complementary metal–oxide–semiconductor field-effect transistor (CMOSFET) technology in an area of approximately 0.205 mm^2. The measurement results agree well with the simulated data, such as the simulated and measured output voltages without load reaching 8.6 and 8.28 V at a supply voltage of 1.8 V, as well as those with a 60 μA loading current producing 6.2 and 6 V at a frequency of 10 MHz, respectively.

DOI: 10.1143/JJAP.48.04C069

1. Introduction

Charge pump circuits have been extensively adopted in many integrated circuits, such as flash memories, electrically erasable programmable read-only memory (EEPROM), liquid crystal display (LCD) displays, and micro electro mechanical system (MEMS) sensors to generate voltages that are higher than the supply voltage or lower than the ground voltage. The most popular schemes are based on the Dickson structure using n-channel metal–oxide–semiconductor field-effect transistors (NMOSFET).[1] However, the threshold voltage and the body effect degrade the performance of the Dickson charge pump when the number of stages is increased.

Many charge pumps, such as four-phase[2] and voltage doubler charge pumps,[3] as shown in Fig. 1, can minimize the effects caused by threshold voltages and body effects. However, the body effects may become more pronounced if the body potentials of charge transfer transistors are not dealt with carefully. To solve this problem, the bodies are either connected to their source/drain electrodes[4] or to special circuits to control the well potentials.[5] These charge pumps require a larger guard ring area, since p-type substrates are usually employed in triple-well complementary metal–oxide–semiconductor field-effect transistor (CMOSFET) technology. They may not even be feasible in a twin-well CMOSFET process with p-substrates. In addition, the driving capacity of voltage doubler charge pumps may be degraded at lower supply voltages owing to the low overdrive voltage of transfer devices.[6]

If only p-channel MOSFETs (PMOSFET) are used for positive charge pumps, N-wells are easy to isolate using a smaller guard ring area, and thus, twin-well processes with p-type substrates can be selected for implementation. Recently, Racape and Daga[7] proposed a PMOSFET charge pump using standard CMOSFET processes, as shown in Fig. 2, which requires a four-phase clock generator and six PMOSFETs in each stage. In this paper, we propose a new PMOSFET charge pump. One stage of the proposed PMOSFET charge pump requires only four PMOSFET devices with two-phase clocks and two simple auxiliary clocks.

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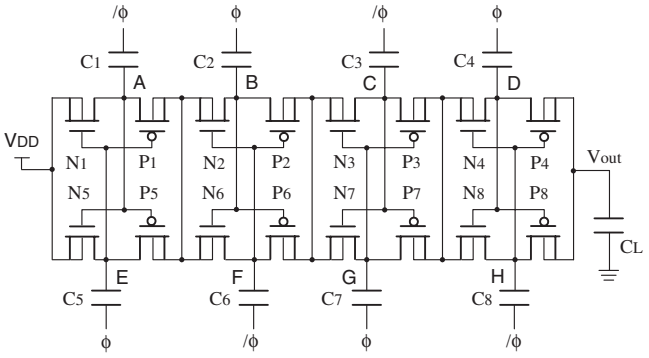

Fig. 1. Four-stage voltage doubler pumping circuit as described in ref. 3.

This paper is organized as follows. In §2, we present the proposed PMOSFET charge pump circuit and its operations. In §3, we demonstrate the agreement between the simulation and measurement of the proposed scheme. Conclusions are drawn in §4.

2. Proposed PMOSFET Charge Pump

The proposed PMOSFET charge pump circuit and the clock waveforms are shown in Figs. 3(a) and 3(b), respectively. The circuit has two pumping branches, the top branch and the bottom branch, which alternatively transfer charges to the output (V_{out}). Each stage comprises a pair of pumping capacitors, C_i and C_{i+4}, where $i = [1, 4]$, a pair of auxiliary capacitors, C_{gi} and C_{gi+4}, a pair of PMOSFET switches, M_i and M_{i+4}, and a pair of auxiliary transistors, Mp_i and Mp_{i+4}. The pumping capacitors and the auxiliary capacitors are driven by two nonoverlapping clocks, ϕ_1 and ϕ_2, and two auxiliary clocks, δ_1 and δ_2, respectively. The first stage is from V_{DD} to node A/E. The body electrodes are connected to node A or E for the top or the bottom branches, respectively. The second to fourth stages are from A/E to B/F, B/F to C/G, and C/G to D/H, respectively. The output stage comprises two cross-connected transistors, M_{o1} and M_{o2}.

According to Fig. 3(b), the two auxiliary clocks δ_1 and δ_2 can easily be generated from clocks ϕ_1 and ϕ_2. When ϕ_1 is low and ϕ_2 is high during time t_1, transistor M_{a2} is turned off and transistors M_{a1} and M_{b1} are turned on. Therefore, δ_1 becomes low and charge is transferred from V_{DD} to node 1.

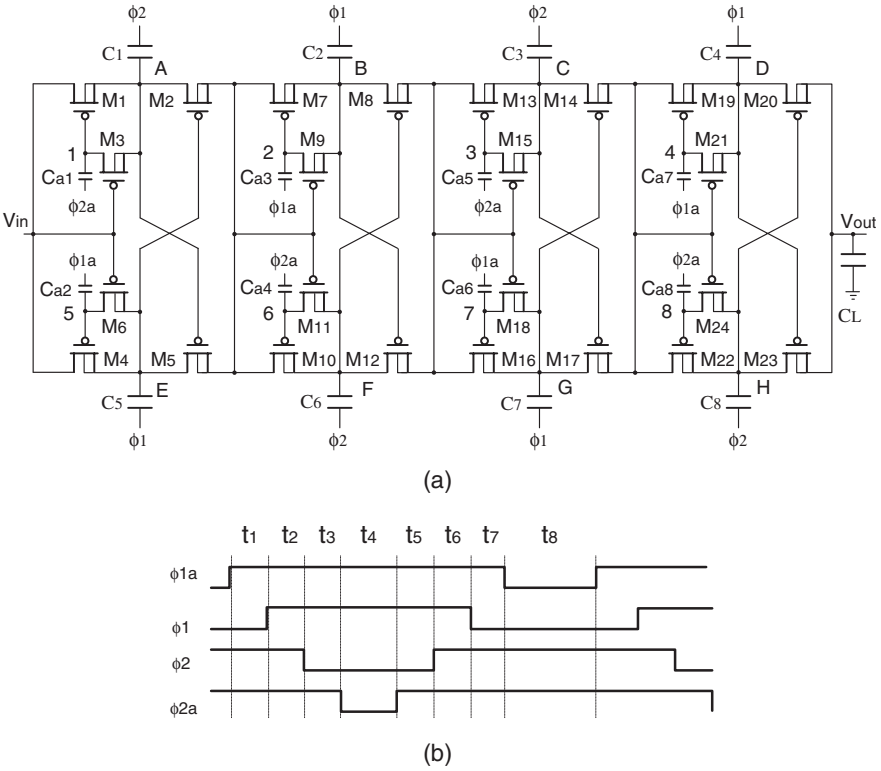

Fig. 2. Four-stage Racape and Daga's PMOSFET charge pump circuit as described in ref. 7.

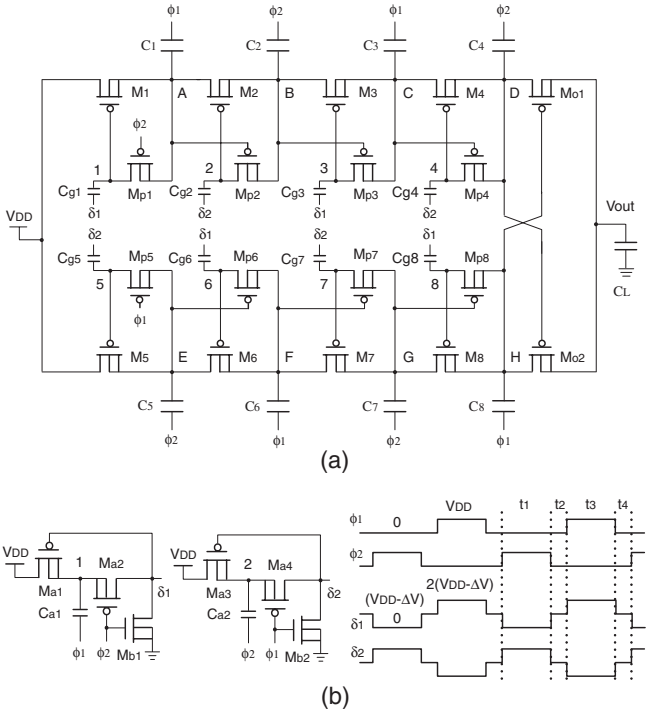

Fig. 3. Proposed four-stage PMOSFET charge pump. (a) Circuit diagram and (b) clock patterns and auxiliary clock generator.

Then, ϕ_2 becomes low at time t_2, transistors M_{b1} and M_{a1} are turned off, but transistor M_{a2} is turned on to make δ_1 become $V_{DD} - \Delta V$, where ΔV is the voltage degradation due to parasitic effects. At time interval t_3, clock ϕ_1 becomes high. M_{a1} and M_{b1} are still turned off, and M_{a2} is turned on, so δ_1 jumps from $V_{DD} - \Delta V$ to $2(V_{DD} - \Delta V)$. The operation of time t_4 is similar to that of time t_2. The operations of the auxiliary clock δ_2 resemble those of the auxiliary clock δ_1 but with a 180° phase difference. Note that time intervals t_2 and t_4 are much smaller than the clock cycle and Fig. 3(b) is not scaled for t_2 and t_4.

Detailed operations of the proposed PMOSFET charge pump in one clock cycle are described below for each stage. The ideal waveforms of the proposed charge pump at nodes A to H and nodes 1 to 8 are shown in Fig. 4 for the case without loading current and with ΔV assumed to be zero.

2.1 First stage

During time t_1, transistor M_1 is turned on to transfer charges from V_{DD} to node A and transistor M_{p5} is also turned on to transfer charges from capacitor C_{g5} to node E, but transistors M_5 and M_{p1} are turned off to cut off the paths from node E to V_{DD} and from node A back to capacitor C_{g1}, respectively. At time t_2, clocks ϕ_2 and δ_2 drop V_{DD} at the same time, so transistor M_i is turned off in a short period of time. The charges in C_{gi} and C_i are shared during this time. The operations in time interval t_3 resemble those in t_1 with the roles of the devices interchanged. The operation of time interval t_4 is identical to that of time interval t_2.

2.2 Second stage

During time interval t_1, transistors M_2 and M_{p6} are turned off to cut off the paths from node B to node A and from node F to capacitor C_{g6}, respectively. Transistors M_6 and M_{p2} are turned on to transfer charges from node E to node F and from capacitor C_{g2} to node B, respectively. At times t_2 and t_4, similarly to the operations in the first stage, transistors M_2 and M_6 are both turned off, but transistors

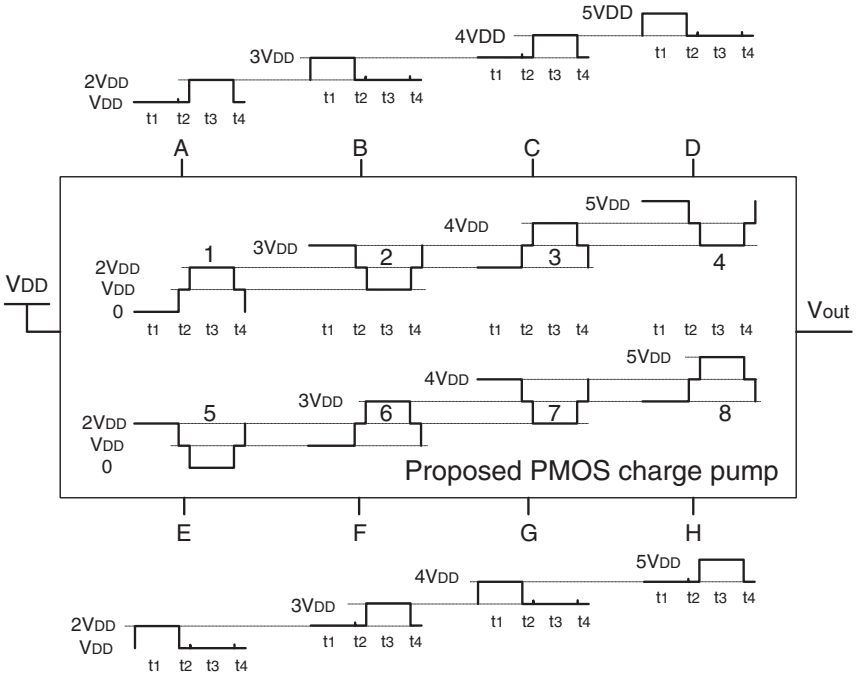

Fig. 4. Waveforms of the internal nodes in the proposed PMOSFET charge pump.

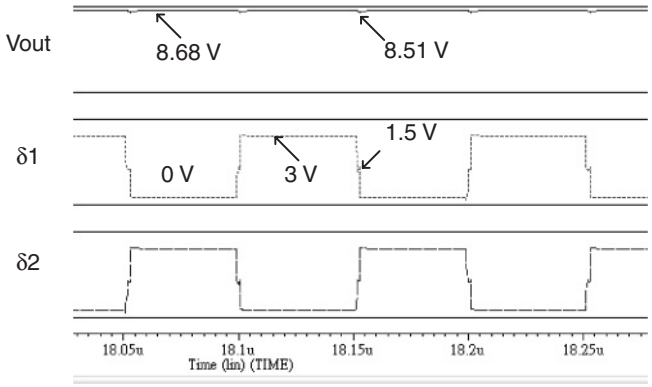

Fig. 5. Simulated waveforms of the output node and the two auxiliary clocks at a supply voltage of 1.8 V and a frequency of 10 MHz.

M_{p2} and M_{p6} are turned on. Meanwhile, charges sharing occur between node B and capacitor C_{g2} through transistor M_{p2}, as well as node F and capacitor C_{g6} through transistor M_{p6}. The operations in time interval t_3 are similar to those in t_1 with the roles of the devices interchanged. The operations of stages 3 and 4 are also similar to those of stage 2.

2.3 Output stage

During time interval t_1, transistor M_{o1} is turned on and the charges are transferred from node D to output capacitor C_L, but transistor M_{o2} is turned off to cut off the path from V_{out} back to node H. A similar operation occurs at time interval t_3. Notably, because the time intervals t_2 and t_4 are much smaller than the clock cycle, only negligible charges are transferred back through transistors M_{o1} and M_{o2} during these two intervals. Figure 5 shows the simulated waveforms of clocks δ_1 and δ_2, and V_{out} with $V_{DD} = 1.8$ V and a clock frequency of 10 MHz.

3. Simulation and Measurement Results

In an N-stage PMOSFET charge pump, the output voltage is expressed as

$$V_{out} = V_{DD} + N\left(\frac{C}{C + C_{top}}\right)V_{DD} - \frac{NI_{load}}{f(C + C_{top})}, \quad (1)$$

where C denotes the total pumping capacitance in each stage, which is $C_i + C_{i+4}$ for the proposed circuit. C_{top} represents the switch-node parasitic capacitance, I_{load} indicates the loading current, and f is the clock frequency, the amplitude of which is the same as the supply voltage (V_{DD}). If C_{top} is much smaller than C, the output voltage of the proposed four-stage PMOS charge pump without loading current is close to 5 V_{DD}.

The three four-stage charge pumps were simulated using 0.18 μm CMOSFET technology. These charge pumps were designed using the same pumping capacitance, clock frequency, and optimized transistor size for maximum output voltages. Pumping and output capacitances of 5 and 10 pF, respectively, were chosen for all pumps. The auxiliary capacitors of Racapa and Daga's charge pump and the proposed PMOSFET charge pump were 0.5 pF.

Figure 6 shows the simulated output voltages of the proposed PMOSFET charge pump for different output currents and supply voltages at 10 MHz. The output voltages are decreased linearly when the output current is increased. Even though the supply voltage is less than 1 V, the proposed PMOSFET charge pump still has a voltage gain of more than 90%, where the voltage gain is defined as the actual output voltage divided by $(N + 1)V_{DD}$ with no load.

Figure 7 shows a comparison of the simulated output voltages of the voltage doublers,[3] Racape and Daga's charge pump,[7] and the proposed PMOSFET charge pump for different loading currents and supply voltages at a frequency of 10 MHz. The output voltages of the three

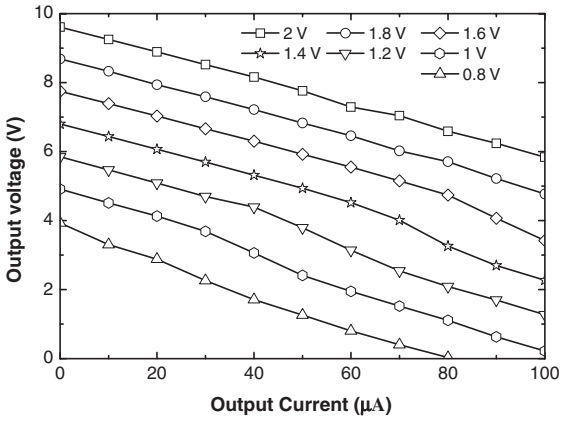

Fig. 6. Simulated output voltages of the proposed four-stage PMOSFET charge pump for different loading currents and supply voltages.

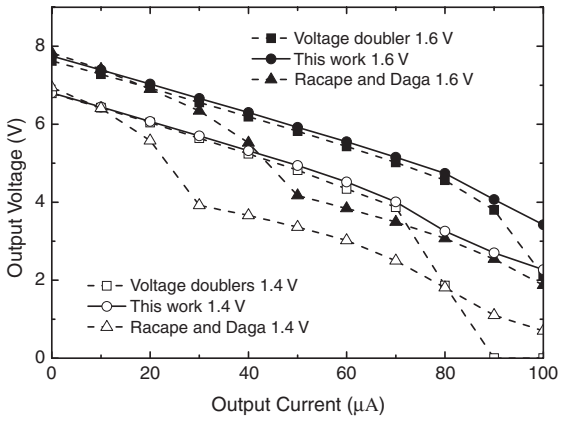

Fig. 7. Comparison of output voltages of the voltage-doubler, Racape and Daga's, and the proposed four-stage PMOSFET charge pumps for different loading currents and supply voltages.

charge pumps are decreased when the loading current is increased. However, the proposed PMOSFET charge pump has higher output voltages for a larger loading current because the proposed PMOSFET charge pump has higher overdrive voltages for the charge transfer devices to be fully turned on and off. Thus, the proposed circuit provides a higher voltage gain and is suitable for low-supply-voltage applications.

Figure 8 shows a photomicrograph of the test chip with an area of about 0.205 mm^2. A 5 pF MIM-type pumping capacitor was selected for implementation. A gate-boosting capacitor and an output capacitor of 0.5 and 10 pF, respectively, were selected. Figure 9 shows the measured output waveform of the proposed PMOSFET charge pump at a frequency of 10 MHz and a supply voltage of 1.8 V. The output voltage is about 8.28 V and the voltage gain is more than 92%. The simulated and measured output voltages versus supply voltages, as well as the measured voltage gains versus supply voltages without loading current are shown in Fig. 10. The measured output voltages are slightly lower than the simulation results. This may be due to parasitic effects of pad capacitance, and package capacitance and resistance. Figure 11 shows the simulated and measured output voltages versus loading current at a supply voltage of

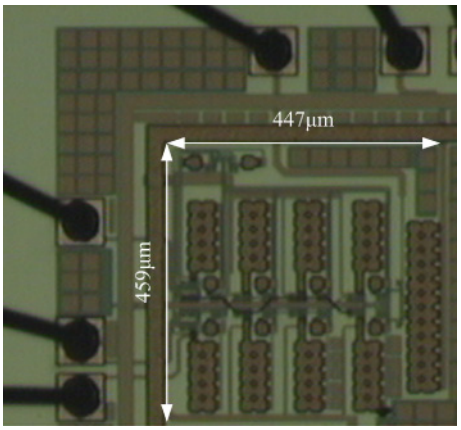

Fig. 8. (Color online) Chip photomicrograph of the proposed four-stage PMOFETS charge pump circuit.

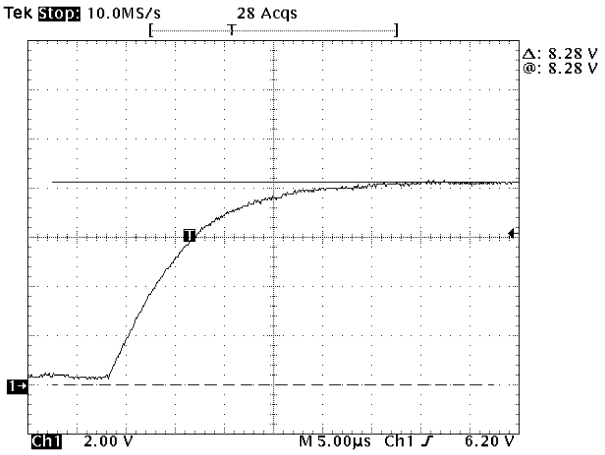

Fig. 9. Measured waveform of the proposed PMOSFET charge pump at a frequency of 10 MHz and a supply voltage of 1.8 V.

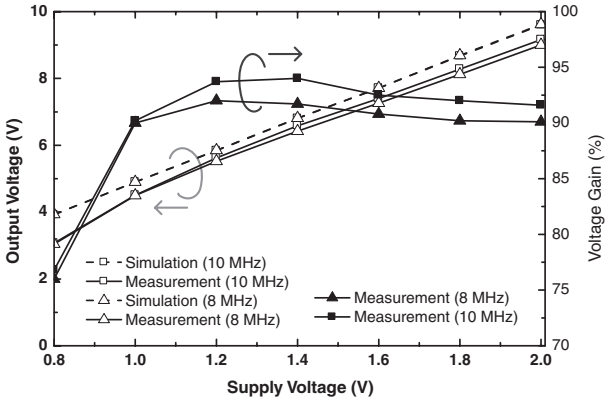

Fig. 10. Simulated and measured output voltages and measured voltage gains of the proposed four-stage PMOSFET charge pump against supply voltage without load at frequencies of 8 and 10 MHz.

1.8 V. The measured data agree well with the simulation results.

The power efficiency of a charge pump was also investigated. It is defined as the output power, P_o, divided by input power, P_i, and can be written as

$$\eta = \frac{P_o}{P_i} = \frac{V_{out} I_{load}}{V_{DD} I_{power}}, \quad (2)$$

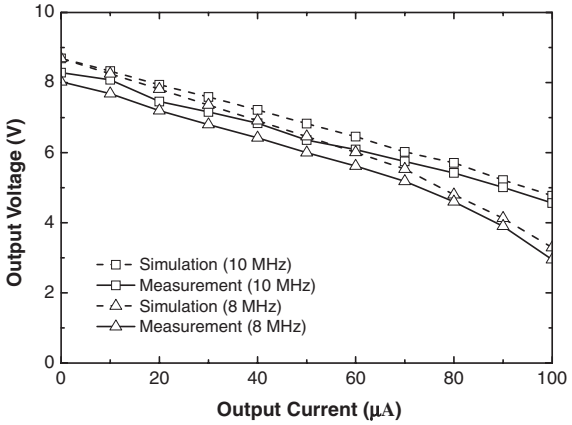

Fig. 11. Simulated and measured output voltages of the proposed four-stage PMOSFET charge pump versus loading current at V_{DD} = 1.8 V with frequencies of 8 and 10 MHz.

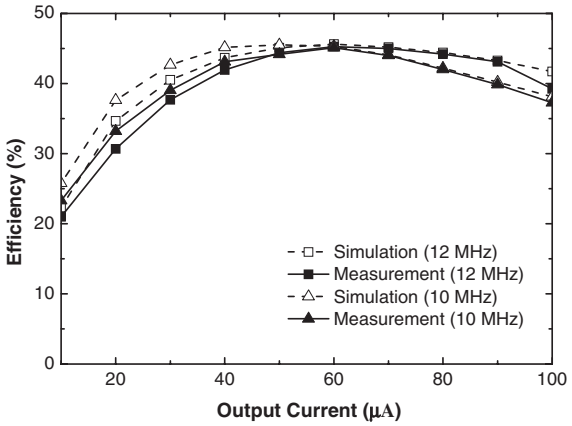

Fig. 12. Comparison of simulated and measured power efficiencies of the proposed four-stage PMOSFET charge pump for various loading currents at V_{DD} = 1.8 V with frequencies of 10 and 12 MHz.

where I_{power} denotes the total current drawn from the power supply and V_{out} is the output voltage.

The simulated and measured power efficiencies of the proposed four-stage charge pump with different loading currents and frequencies have good agreement, and are plotted in Fig. 12. The peak values of the power efficiency at a supply voltage 1.8 V are approximately 46% for 12 and 10 MHz at loading currents of 60 and 50 μA, respectively. Figure 13 also shows the agreement between simulation and measurement results for the output voltage and power efficiencies with a loading current of 50 μA and clock frequencies from 6 to 12 MHz. The maximum measured power efficiency and output voltage of the proposed PMOSFET charge pump were 45% at a frequency of 8 MHz and 6.6 V at a frequency of 12 MHz, respectively. Note that the power efficiency was not optimized in this experiment, since smaller pumping capacitors were selected for chip implementation in a smaller area. In fact, the proposed charge pump could reach nearly 70% of power efficiency if larger pumping capacitors are employed.

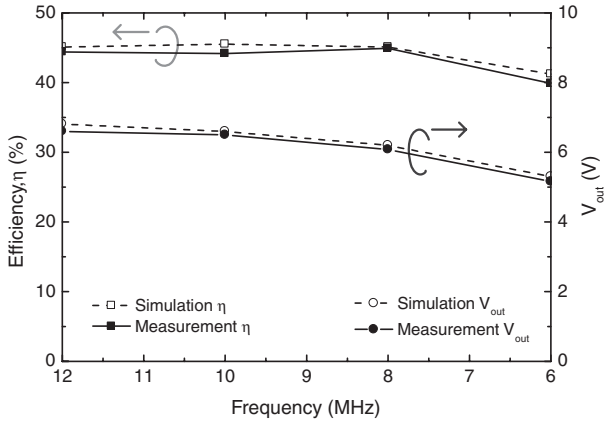

Fig. 13. Comparison of output voltages and efficiencies of the proposed four-stage PMOSFET charge pump for various frequencies with V_{DD} = 1.8 V and a loading current of 50 μA.

4. Conclusions

A new two-phase PMOSFET charge pump is proposed and was implemented using standard 0.18 μm CMOSFET technology. Its voltage gain is higher than those of the voltage doubler and Racape and Daga's charge pump because the transfer devices of the proposed PMOSFET charge pump can be fully turned on and off even at very low supply voltages. The simulated output voltages and power efficiencies of the proposed PMOSFET charge pump are in good agreement with the experimental data for various conditions, such as loading currents and clock frequencies. The measurement results show that the proposed four-stage charge pump has high driving capability with a voltage gain of more than 90% even at a supply voltage of 1.0 V.

Acknowledgments

The authors would like to thank the Chip Implementation Center (CIC) of the National Applied Research Laboratories (NARL) of Taiwan for chip fabrication, and the National Science Council of Taiwan for financially supporting this research under Contract nos. NSC 96-2221-E-005-091 and NSC 96-2220-E-005-005, as well as the Ministry of Education, Taiwan, for partial support under the ATU plan.

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