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TECHNICAL PAPER

Evaluation of multi-Gbps serial link using wire-bonded multiple exposed pads (M-pad) leadframe package

Nansen Chen · Hongchin Lin

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Abstract The conventional exposed pad low-profile quad flat pack (E-pad LQFP) package is a low cost solution for multimedia chips, but its disadvantages are limited pin count and worse electrical characteristics. In order to increase their pin utilization rate and electrical characteristics for high-speed applications, an innovative leadframe package, named multiple exposed pads (M-pad) LQFP package, is proposed. By bonding all power and ground wires to their dedicated exposed pads, the leads originally bonded to the corresponding power and ground wires can be used as the spared leads for the other signals, or they can be just removed to reduce the lead numbers, and thus the size and cost of the M-pad leadframe package. The M-pad LQFP package was evaluated for manufacturing processes and electrical characteristics. The parasitics of power nets and S-parameters of high-speed differential signals were extracted using 3D electromagnetic field solvers. The simulated power parasitics of M-pad LQFP are much lower than those of E-pad LQFP and BGA packages. The simulated differential S-parameters of M-pad LQFP also indicate less signal loss compared with those of E-pad LQFP. The co-simulation of chip-(M-pad) package-board with multi-Gbps serial link was performed with well-behaved eye-diagrams that conform to high-definition multimedia interface (HDMI) specification.

N. Chen (✉) · H. Lin
Department of Electrical Engineering, National Chung-Hsing University, No. 250, Kuo-Kuang Rd., Taichung 402, Taiwan
e-mail: nansen.chen@mediatek.com

H. Lin
e-mail: hclin@dragon.nchu.edu.tw

N. Chen
Digital Home BU, MediaTek Inc, No. 1, Dusing Rd. 1, Hsinchu Science Park, Hsinchu 300, Taiwan

1 Introduction

The technology trend in the consumer electronics can be summarized as more functionalities in a smaller geometry with lower cost. Since the first working integrated circuit (IC) was invented in 1958 (The Nobel Foundation 2007), the leadframe packages have been served as the IC encapsulation for almost a half century. The leadframe packages are always treated as a low-level application due to their limited pin count and worse electrical characteristics. After the exposed pad (E-pad) leadframe packages were developed, the exposed die-pad could be served as a grounding pad where all the digital and analog ground pads on the chip could be bonded onto the exposed die-pad. Therefore, the leads originally bonded to the respective digital and analog ground pads on the chip can be used for the other purposes. However, for some system-on-chips (SoC) with mixed signal designs, the high-speed digital ground noises may adversely affect the analog signal paths. The proposed multiple exposed pads (M-pad) leadframe package that splits the unique exposed pad of the conventional E-pad leadframe package into several exposed pads is beneficial for high-speed SoC applications. Since the photochemical machines are popularly used in package assembly of bump chip carrier (BCC) (Mercado et al. 2004), thin array plastic package (TAPP) (Chen et al. 2005), and non-leaded bump array (NBA) (Hung et al. 2006), it makes the two-stage etching methodology possible to fabricate the M-pad leadframe package. In this paper, the manufacturing processes and electrical characteristics of M-pad leadframe packages are evaluated first. Then, the 3D electromagnetic field solvers were also used to extract their parasitics and differential S-parameters up to 15 GHz. Further investigation of transient analyses with multi-Gbps serial links using HDMI interface was followed. The analyses show that the M-pad

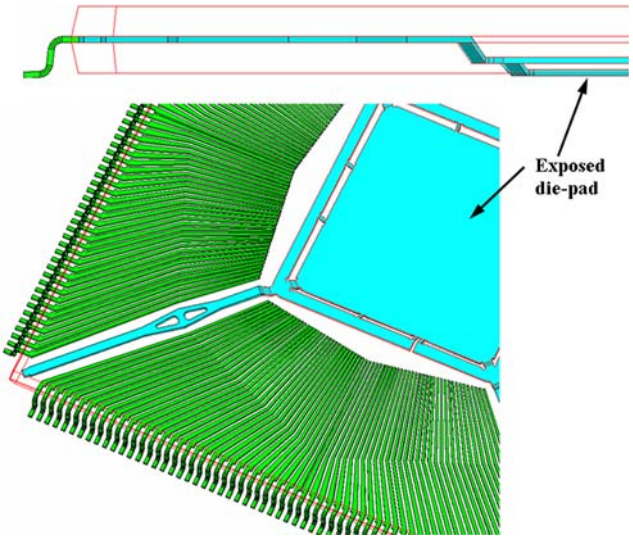

Fig. 1 Conventional E-pad LQFP package with only one exposed die-pad

leadframe package has excellent electrical characteristics that are appropriate for high-speed and mixed signal applications.

2 Package structures

The conventional E-pad LQFP package, as shown in Fig. 1, which has only one exposed die-pad for bonding all digital and analog ground wires from the chip. Figure 2 shows the M-pad structure splitting the exposed die pad into several independent exposed pads, which are not supported by leads, held by the molding compound after package assembly. Those exposed pads can be designed as different digital/analog power and ground planes, or high-speed signal pads for wire bonding. Figure 3 illustrates another application for the system in package (SiP) that includes two chips and one pair of high-speed differential wires bonded onto their corresponding exposed pads. Due to shorter bond wires, the improved electrical characteristics can be expected. Mounting passive components, such as decoupling capacitors between power and ground pads, is applicable in the package. Both the E-pad and M-pad LQFP packages are made of copper alloy, such as C7025 or A42, with the same inner/outer lead pitch, lead thickness (0.127 mm), down-set and package thickness, as well as encapsulated with the same molding compound. Since the die-pad size in M-pad leadframe package is still larger than the die size, its thermal characteristics is similar to that of E-pad leadframe package.

3 Manufacturing evaluation

The M-pad leadframe with 127-μm thickness can be fabricated with the stamping or etching technologies. However, the etching method is recommended because the half-etching can be adopted to design the reverse T-shaped mold lock, as shown in Fig. 2b, which can improve the package reliability and delamination. The bottom side of each exposed pad can be etched with a ringed groove which can prevent mold resin bleed-out during package

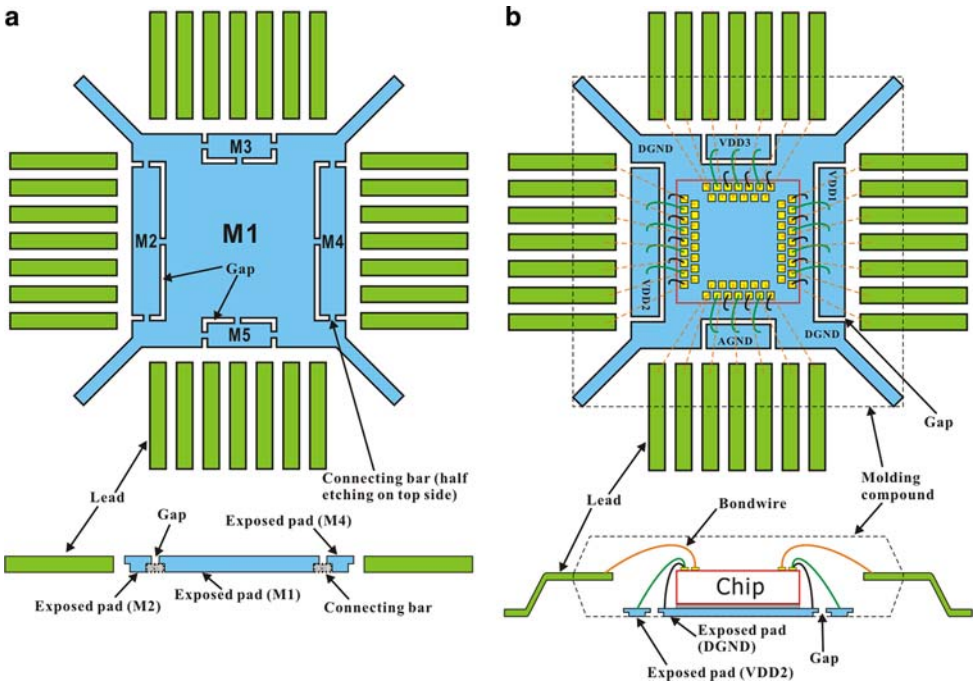

Fig. 2 The *top* and *cross-sectional views* of M-pad leadframe package **a** before assembly and down-set, **b** after assembly processes

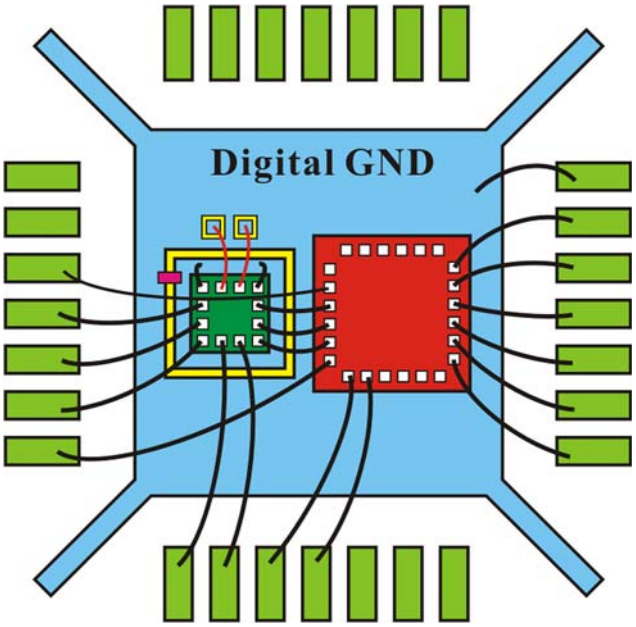

Fig. 3 SiP application using M-pad leadframe package to integrate multi-chips and passive components

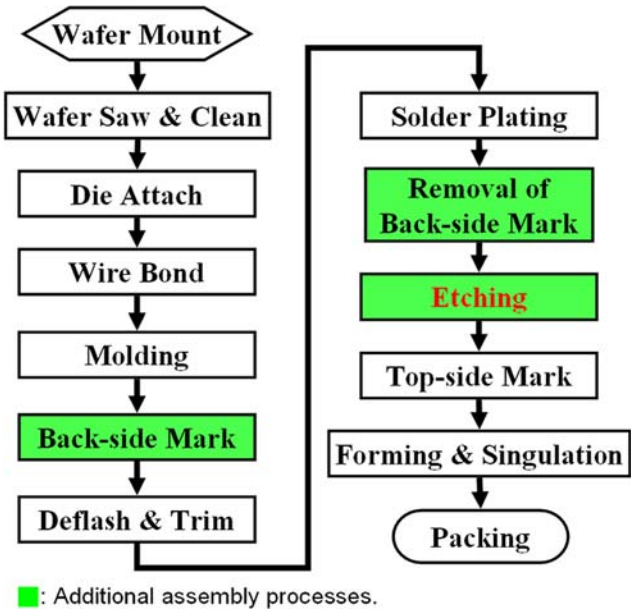

Fig. 4 The assembly process modified from the conventional leadframe process (*white blocks*) for M-pad leadframe package

assembly. Figure 2a illustrates that the top connecting bars are etched half for 63.5-μm thickness in the leadframe supplier. The conventional leadframe package assembly process can be used except "Back-side Mark", "Removal of Back-side Mark", and "Etching" after "Molding" as shown in Fig. 4. "Back-side Mark" is to print with the artwork or photoresist on the connecting bars of the bottom metal for the purpose of plating (Sn) resistant. After the

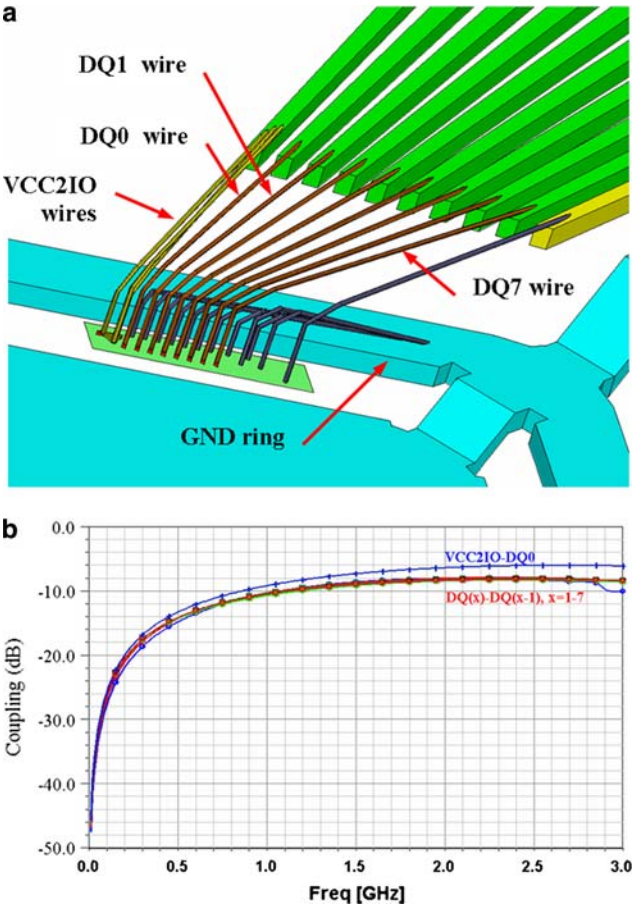

Fig. 5 The geometry and coupling for E-pad LQFP256 package. **a** 3-D view of wire portion showing triple gold-wires bonding for VCC2IO. **b** Simulated S-parameters for near end coupling at wire side

package is plated with tin (Sn) except the connecting bars, the molded package with exposed leadframe is protected and resistant to corrosion. Then, the artwork or photoresist on the bottom side of connecting bars is removed. The connecting bars are etched away in the photochemical machine and each exposed pad is electrically isolated. Because the most manufacturing processes are the same with those in the leadframe vendor and assembly house, the expected cost would be between the conventional E-pad leadframe and BGA packages.

4 Electrical design and simulation

The package is acted like a low pass filter (LPF) that filters out high-frequency components of high-speed signals. Lower parasitic inductance and capacitance in the package may relax the LPF effect. The most popular solution to reduce inductance in package is to bond multiple gold-wires for power or ground nets. Figure 5a illustrates an example of a power net (VCC2IO) in the E-pad LQFP256 package with triple gold-wires adjacent to the high-speed

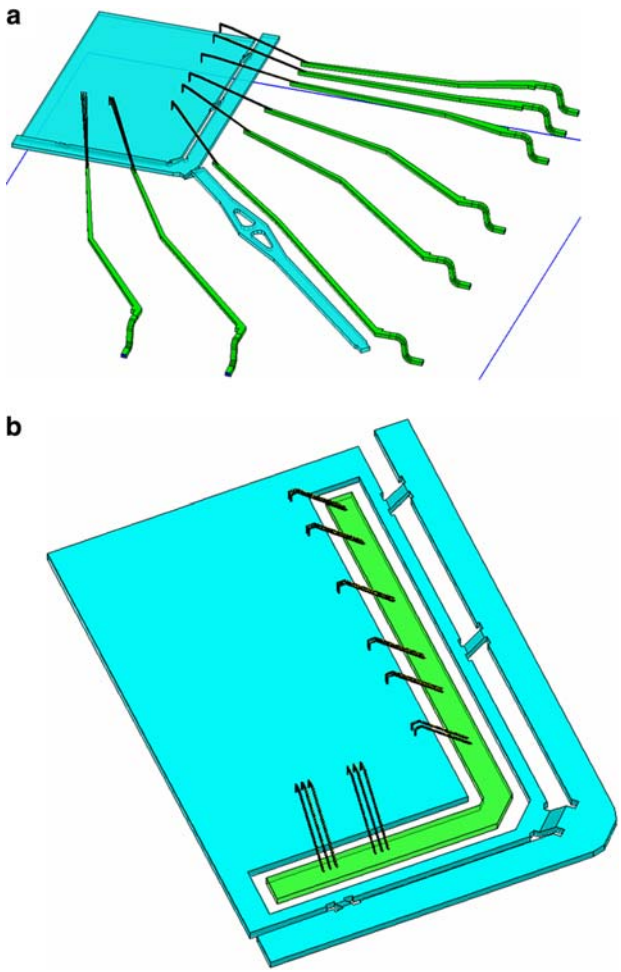

Fig. 6 Power delivery configurations for DDR SDRAM for different leadframe packages. **a** Conventional E-pad LQFP with 8 leads and 18 gold wires, and **b** M-pad LQFP with 18 shorter gold wires and a dedicated exposed power pad

signal, DQ0. According to the simulated S-parameters shown in Fig. 5b, the power net (VCC2IO) couples more noise (about 2 dB) from DQ0 compared to the other signals (DQx, $x = 1 \sim 7$). Triple gold-wires reduce the power inductance, but they couples more noise from the adjacent high-speed signals and results in less efficient power delivery. Separating the power net from the high-speed nets can reduce the power coupling from the adjacent wires. It can be implemented by using the M-pad structure as depicted in Fig. 6. There are 8 leads and 18 gold wires designed for the power delivery system of DDR SDRAM controller in the conventional E-pad LQFP256 package. A larger inductance is expected due to its longer gold-wires and leads compared to the M-pad LQFP with only 18 shorter gold wires bonding onto the dedicated exposed pad without any lead for interconnection.

The Ansoft Maxwell 3-D Quick Parameter Extractor was used to extract power parasitics in some packages and the results are summarized in Table 1. The results indicate that M-pad leadframe package has the smallest resistance of 4.1 mΩ and the smallest inductance of 0.17 nH among all of the leadframe and BGA packages except BGA465 package bonding with 65 wires for DVDD2 net. With the shortest electrical path, gold-wire length plus 0.127-mm thickness of exposed pad, the M-pad leadframe package achieves very low parasitics. Thus, less IR drop and power impedance can be achieved.

S-parameters are important for evaluating high-speed signal losses in frequency domain. A less insertion loss is preferred, meanwhile a less return loss and coupling must be preserved. To avoid reflection in the BGA package, a straightforward solution is to reduce the effects of impedance discontinuity including the bonding wires, via-holes, and solder balls (Kam et al. 2006). Larger signal loss is always occurred in the LQFP package due to only one metal layer in the package, which is hard to control the lead impedance, and thus results in larger reflection and coupling.

Figure 7 shows the electrical design for dual channels of differential net for serial link applications. The E-pad LQFP256 package on the PCB includes the shorter copper traces (5.8 mm) and longer gold-wires (3.3–3.4 mm) bonding onto their corresponding inner leads. The M-pad LQFP256 package on the PCB includes the longer copper traces (15.7 mm) and shorter gold-wires (1.4–1.5 mm) bonding onto their corresponding exposed signal pads. Their total interconnecting lengths are almost the same. Without using the leads for signal transmission in the M-pad LQFP256 package, a less reflection and coupling can be expected. The differential traces are routed on the top

Table 1 Comparison of power parasitics between different packages

Package type	Layer no.	Net name	Wire count	Lead/ball count	R_{dc} (mΩ)	L_{dc} (nH)
E-pad LQFP256	N/A	VCC2IO	18	8	13.3	3.75
M-pad LQFP256	N/A	VCC2IO	18	0	4.1	0.17
BGA388	2	DVDD2	12	5	21.1	4.13
BGA465	4	DVDD2	65	18	3.4	1.53
BGA680	4	VDD18	36	10	8.2	1.69
BGA680	4	VDD33	45	11	5.2	0.94

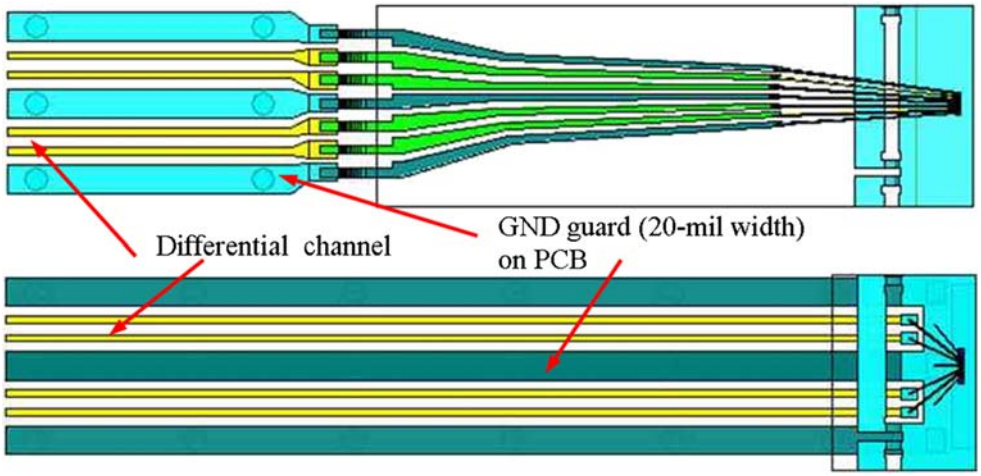

Fig. 7 *Top view* of package on PCB for E-pad LQFP256 (*top*) and M-pad LQFP256 (*bottom*) packages

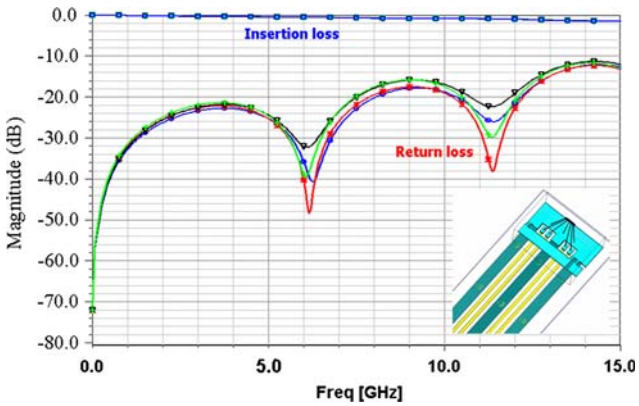

Fig. 8 Simulated insertion and return loss of M-pad leadframe package

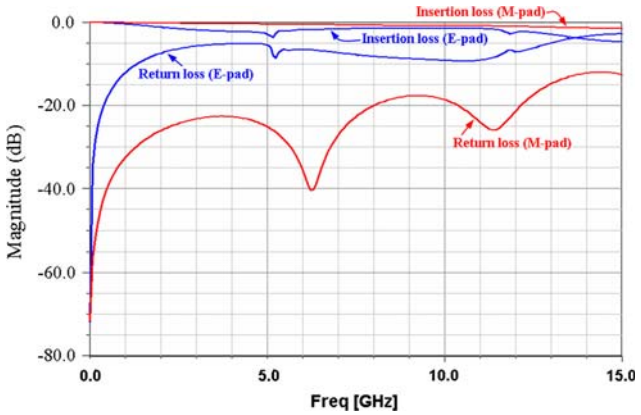

Fig. 9 Comparison of differential S-parameters between M-pad and E-pad LQFP256 packages

layer of PCB are 34-μm thickness, 127-μm signal width, 203-μm signal space, and 178-μm ground space. The PCB has four metal layers with 10.2-μm solder-mask thickness and 114-μm prepreg (PP) thickness, and their differential impedance on the PCB is about 99 Ω with the ground layer in the PCB was located 0.148-mm below the package. The S-parameters of the 8-port structure were obtained using Ansoft HFSS up to 15 GHz. The dielectric D_k/D_f (dielectric constant/loss tangent) for molding compound, solder mask and FR-4 epoxy in PCB are 4.4/0.01, 3.4/0.03, and 4.4/0.02, respectively. The results indicate that the M-pad leadframe package achieves very low insertion loss, −0.5 dB at 5 GHz, −0.9 dB at 10 GHz, and −1.5 dB at 15 GHz as shown in Fig. 8. The figure also shows no resonance, which indicates EMI would be less. All return losses are less than −20 dB up to 7 GHz that can conform to the electrical specification of serial ATA Gen2 (Serial ATA International Organization 2007). Figure 9 demonstrates the comparison of differential S-parameters between M-pad and E-pad LQFP up to 15 GHz based on the same transmission line length. The insertion loss of

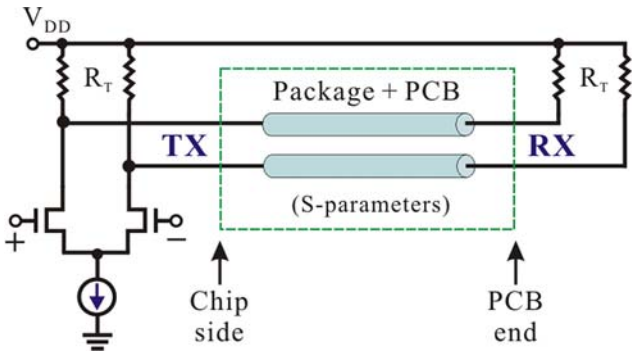

Fig. 10 Co-simulation topology of multi-Gbps serial link using chip SPICE model and package/board S-parameters ($R_T = 50\ \Omega$)

E-pad LQFP is −4.4 dB at 15 GHz and a resonance is occurred at 5.2 GHz, where the insertion loss is increased to −3.5 dB. The E-pad LQFP256 package has little margin for the electrical specification of serial ATA Gen2 that requires the maximum return loss for −6 dB in 1.2–2.4 GHz.

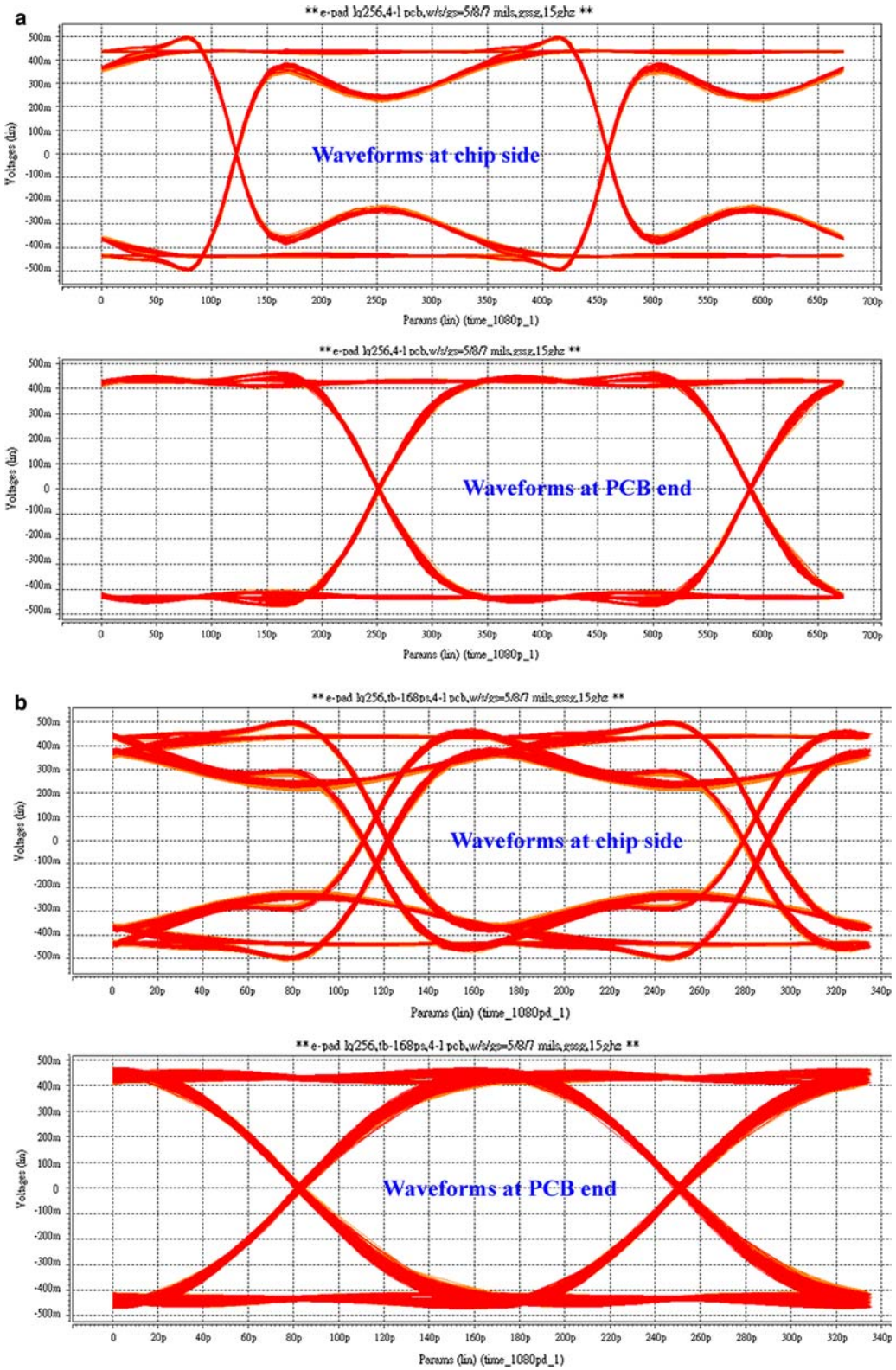

Fig. 11 Output eye-diagrams of dual channels in E-pad LQFP256 package. **a** 2.97 Gb/s and $T_b = 336.7$ ps. **b** 4.75 Gb/s and $T_b = 168$ ps

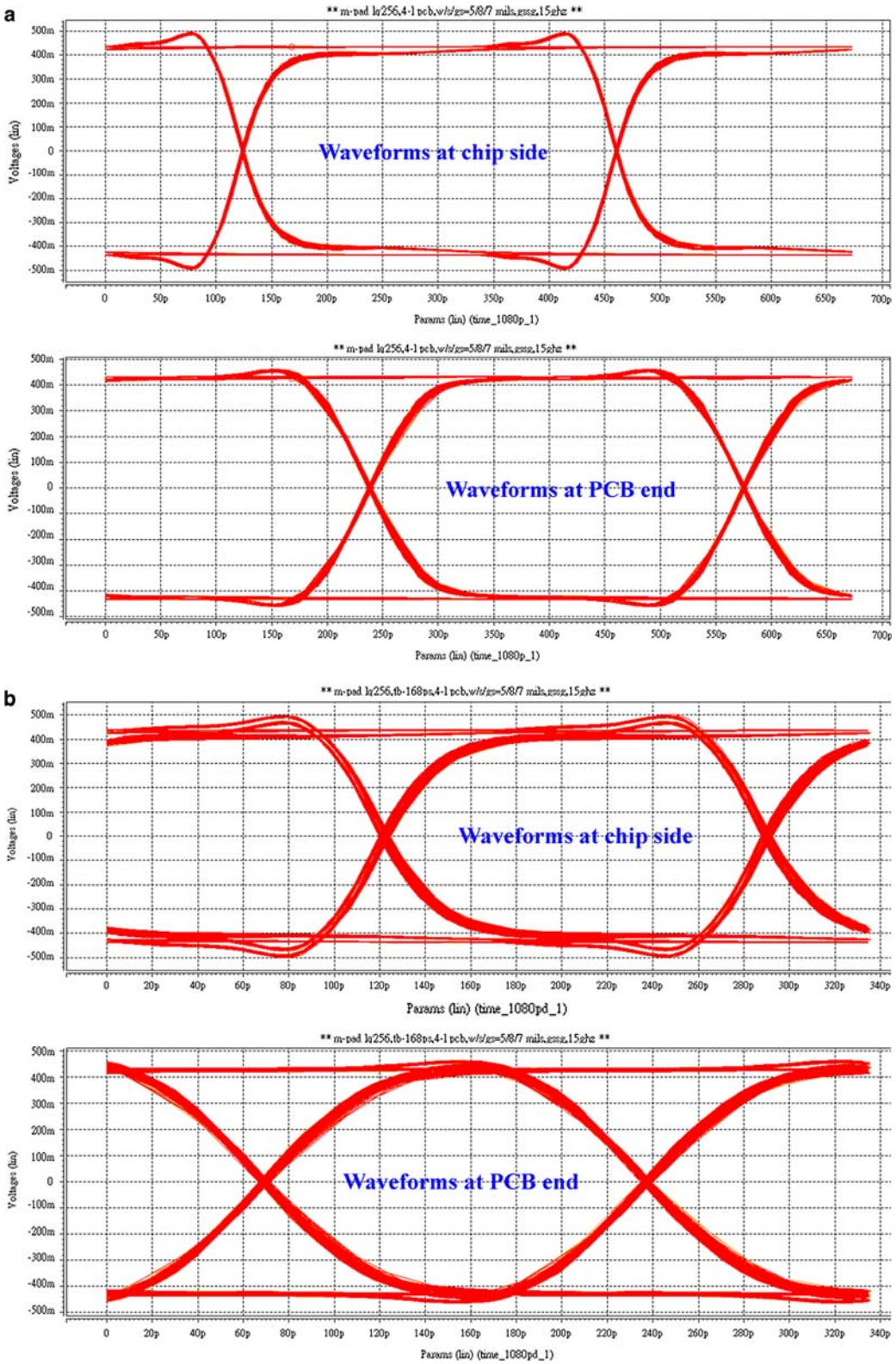

Fig. 12 Output eye-diagrams of dual channels in M-pad LQFP256 package. **a** 2.97 Gb/s and $T_b = 336.7$ ps. **b** 4.75 Gb/s and $T_b = 168$ ps

5 Co-simulation of multi-Gbps serial link

The above S-parameters with 15-GHz bandwidth were adopted for the co-simulation with the chip SPICE model, a HDMI using the TSMC 90-nm process, and the topology is illustrated in Fig. 10. Two channels of serial link were simulated at 2.97 and 4.75 Gb/s, and their bit times (T_b) are 336.7 and 168 ps, respectively. The transient analysis is in 1 μs. Figures 11 and 12 show the output eye-diagrams at chip side and PCB end for E-pad and M-pad LQFP256 packages, respectively. The results indicate that both packages can meet the eye diagram requirements of HDMI specification (HDMI Licensing, LLC 2006) at PCB end, but the E-pad LQFP256 package has worse eye-diagrams at chip side due to its large return loss causing large reflective waveform.

6 Conclusions

The cost effective M-pad leadframe package was evaluated without changing the conventional leadframe manufacturing and assembly processes significantly. Smaller power parasitics and signal loss were evaluated and achieved for multi-Gbps serial links with perfect eye diagrams due to shorter electrical paths in the package. With implementation of the M-pad structure in the leadframe package, it is no longer a low-level package. It could be a versatile package and contributes the consumer electronic market for another half century!

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