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A fast-locking agile frequency synthesizer for MIMO dual-mode WiFi/WiMAX applications

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Abstract In this paper, a wide-range and fast-locking phase-locked loop (PLL) frequency synthesizer using the band selection technique for the agile voltage-controlled oscillator (VCO) is proposed. The minimum time for band selection, discretely tuned by a time-to-voltage converter, can reach four times of the reference period. In addition, a current-enhanced circuit applied to the PLL can make settling behavior faster. The synthesizer is implemented in a 0.13-μm CMOS process, which provides the range from 4.6 GHz to 5.4 GHz with the phase noise of −106 dBc/Hz at 1-MHz offset. Combining the fast-locking techniques, the lock time of the synthesizer can be less than 13.2 μs and consume 39 mW from a 1.2-V power supply.

Keywords Frequency synthesizer · Phase-locked loop · Time-to-voltage converter · Fast locking · Voltage-controlled oscillator · Phase alignment

1 Introduction

Recently, the market for broadband wireless communications has generated increasing interests in the Worldwide Interoperability for the Microwave Access (WiMAX) technology. It is a developing trend for integrated low-cost dual-mode transceivers to provide seamless connectivity for mobile users as they roam between WiMAX and WLAN standards. Referring to [1, 2], the receiver requirements for these two standards are similar, and a dual-mode transceiver for WiMAX and WLAN can provide more flexibility and lower cost. In order to generate a pure LO signal with a reasonable gigahertz frequency range, a single-chip PLL-based frequency synthesizer with low power and low cost in CMOS technology is preferred. To synthesize both bands of 2.4-GHz and 5-GHz applications, however, the challenge existing in this dual-mode system specification is that the LO frequency hopping time is restricted in a limited lock time (10 μs) and a wide tuning range (4.6–5.4 GHz).

PLLs for wide-band systems typically require a wide frequency tuning range to cover the desired bands and to overcome process, voltage and temperature (PVT) variations. It is a practicable way to adopt both discrete and continuous tuning mechanisms in the VCO design to achieve a wide frequency tuning range with low gain. This can be implemented with multiple overlapped tuning bands to cover the desired frequency range, instead of using just one single frequency tuning curve which might seriously degrade the VCO noise performance.

However, a wide-frequency range leads to the difficulties in the PLL locking behavior. Both discrete and continuous tuning methods are generally needed in the wide-band designs. In recent works, the coarse-tuning capacitive technique is applied to the VCO, controlled with an up/down counter by the comparison logic circuit to determine the switch positions of the capacitor array network in the VCO. As mentioned in [3, 4], the search for the proper capacitor array state to represent the target frequency curve is based on frequency comparison as PLL is locking. The VCO frequency is compared to the lower and upper threshold frequencies with a voltage definition to determine whether to update the counter or not. Owing to the repeated

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locking process and repeated checking when the PLL settles in a specified frequency sub-band, the technique would take lots of reference cycle to complete the discrete tuning, owing to the repeated PLL locking process and repeated checking when the PLL settles in a specified frequency sub-band. In [5], the control voltage of the VCO is connected to a reference voltage at first, usually the half of the supply voltage. Then the counter begins to calculate the reference and the divided frequency cycles, and some judgments are done after a specified time. In another way, the counter accumulates the reference and the divided frequency cycles until one of the counters overflows, the frequency differences between them can thus be estimated. This process is repeated until a certain selection criterion is satisfied and a long settling time is required to ensure the accuracy of band selection process. In [6], a mixed-signal VCO whose frequency and the divider division ratio are co-related under digital pre-coding process, and then the VCO frequency can be preset by a digital signal depending on the divider ratio. A directly and accurately fast-settling PLL synthesizer with a direct frequency-presetting function can be realized at the cost of frequency presetting. In [7], an agile coarse tuning PLL architecture was represented. The instant measurement of the period converts to voltage accelerated the tuning process. A dual-edge phase detector complicates the design and additive switching noise is injected into the circuit, but degrades the accuracy.

In this work, a proposed coarse tuning technique is reported to simplify the design complexity, which will be described in detail in the following sections. In Sect. 2, the proposed coarse tuning technique is presented, and the proposed frequency synthesizer is described in detail. The circuit implementation of the frequency synthesizer and the experimental results are summarized in Sect. 3.

2 Frequency synthesizer architecture

2.1 Operation of the proposed time-to-voltage converter

Frequency detecting in time is the most important and critical part of the PLL's coarse tuning. Since the cost of the operation time to determine the frequency comparison results dominates the coarse tuning duration, a straightforward method to compare the signal frequency is employed to measure the period. The proposed circuit can efficiently makes real-time translation. The mechanism for frequency coarse tune applies a time-to-voltage converter (TVC) to achieve time-domain frequency detection. Based on the idea in [7], some effort is added to improve the mechanism with a simplified and effective architecture. The circuit diagram and the principle of the proposed TVC are shown in Fig. 1.

Illustrated in Fig. 1(a), the TVC provides an approach that measures the period differences between the reference (F_{ref}) and the divided (F_{div}) signals. Timing diagram is shown in Fig. 1(b), where the aligned phase is generated by the phase selecting circuit. The high state (Aligned Phase = 1) represents the period of the reference signal divided by four. The reference and the divided signal are divided by an even number to make sure the duty cycle is 50%. Therefore, the positive or the negative duration would be a specified integer times of a signal's period. In this case, the divided ratio of four is related to the phase alignment circuit, as explained later. Two capacitors with equal capacitances are charged during the high states of the aligned phase and divided VCO period, respectively. By comparing the voltages on the capacitors after different charging duration, the comparison result determines whether the digital down counter accumulates or not. The voltage difference after the charging process can be calculated by:

$$\Delta V = V_{\text{out\_ref}} - V_{\text{out}} = T\frac{I}{C} - (T + \Delta T)\frac{I}{C} = -\Delta T\frac{I}{C} \quad (1)$$

where T and $(T + \Delta T)$ are the durations as the aligned phase and $F_{\text{div}}/4$ are high, respectively. Equation 1 shows that the capacitor and the charging current decide the voltage difference at the inputs of the comparator. Thus, the frequency difference in the time-domain can be translated to voltage. Since charge pump current (I_{cp}) and capacitor (C_{t}) for the coarse tune loop can be considered as

$$I_{\text{cp}} = C_{\text{t}}\frac{\mathrm{d}V}{\mathrm{d}t} \text{ or } V = \frac{I_{\text{cp}}}{C_{\text{t}}}t + V_{\text{dc}} \quad (2)$$

the voltage difference between the outputs of time-to-voltage converter can be represented as

$$\Delta V = (V_2 - V_1) = \frac{I_{\text{cp}}}{C_{\text{t}}}(t_2 - t_1) = \frac{I_{\text{cp}}}{C_{\text{t}}}\Delta t \quad (3)$$

Assuming the charge (or discharge) duration is determined for about 25 ns operating at the 40-MHz reference clock, a proper voltage level for comparator can be determined as $\Delta V = 0.8$ V, and then $I_{\text{cp}}/C_{\text{t}} \approx 3.2 \times 10^7$ A/F. Thus, the charge pump current and the capacitor for the coarse tune loop can be determined. In this case, $I_{\text{cp}} = 96$ μA and $C_{\text{t}} = 3$ pF are chosen for the area, power, and noise consideration. If I_{cp} is selected too small that leads the TVC circuit to be noise sensitive. The voltage difference in the proposed TVC circuit applies the dual-edge phase detector to generate the phase difference. However, the digital switching noise is reduced in the proposed architecture, and that is not so sensitive owing to the comparator input offset.

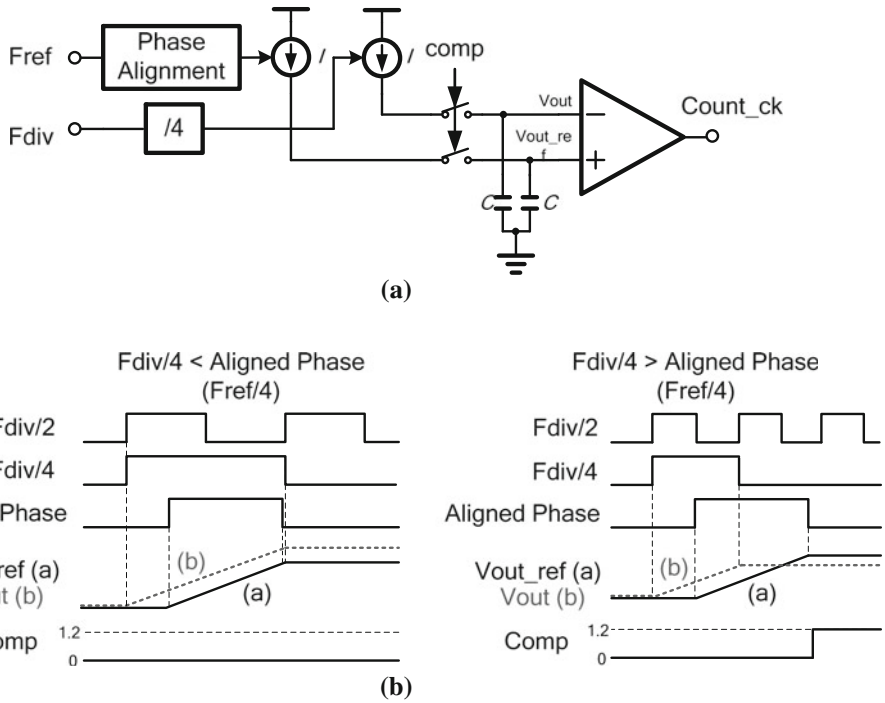

Fig. 1 Principle of the proposed TVC **a** simplified scheme, and **b** timing diagram

The detail operation of the TVC can be recognized from Fig. 2. By converting the time-domain aligned phase of F_{ref} and $F_{div}/4$ to control the current sources, the capacitors are charged and the timing duration difference between the inputs can be represented as the voltage difference on the capacitors. The timing control signals, $\Phi_{hold(1,2)}$, control the switches between the current sources and the capacitor. When the switches are under "ON" state, the current sources controlled by the durations of the reference signal and the divided signal feed current into the capacitor, respectively; otherwise, hold the result of the TVC circuit output. Φ_{comp} is used to control the dynamic of the comparator. When Φ_{comp} is high, the comparator compares the voltage value of the two inputs and outputs a digital signal to determine the frequency comparison result; otherwise, the result of the comparator is reset to ground. The control signals, $\Phi_{rst(1,2)}$, determine the reset operation of the voltage on the capacitor and wait for the next comparison. The proposed TVC applies fully differential architecture to reduce common mode noise, and thereby the timing errors typically can be at least 10 times smaller than that in the single-ended case. Figure 2(b) shows the timing diagram of the TVC. As can be seen, when voltage value of V_{c_div} is lower than V_{c_ref}, i.e., F_{div} is larger than F_{ref} in frequency-domain, the comparator generates a pulse to stop the digital down counter accumulating.

Furthermore, in order to achieve the high resolution performance between the comparison results and improve the timing accuracy, a current-mode voltage comparator is applied. The signal CLK latches the output results from input data dependence, which must be carefully designed for determining small voltage differences, as illustrated in Fig. 3.

2.2 Phase alignment circuit

To operate correctly in the frequency and phase detection with the TVC circuit, the rising edge between the reference and divided VCO output requires a proper phase relationship. Assuming the duty cycle of the input reference clock is 50%, the phase alignment circuit is illustrated in Fig. 4(a). Eight-phase signals, $ph1 - ph8$, are generated by a divided-by-4 circuit, and signals $np1 - np8$ can be synthesized with $ph1 - ph8$ phases. The signals, $np1 - np8$, behave as detection windows that determine where the rising edge of the $F_{div}/4$ signal is. If the rising edge of the $F_{div}/4$ is detected by the detection window $np(x)$, then the signal $ph(x + 1)$ is selected as the output signal $f1$ (as shown in Fig. 4(a)) that can be realized with digital logic circuits.

The phase alignment circuit makes the aligned phase $f1$ lag the $F_{div}/4$ by 0–45°, as shown in Fig. 4(b). This phenomenon is realized by taking the advantage of the multi-phase characteristics of the divided-by-4 divider. As the rising edge of the $F_{div}/4$ happens at the border between the $np(x)$ and $np(x + 1)$, there would be glitches occurred at the aligned phase. In order to eliminate the glitches and avoid the TVC circuit operating near dead zone region, a D-type flip flop triggered by the reference clock can be

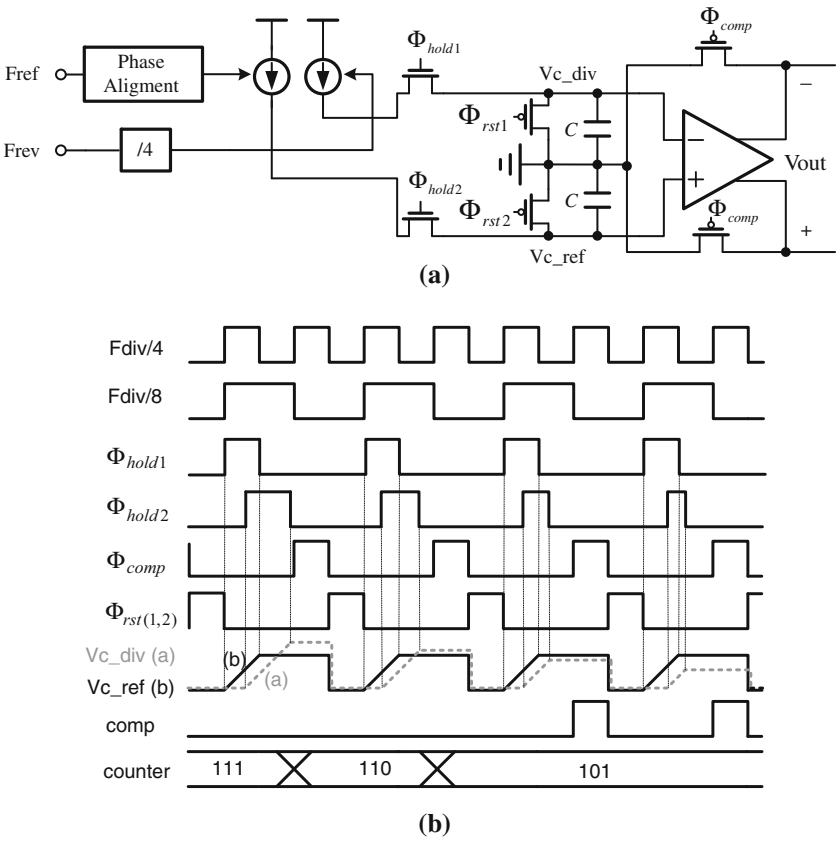

Fig. 2 Detail operation of the TVC **a** circuit diagram and **b** operation principle

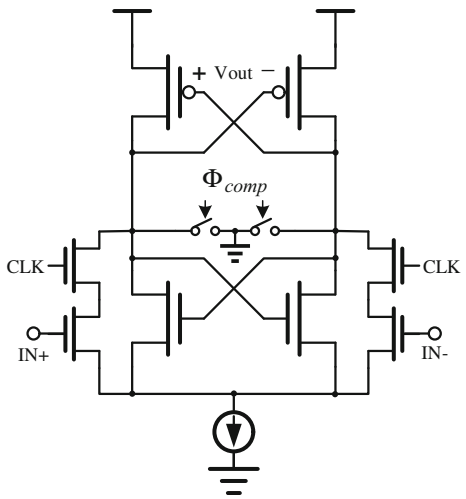

Fig. 3 Current-mode comparator

added at the output, to eliminate the glitches caused by the critical timing. Therefore, the aligned phase is now lagging by 90–135°. In this design example, $F_{ref}/4$ is lagging $F_{div}/4$ by 90–135°. The phase alignment circuit behaves as an open-loop circuit, which is unconditionally stable, and will not degrade the TVC performance.

2.3 Frequency synthesizer architecture

The specification for dual-mode WiMAX and WiFi requires a quite limited time (13.2-μs) for frequency hopping. The traditional method with a frequency discrete coarse tune mechanism is adopted, but it needs lots of reference cycles for the counters to accumulate as mentioned before. For example, the PLL must settle before a valid control voltage value in the VCO that can be read to make voltage comparison [3, 4]. In the other case [5], the counter must accumulate a sufficient amount of counts to ensure certain calibration accuracy.

The proposed frequency synthesizer architecture is shown in Fig. 5, which can be applied in a direct down conversion RF architecture. For the system applications, 2.4-GHz band oscillating signals can be generated by the divided-by-2 circuit from the VCO output, and that can meet 2.3−2.7 and 5-GHz frequency bands of the WiMAX standard. Therefore, both 2.4 and 5 GHz for WLAN and the WiMAX standard are met, and frequency channels can be generated by delta-sigma modulated divider. The associated timing diagram is illustrated in Fig. 6.

The synthesizer architecture consists of a PLL and a discrete coarse frequency-tuning mechanism. The coarse

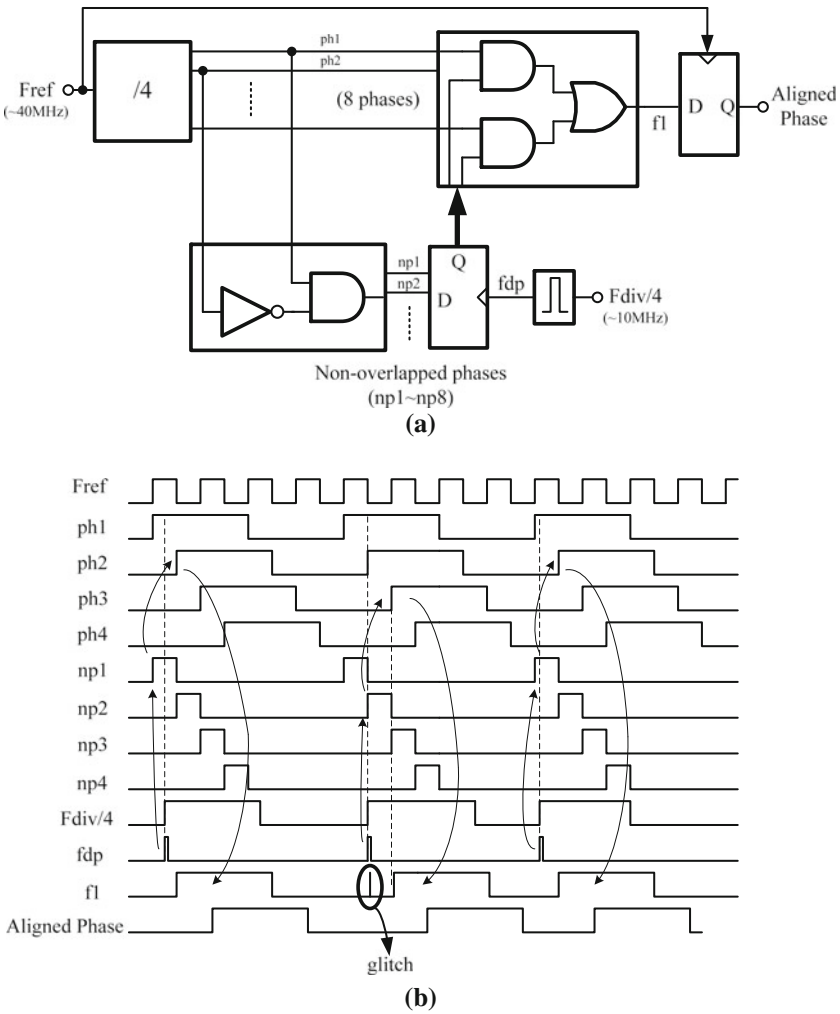

Fig. 4 **a** Circuit implementation of the phase alignment, and **b** operation principle

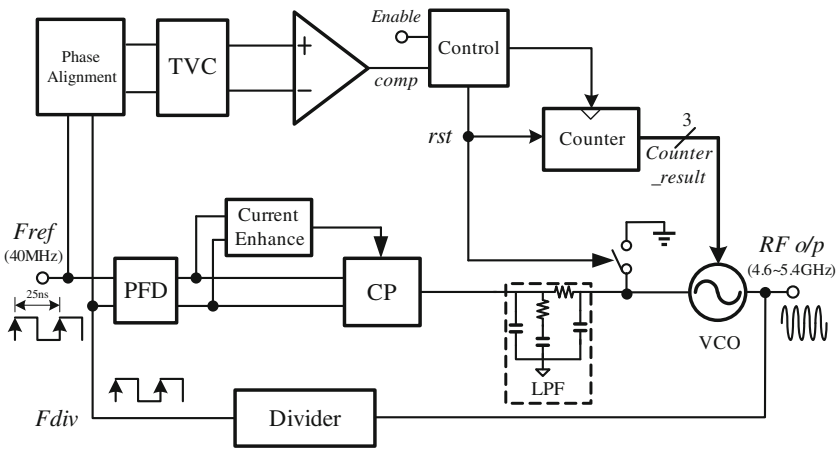

Fig. 5 Proposed frequency synthesizer architecture

tuning is achieved with the phase alignment circuit and the TVC circuit. The PLL employs a current-enhanced circuit to perform a non-linear adaptive bandwidth characteristic to reduce the settling time for fast locking purpose, as discussed later. The Enable signal resets the rst signal to trigger the coarse tune mechanism. The phase alignment

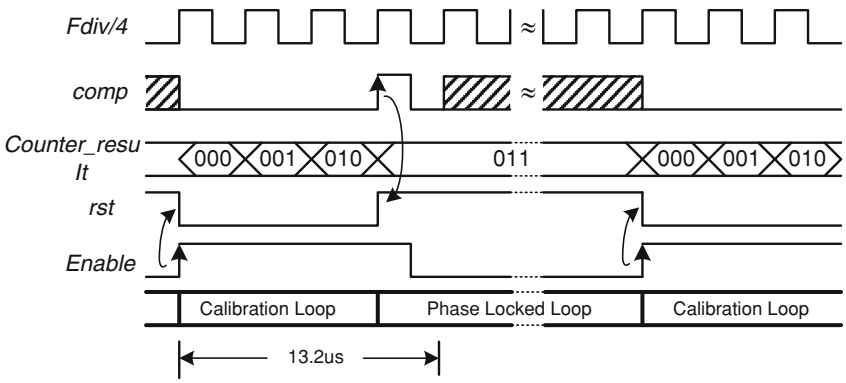

Fig. 6 Timing diagram of the proposed frequency synthesizer

circuit generates the $F_{div}/4$ and the phase aligned reference, and then the TVC circuit starts to convert the period time of them into a voltage level with the duration of around 0.1-μs (10 MHz). Furthermore, as the timing diagram mentioned in Fig. 2(b), the minimum coarse tune time is 0.2 μs for each sub-band selection. When the correct band is selected, the comparator outputs a comp signal and triggers rst to high level. The PLL then begin settling until the next enable signal triggers. Considering the PLL settling behavior, the VCO control voltage is set corresponding to the highest frequency in each sub-band.

The PLL can be extended to a fraction-N frequency synthesizer for direct conversion RF architecture. In order to achieve fine resolution of the LO frequency steps, a delta-sigma modulator (DSM) can be used. A DSM is applied to provide fraction divisions. However, the coarse tune mechanism proposed here is a real-time period detection. The DSM principle is the average of an amount different integer division clock cycles. DSM cannot operate during coarse tune duration. Therefore, the DSM is able to be turned on as the coarse tune process finishes.

2.4 VCO and frequency divider

The VCO is one of the most important components in the frequency synthesizer. Two of the most important design targets are the frequency tuning ability and the low-phase noise performance. In this work, we need a wide-tuning range to meet the dual-mode WiMax and WiFi specifications. A 3-bit capacitor array and a varactor are implemented to cover all the frequency bands. The VCO architecture is shown in Fig. 7. The 3-bits digital binary capacitor array is employed for coarse tuning controlled by the TVC circuit, and the capacitive varactor is used for fine tuning by the PLL mechanism. The transistor, MB_2, operates as the current source of the VCO, and its length and width are designed with large dimension to reduce 1/f noise. R_1 and *Mnc* form a low-pass filter to reduce current source noise, and *Cs* couples the VCO output second harmonics to ground to reduce noise. A symmetric inductor is applied for the design symmetry.

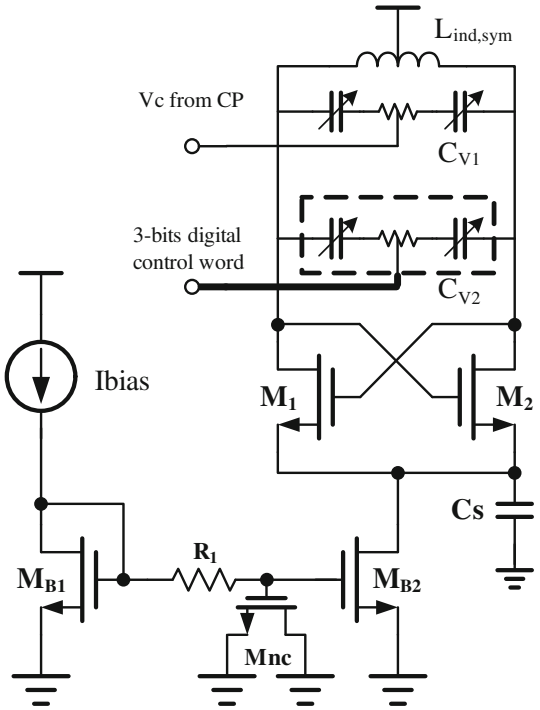

Fig. 7 VCO

Table 1 comparatively presents important architectures of high-speed frequency dividers. F_{DFF} is the D flip-flop's toggling speed, and F_{VCO} is the resonant tank's self-oscillating frequency. The conventional divider maximum operating speed by the first prescaler stage, as $1/2F_{DFF}$, is limited. The injection-locked type frequency divider is restricted to its narrow operation range. Figure 8 shows the divided-by-113 ~ 143 frequency divider. The phase-rotated type frequency divider is applied to ease the operating speed of the first divider stage. The MSB of the control bits, D_4, decides the direction of phase rotation. The other bits control the times of phase rotations in an F_{vco}/N cycle. A D-flip flop is added in the phase selector circuit to avoid the glitches caused by the phase switching architecture [8].

Table 1 Comparison of frequency divider architecture

Divider architecture	Conventional	Phase-rotated	Injection-locked
Operating speed	$1/2F_{DFF}$	F_{DFF}	F_{VCO}
Power dissipation	High	Medium	Low
Programmability	Best	Good	Bad
Operating range	Large	Large	Small

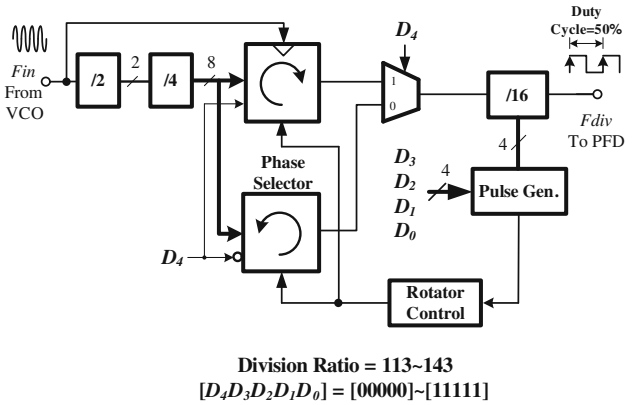

Fig. 8 Architecture of the frequency divider

2.5 Current-enhanced circuit

When the discrete coarse tune process is done, the PLL initially begins to lock onto the input signal. In the beginning, the input phase may differ from the output phase significantly. The PLL settling speed may degrade due to the initial condition of the phase difference between the reference and divided VCO signals. In this case we make the charge rate of the charge pump exceed the original charge rate. The increased voltage on loop filter makes PLL loop bandwidth widen and thus achieves fast lock. However, increasing the charge pump current may lead the PLL system to an unstable condition [9].

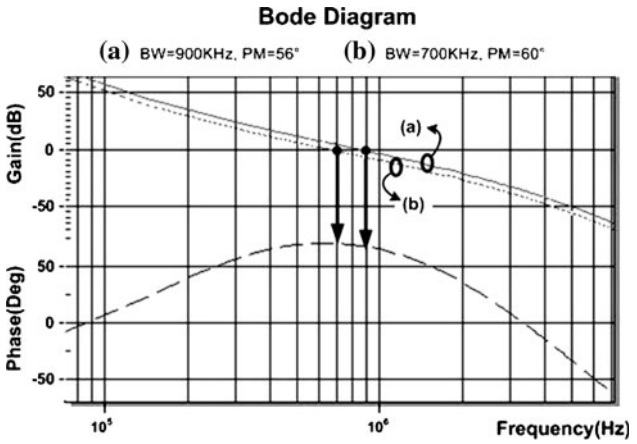

Fig. 9 Bode plot of the PLL

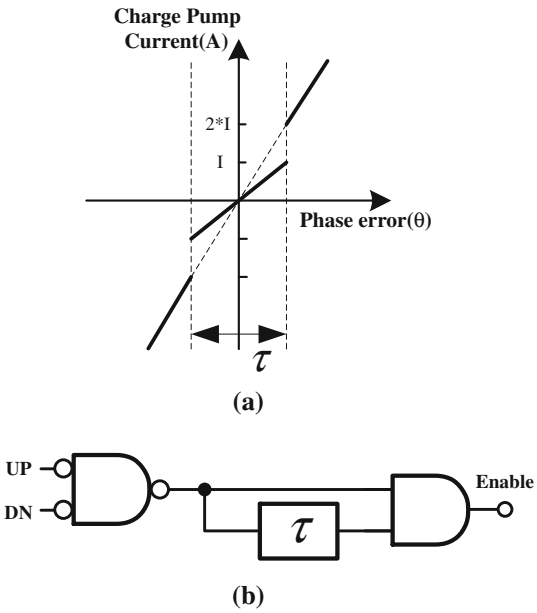

Fig. 10 Concept of current-enhanced operation **a** characteristic of the phase detector, and **b** control circuit

Seen from a third-order PLL open-loop transfer function, which can be represented as

$$G(s) = \frac{I_{cp} \cdot K_f \cdot K_{vco}}{N} \cdot \frac{s + \omega_z}{\frac{1}{\omega_p} s^3 + s^2} \tag{4}$$

where $K_f = \frac{R_p \cdot C_p}{C_p + C_s}$, $\omega_z = \frac{1}{R_p \cdot C_p}$, and $\omega_p = \frac{1}{R_p} \cdot \frac{C_p + C_s}{C_p \cdot C_p}$. I_{cp} is the charge pump current, K_{vco} is the gain of the VCO, N is the division ratio, and R_p, C_p, C_s are the passive elements of the loop filter that provide poles and zeros for the PLL system stability. The phase margin of the open-loop transfer function can be represented as

$$\text{PM} = \tan^{-1} \frac{K}{\omega_z} - \tan^{-1} \frac{K}{\omega_p} \tag{5}$$

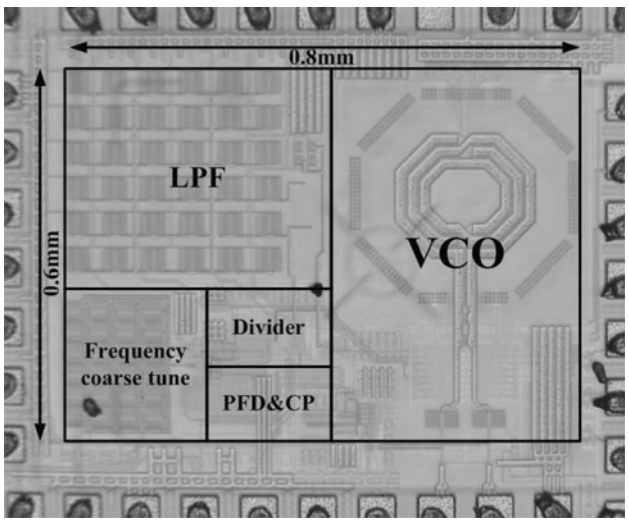

Fig. 11 Photograph of the test chip

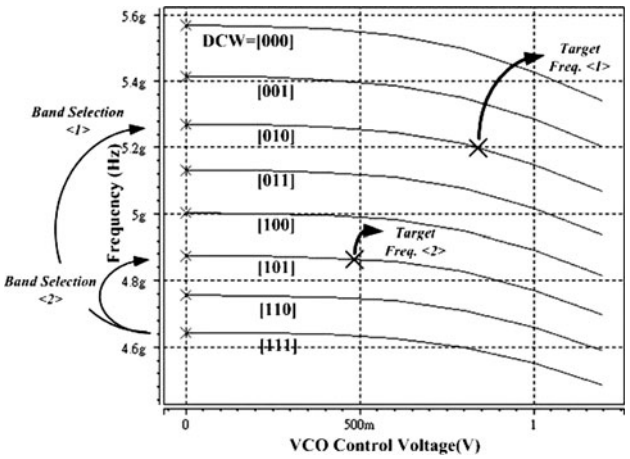

Fig. 12 Tuning characteristic of the VCO

K is the dc gain of a third-order PLL open-loop transfer function as shown in 4. The current-enhanced circuit injects additional current into the loop filter when the phase difference is large. If double current is provided, K will become double and the phase margin may degrade. Furthermore, with an open-loop analysis, Bode plot of the PLL is shown in Fig. 9. Curve (a) shows the characteristics of the PLL with the current-enhanced circuit. The PLL will return to curve (b) when it is near in lock. These curves provide the phase margin close to 60°, and PLL would be stable. In this design example, the loop bandwidth increases from 700-KHz to 900-KHz, and the phase margin degrades from 60° to 55°. The phase margin during the current-enhanced mode must be design carefully for stability. The injected current should be chosen not too much, in this case, the injected current is the same amount as the PLL charge pump current.

In the phase tracking mode, the phase difference between input and output is small. Figure 10(a) shows the characteristic of phase detection in this work, where time delay τ is designed as a detection window. As the phase difference is smaller than τ in Fig. 10(b), the current-enhanced circuit shuts down, and the PLL exhibits original loop bandwidth. The logic circuit would determine whether the PLL phase different is within this window or not. In this

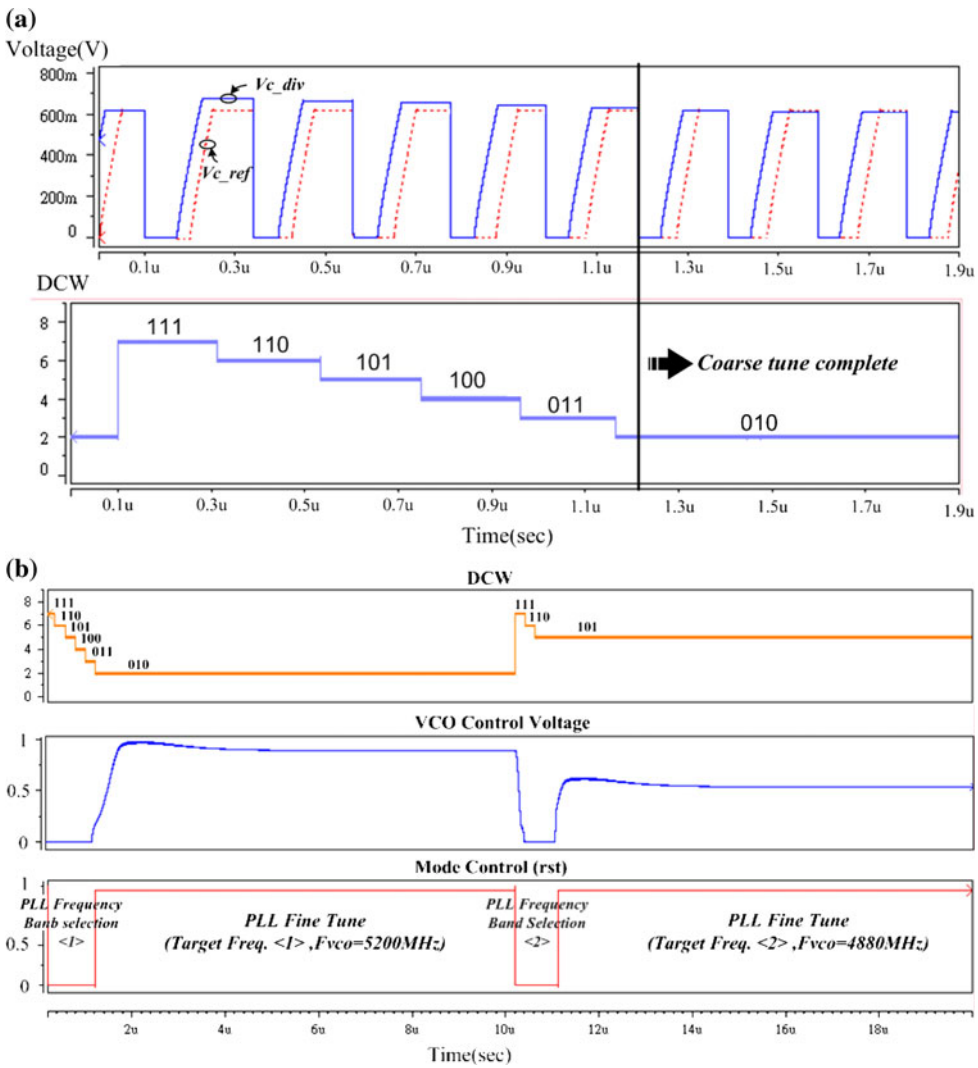

Fig. 13 PLL simulation **a** frequency coarse tune simulation, and **b** transient simulation

design, we make charge pump current double in large phase difference case to accelerate PLL settling time [10].

3 Simulated and measured results

The chip has been fabricated in the TSMC 0.13-μm 1P8 M standard CMOS process. The micrograph of the test chip with a die area of 0.8 × 0.6 mm^2 is shown in Fig. 11. In this design, frequency coarse tuning duration and the settling time of the frequency synthesizer must be limited in 13.2 μs. Thus the loop bandwidth must be carefully designed in order to fit the timing restrictions. A third-order loop filter is designed for the PLL with 700-KHz loop bandwidth and 60° phase margin. Figure 12 shows that the VCO tuning range is from 4.6-GHz to 5.4-GHz. The wide frequency tuning range is separated to discretely coarse tuning and fine tuning. The 3-bits digital control word (DCW) represents each fine tune curve. Figure 13(a) represents the operation of the coarse tune. The beginning of the coarse tune DCW is set to 111, which corresponds to the lowest frequency sub-band. V_{c_ref} and V_{c_div} are the outputs of the TVC circuit as shown in Fig. 2. Reference clock and divided VCO signal both translate into voltage levels. The conversion process repeats as the counter accumulates until V_{c_div} down below V_{c_ref}. Each conversion duration is 1/8 reference clock, i.e., 200 ns each one coarse tune step.

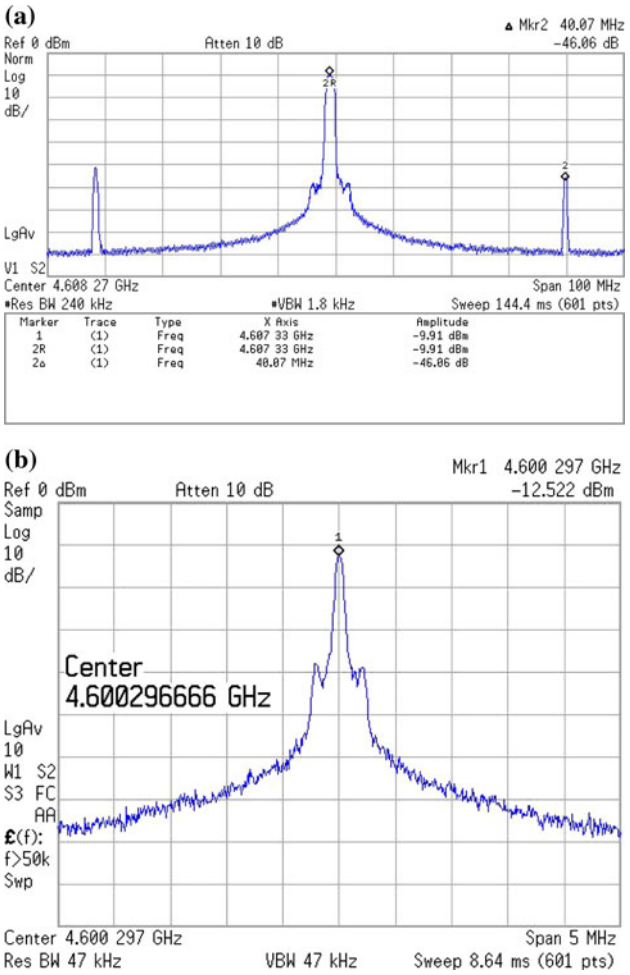

Fig. 14 PLL output spectrum at 4.6-GHz frequency **a** with 100-MHz span, and **b** with 5-MHz span

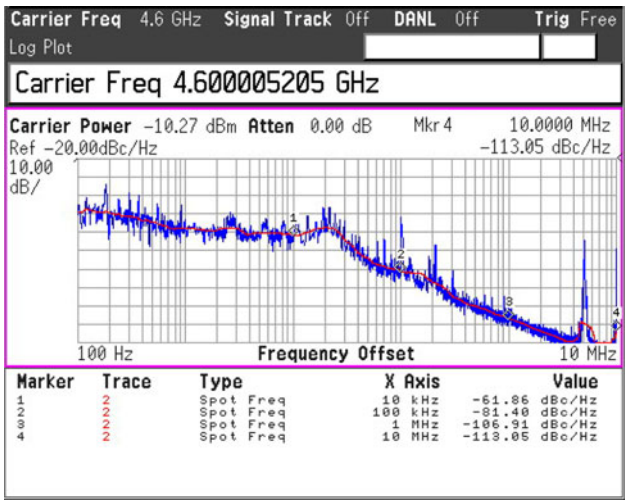

Fig. 15 Measured phase noise of the PLL at 4.6-GHz frequency

The frequency synthesizer closed-loop simulation is shown in Fig. 13(b). During frequency band selection period, DCW accumulates according to the result from the TVC circuit until the comparator generates a pulse, and the band selection mechanism completes. Afterwards, the frequency synthesizer switches to the fine tune loop, phase-locking operation in the PLL. Total operation duration can be completed in 10-μs. Figure 13(b) shows the output frequency hopping from 5200 MHz to 4880 MHz. Note that the 5200-MHz frequency is within the sub-band corresponding to the digital control word 010. Five times of coarse tuning duration is needed, and that costs 1-μs to

Table 2 Performance summary

Process	0.13-μm CMOS
Supply voltage	1.2 V
Frequency tuning range	4.6–5.4 GHz
Reference spurs	<−46 dBc
Phase noise	−106 dBc/Hz at 1-MHz offset
PLL coarse tune time	<3.2 μs
PLL locking time	<10 μs
Power consumption (at 4.6-GHz)	36 mW
PLL (VCO + Divider + PFD/CP + Buffer)	(8 + 13 + 3 + 12) mW
Coarse tune circuit	3 mW
Core size	0.8 × 0.6 mm^2

Table 3 PLL performance summary and comparison

	Technology	Frequency tuning range	Lock time	Chip size	Phase noise	Reference frequency	PLL bandwidth	Power consumption	Frequency band selection
JSSC, 2001 [3]	0.6-μm CMOS	820 ~ 1000 MHz	<2 ms	0.7 mm^2 (w/o IO)	−102 dBc/Hz at 100 KHz	125 KHz	120 KHz	7.5 mW	Closed-loop tuning
ISSCC, 2006 [5]	0.11-μm CMOS	90 ~ 770 MHz	>80 μs	1.9 mm^2 (w/o IO)	<−100 dBc/Hz at 100 KHz	48 MHz	N/A	18.59 mW	Auto-tuning
ISSCC, 2006 [6]	0.35-μm CMOS	560 ~ 820 MHz	<1 ms	0.4 mm^2 (w/o IO)	−85 dBc/Hz at 10 KHz	1 MHz	N/A	N/A	Frequency presetting
JSSC, 2007 [7]	0.18-μm CMOS	8.67 ~ 10.12 GHz	<7 μs	1.35 mm^2 (w/i IO)	−102 dBc/Hz at 1 MHz	40 MHz	670 KHz	44 mW	Agile calibration
This work	0.13-μm CMOS	4.6 ~ 5.4 GHz	<13.2 μs	0.48 mm^2 (w/o IO)	−106 dBc/Hz at 1 MHz	40 MHz	900/700 KHz	39 mW	Fast coarse tuning

complete. After that, an enable signal rising edge triggers the next frequency hopping to 4880 MHz. Three times of coarse tuning duration is needed, and so on. The worst case that coarse tuning mechanism steps from 111 to 000 can be accomplished in 3.2 μs.

The PLL is measured with a 1.2-V supply voltage and the power consumes is 39-mW. The coarse tune circuit consumes about 3-mW. Figure 14(a) shows the measured frequency spectrum at 4.6-GHz frequency. The reference spur is measured −46 dBc at 40-MHz offset with the signal power of −9.91 dBm. Figure 14(b) shows the 5-MHz span frequency spectrum. Figure 15 shows the measured phase noise of the output spectrum. The phase noise measured at 4.6-GHz frequency is about −107 dBc at 1-MHz offset. Generally, the in-band sources dominate within the loop bandwidth and the VCO noise dominates outside of the loop bandwidth [11]. The phase noise (Fig. 15) measured at an offset that is close to the carrier is basically independent of the loop bandwidth, provided that the loop bandwidth is sufficiently wide to eliminate the VCO noise. In this work, however, the close-in spurious may be caused by the frequency divider. The phase-rotated architecture somehow induces switching noise and should be reduced as possible. Table 2 summarizes the performance of the proposed PLL, and Table 3 shows the comparison with the prior works.

4 Conclusion

A frequency synthesizer for dual-mode WiMax and WiFi applications with agile frequency tuning mechanism is proposed. A current-enhanced circuit is employed to accelerate PLL transient response. To achieve fast locking, a mechanism constituting phase alignment and TVC to establish the frequency band selection, and then a fine-tuning work is completed by the PLL. The overall response time can be under 13.2 μs. The frequency synthesizer was simulated in 0.13-μm CMOS process, and the power consumption is 39 mW from a 1.2-V supply.

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