LETTER

Injection-Locked Clock Recovery Using a Multiplexed Oscillator for Half-Rate Data-Recovered Applications

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SUMMARY An injection-locked clock recovery circuit (CRC) with quadrature outputs based on multiplexed oscillator is presented. The CRC can operate at a half-rate speed to provide an adequate locking range with reasonable jitter and power consumption because both clock edges sample the data waveforms. Implemented by 0.18-μm CMOS technique, experimental results demonstrate that it can achieve the phase noise of the recovered clock about −121.55 dBc/Hz at 100-kHz offset and −129.58 dBc/Hz at 1-MMz offset with ±25 MHz lock range, while operating at the input data rate of 1.55 Gb/s.

key words: *clock recovery, data recovery, injection-locked oscillation*

1. Introduction

Clock and data recovery (CDR) circuits are a key component of optical transmission receivers. The CDR generally consists of a clock recovery circuit (CRC) for realizing retiming, and a decision circuit for realizing regeneration. A common CRC configuration employs a nonlinear technique by a differentiator, a limiting amplifier and a high-Q filter such as a resonator filter. Such CRCs have a simple circuit configuration but the filter is difficult to integrate with other circuits. Actually, the CRC can be viewed as a voltage-controlled oscillator (VCO) with injection lock and tunable operation [1], [2]. Thus, this CRC structure can be implemented by a matched gated oscillator which utilizes an edge detector and a gated ring oscillator [3]–[5]. The oscillators suffer from a limitation, however, in that the phase error is accumulated and data decision errors consequently occur. The other configuration uses the phase-locked loop (PLL) technique, which is widely used for communication ICs but needs longer locked time than above ones.

In this letter, we combine the gated oscillator by using a multiplexed-type oscillation technique and the PLL into the CRC structure [6]. Some features of the proposed scheme are summarized in the following.

1) A CRC generally synchronizes a clock to the data, so the clock frequency equals the data rate. However, it may be difficult to design a very high-speed oscillator that provides an adequate tuning range with reasonable jitter. For this reason, the proposed CRC can sense the input data at full rate but employ an oscillator running at a half input rate [8].

2) The conventional structures usually need an edge detector to generate a pulse output to realign the oscillator while the input edge occurs. Without an edge detector, the proposed CRC can directly active through NRZ data as well as save the power dissipation to align the oscillation.

3) The synchronized oscillator is a quadrature structure, which produces outputs have a phase difference of 90° [9].

4) A PLL is combined with the proposed CRC to achieve a wanted frequency in the present of temperature and process variations.

2. Circuit Configuration

2.1 Basic Concepts

Figure 1(a) shows a conceptual schematic and time chart of the conventional CRC, which consists of an edge detector and a free-running oscillator. The edge detector converters the NRZ data to a RZ-like data, and then recovery clock from that RZ-like data with an oscillator [3]–[5], [7]. In gated oscillation design, the RZ-like signal usually has a half of data period to introduce temporal phase errors in the output clock that are discard when data transition occurs. However, the pulse duration of the RZ-like signal becomes a critical issue because its variation introduces more jitter to the oscillator.

Without an edge detector to produce a RZ-like signal, Fig. 1(b) depicts the basic concept of the proposed CRC. The principle of operation is to stimulate an oscillator by an input NRZ signal where the input frequency is close to the free running one. Then the oscillator will lock on this input reference for synchronization versus the clock. When

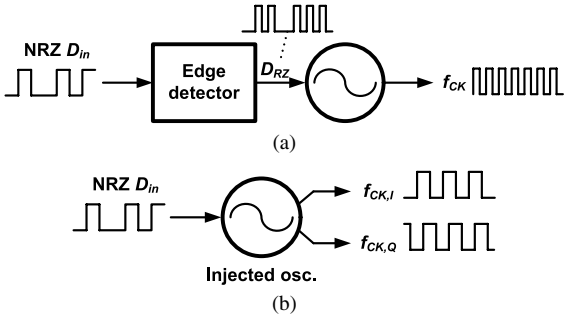

Fig. 1 (a) The conventional CRC, (b) concept of the proposed CRC.

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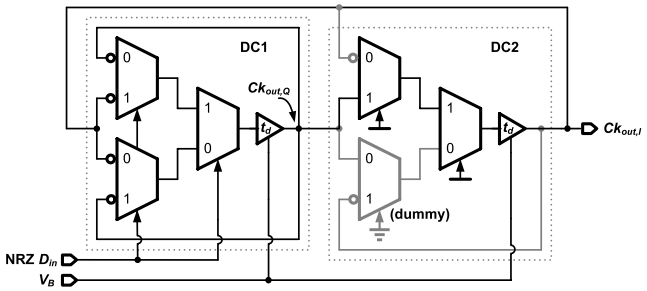

Fig. 2 Schematic of the proposed synchronized oscillator for clock recovery.

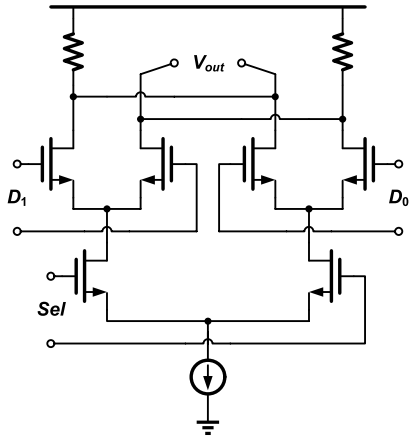

Fig. 3 2-to-1 multiplexer.

no data is delivered to the input data lines, the output clock is given by the free running frequency of the oscillator. In addition, the synchronized oscillator can provide quadrature outputs.

2.2 CRC Realization

Figure 2 shows the proposed CRC employing a multiplexed structure to implement the synchronized oscillator, which is a ring structure with two stages of delay cells (DC1 and DC2). Each delay cell consists of a multiplexed architecture and a voltage-controlled delay element. The input data is injected to DC1, while DC2 is a forward delay path with a matched circuit to DC1. As can be seen, the multiplexed oscillator consists of two paths which are selected according to the value of D_{in}. If D_{in} is "high," the upper path in DC1 is selected and the CRC operates as a ring oscillator, while the lower path feedbacks the information of $CK_{out,Q}$, and vice versa.

The CRC is a fully-differential scheme. Figure 3 shows the 2-to-1 multiplexer schematic, where two differential pairs sense the two inputs and convert the signals to current, and then apply the result to the load resistors. The approach to tuning the ring oscillator is based on interpolation [10]. As illustrated in Fig. 4(a), each stage consists of a path and a slow path whose outputs are summed and whose delay times are adjusted by V_C in opposite directions. At one

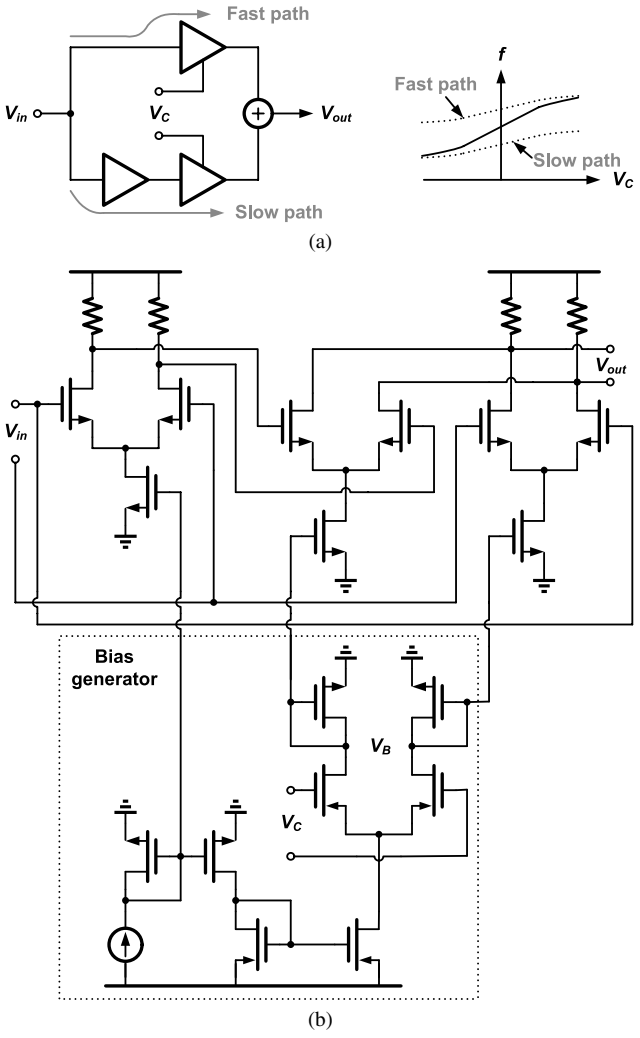

Fig. 4 Voltage-controlled delay cell: (a) Concept of interpolating delay stage, (b) schematic of the delay stage.

extreme of the control voltage, only the fast path is on and the slow path is disabled, yielding the maximum oscillation frequency. Conversely, at other extreme, only the slow path is on and the fast path is off, providing the minimum oscillation frequency. If V_C lies between the two extremes, each path is partially on and the total delay is a weighted sum of their delay. The detail schematic of Fig. 4(a) is shown in Fig. 4(b).

2.3 System Architecture

Since the lock range is typically quite narrow and since the free-running frequency of the oscillator incurs significant error due to process variations and poor modeling, the locking may occur near the edge of the lock range. Figure 5 shows the block diagrams of the CDR, which contains a PLL, a CRC and decision circuits. The CRC is performed to realign by injection locking the VCO to the input data signals. The oscillation frequency of the CRC is determined by the VCO of the PLL. Note that the VCO in the PLL is a replica

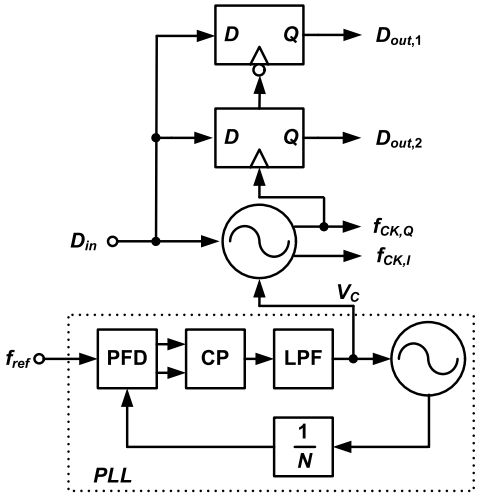

Fig. 5 System configuration of the CDR.

circuit of the CRC while no data transition appears at its input terminals. The PLL can provide a control voltage (V_C) to make the CRC generate a desired frequency.

3. Experimental Results

The CDR was fabricated in a 0.18-μm CMOS technique. Figure 6 shows the microphotograph with a chip area of $1360 \times 1175\,\mu\text{m}^2$. The tested circuit was measured under a supply voltage of 1.8 V, and power consumption is 25 mW. A serial data stream was generated by a pulse-pattern generator. The waveforms were derived from a digital oscilloscope and a spectrum analyzer for measurement.

The PLL employs a 1/64 frequency divider to synthesize the VCO's frequency from the external reference source. The PLL has a tuning range of around 650 to 800 MHz. Before injecting the data stream, the measured spectrum and phase noise of the free running VCO at around 775 MHz are shown in Figs. 7(a) and (b), respectively. The measured phase noise is −84.18 dBc/Hz at 100-kHz offset and −105.51 dBc/Hz at 1-MHz offset. As a 1.55-Gb/s pseudo-random binary data of $2^7 - 1$ is injected, the output spectrum of the CRC is shown in Fig. 8(a), which is slightly larger than the free-running frequency of Fig. 7(a). This is because the injected signal also feeds through the CRC to the output with phase alignment. Measurement also confirms that the spectrum remains symmetric but the sidebands rise in both magnitude and number [1]. The injection-locked phase noise is shown in Fig. 8(b), −121.55 dBc/Hz at 100-kHz offset and −129.58 dBc/Hz at 1-MHz offset, better than that in Fig. 7(b) [11]. The measured lock range is equal to ±25 MHz. To the retimed data, we add a decision circuit driven by the CRC output, and the eye diagram of the recovered data is shown in Fig. 9. The measured rms and peak-to-peak jitter is 14.7 ps and 101.5 ps, respectively. Table 1 gives the performance summary of the proposed CDR with those in the literature.

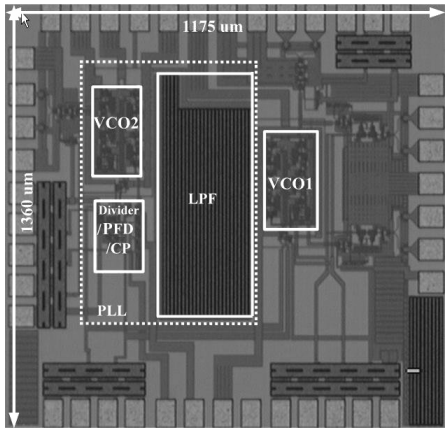

Fig. 6 Chip microphotograph.

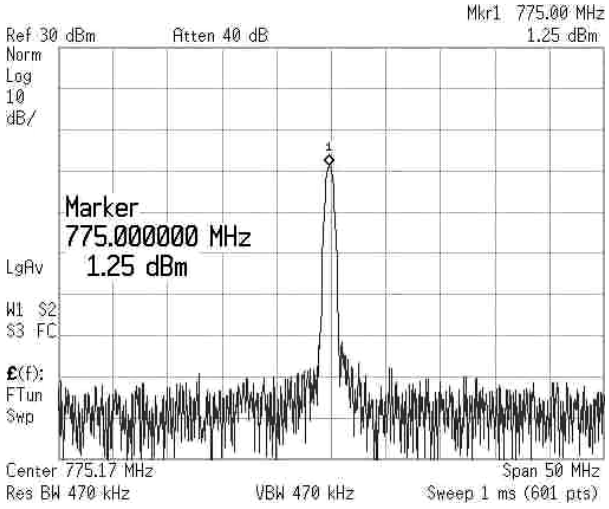

Fig. 7 (a) Measured spectrum and (b) phase noise of free-running CRC before injection.

4. Conclusion

The CDR with an injection-locked CRC fabricated in a 0.18-μm CMOS process is presented. Unlike the conventional structures employing an edge detector to produce RZ-like signals, the CRC can directly synchronize a clock to the data at a half rate and generates quadrature outputs. The measured results show that the CRC under data injection does achieve the injection-locked function as expected.

Table 1 CDR performance summary and comparison.

Reference	This work	[3]	[4]	[5]	[6]
Technology (CMOS)	0.18-μm	0.9-μm	0.35-μm	0.18-μm	0.18-μm
Supply voltage	1.8 V	5 V	3.3 V	1.8 V	1.8 V
Measured data rate	1.55 Gb/s	660 Mb/s	622 Mb/s	1.25 Gb/s	3.125 Gb/s
Recovered clock frequency	775 MHz	660 MHz	311 MHz	625 MHz	3.125 GHz
Power dissipation	28 mW	600 mW	130 mW	32 mW	80 mW
Jitter performance	Recovered data: $\Delta T_{r.m.s}$: 14.7 ps ΔT_{pk-pk}: 101.5 ps	N/A	PLL output: $\Delta T_{r.m.s}$: 11.35 ps ΔT_{pk-pk}: 76 ps	Recovered clock: $\Delta T_{r.m.s}$: 6.66 ps ΔT_{pk-pk}: 34.0 ps Retimed data: $\Delta T_{r.m.s}$: 12.27 ps ΔT_{pk-pk}: 40.0 ps	Recovered clock: $\Delta T_{r.m.s}$: 2.65 ps ΔT_{pk-pk}: 26.7 ps

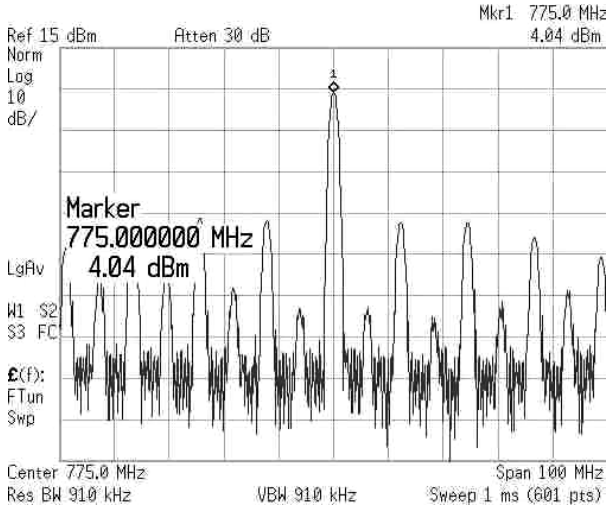

Fig. 8 (a) Measured spectrum and (b) phase noise of CRC under data injection.

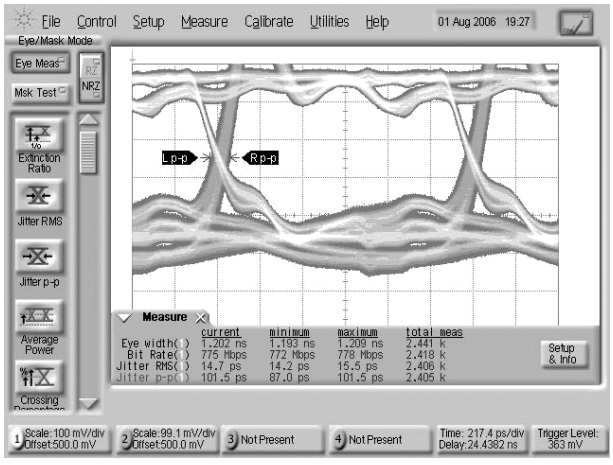

Fig. 9 Recovered data eye.

Acknowledgments

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