IEICE TRANS. ELECTRON., VOL.E90–C, NO.1 JANUARY 2007

LETTER

A 1.25-Gb/s Burst-Mode Half-Rate Clock and Data Recovery Circuit Using Realigned Oscillation

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SUMMARY In this letter, a 1.25-Gb/s 0.18-μm CMOS half-rate burst-mode clock and data recovery (CDR) circuit is presented. The CDR contains a fast-locking clock recovery circuit (CRC) using a realigned oscillation technique to recover the desired clock. To reduce the power dissipation, the CRC uses a two-stage ring structure and a current-reused concept to merge with an edge detector. The recovered clock has a peak-to-peak jitter of 34.0 ps at 625 MHz and the retimed data has a peak-to-peak jitter of 44.0 ps at 625 Mb/s. The occupied die area of the CDR is $1.4 \times 1.4\,\mathrm{mm}^2$, and power consumption is 32 mW under a 1.8-V supply voltage.

key words: *burst-mode CDR, clock recovery, phase-locked loop, realigned oscillation*

1. Introduction

Passive optical networks (PONs) utilizing burst-mode transmission and reception have been developed for numerous communication applications of digital telephony, local area and metropolitan networks, and computer interconnects. One of the key building blocks is the clock and data recovery (CDR) circuit, which requires fast-locking characteristics. The CDR generally consists of a decision circuit for realizing regeneration, and a clock recovery circuit (CRC) for realizing retiming. However, the traditional phase-locked-loop (PLL)-based CRC cannot be used for this burst-mode application because of needing long locking time.

There have been several reports for fast-locking CRCs including over-sampling techniques [1]–[3] and matched gated voltage-controlled oscillators (MGVCOs) [4]–[7]. The oscillators suffer from a limitation, however, in that the phase error is accumulated and data decision errors consequently occur. To significantly reduce the effect from phase errors, an oscillator realignment technique is developed in [9] and applied to a conventional PLL. The drawback is that it needs an external delay element to calibrate the loop path due to delay mismatch. This effect can be mitigated by open-loop application in this work. Similar to those of the CDR using MGVCOs, in the letter a burst-mode CDR with instantaneous locking as well as realignment characteristics is proposed. The CDR can extract a low-jitter clock signal by using the realigned technique on 1.25-Gb/s burst-mode operation. In addition, to reduce the operating frequency and provide an adequate tuning with reasonable jitter, the burst-mode CDR senses the input data but employs an oscillator running at a half input data rate.

Manuscript received July 6, 2006.
Manuscript revised August 28, 2006.

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DOI: 10.1093/ietele/e90–c.1.196

2. Basic Concept and System Architecture

2.1 Basic Concept

A simplified realigned oscillator is shown in Fig. 1. It contains a multiplexer and a delay line. If the control signal *ED* always keeps in a low level, the scheme operates as a ring oscillator. Neglecting the delay effect of the multiplexer, the ring oscillator can be formed by a delay line which consists of a number of gain stages in a loop. However, as derived in [8], noise-introduced phase fluctuations persist indefinitely in oscillators, i.e., phase noise stays forever once it is introduced into the circuit. Hence a free-running oscillator can generally be modeled as a phase fluctuation integrator. This can be described as $1/s$ in frequency domain. On the other hand, phase noise depends on the time when the current is injected. The oscillator is most sensitive to noise during the transitions. Assuming that *ED* is generated from an input source with a fixed frequency very closed to that of the free-running oscillator, the realignment technique opens the ring loop and latches its output signal during the pulse duration. This causes the oscillator edge to be pulled toward a correct position. In addition, this realigned way can suppress the memory of the past error [9]. Therefore, the realigned oscillation technique can mitigate the phase noise contribution from the oscillator. In the proposed CDR, the CRC is based on realigned oscillation technique and can forcibly synchronize the clock phase to input burst-mode data signals whenever the data transition occurs.

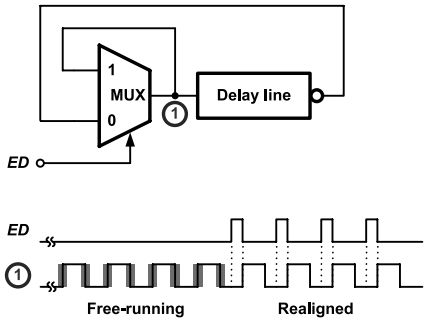


Fig. 1 Realign an oscillator to an edge and suppress the phase noise accumulation.

2.2 Architecture

In this work, the idea is to perform voltage-controlled oscillator (VCO) realignment by injection locking the VCO to input data signals whenever the data rising-edge transition occurs. Figure 2(a) shows a simplified block diagram of burst-mode CDR, which contains a PLL, a CRC, and a decision circuit. The CRC is formed by a rising-edge detector (RED) and a voltage-controlled realigned oscillator (VCRO). The RED can generate a pulse output Ⓐ to realign the oscillator while the input rising edge occurs. The oscillation frequency of the CRC is determined by the VCO in the PLL. It is interesting to note that the CRC in the PLL can be viewed as a VCO because no data transition appears at its input terminal. The PLL provides a control voltage (V_c) to make the CRC generate a desired frequency. The CRC realigns the phase of the burst-mode incoming data at a speed of 1.25 Gb/s to that of its 625-MHz clock signals which drive a decision circuit and retime the data to generate two 625-Mb/s sequences, D_{out1} and D_{out2}. Figure 2(b) shows a conceptual time chart of the proposed CDR.

3. Circuit Description

3.1 CRC Scheme

The half-rate CDR topology requires the CRC that provides a valid output while sensing a full-rate random data stream and a half-rate clock. The CRC employs two functions: (1) data transition detection, and (2) clock retiming with phase-locking operation. The scheme of the proposed CRC is shown in Fig. 3(a), which is built with a RED and a realigned two-stage ring oscillator. In this work, merging the RED to the oscillator can save power and increase the operating speed.

Figure 3(b), as shown in the dotted box of Fig. 3(a), is the schematic of the proposed delay cell merged with a RED to reuse its operation current as well as reduce the power dissipation. When input data keeps in a high or low level without rising-edge transition, the CRC is in *oscillation mode* and acts as an oscillator. Since Mn1-Mn2 active while Mn3-Mn4 are disabled, the delay cell in the ring oscillator consists of an NMOS input pair (Mn1-Mn2), a PMOS positive feedback pair (Mp3-Mp4), a diode-connected PMOS pair (Mp1-Mp2), and a PMOS transistor (MBp) for frequency tuning. The cross-connection of the Mp3-Mp4 differential

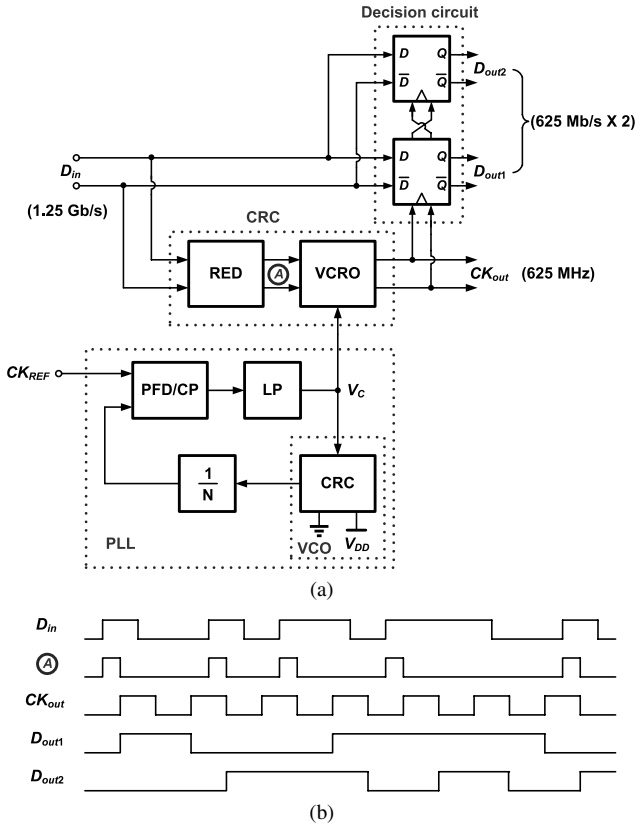


Fig. 2 Proposed burst-mode half-rate CDR: (a) architecture, and (b) conceptual timing.

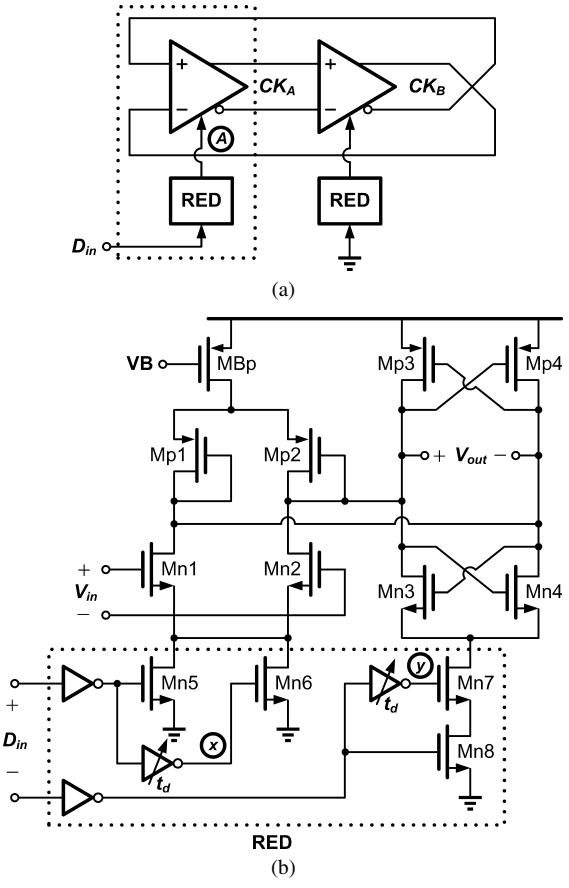


Fig. 3 Circuit implementation of the proposed CRC using (a) two-stage ring structure and (b) delay cell merged with an edge detector.

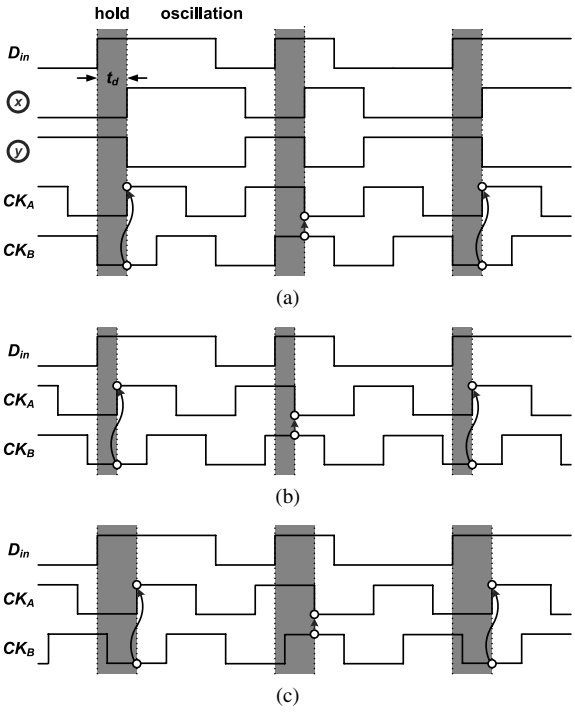


Fig. 4 Conceptual timing diagram of CRC for (a) $t_d = T_{CK}/4$, (b) $t_d < T_{CK}/4$, and (c) $t_d > T_{CK}/4$.

pair in positive feedback forms a negative resistance to suppress the resistive effect in the output, thereby an oscillator can be composed of such two delay cells. This delay cell operates the same as that in [10], which has the features of high-frequency operation, wide frequency-tuning range, and low phase-noise performance. Moreover, only two delay cells are included in the oscillator to minimize the power consumption. When a rising-edge transition of input data is detected, the RED produces a control regime to drive the CRC into *hold mode* with a duration of t_d. During this pulse time, Mn5-Mn6 are off but Mn7-Mn8 turns on, thereby Mn1-Mn2 cannot active while Mn3-Mn4 and Mp3-Mp4 function as a latch now, and thereby the output signal is held. While *hold mode* changes into *oscillation mode*, the input (CK_B) is immediately inversed to the output (CK_A) due to Mn5 or Mn6 turning on.

The CRC produces outputs, CK_A and CK_B, having a phase difference of 90°. Figure 4 illustrates the operation of the CRC. For example, if the input data sequence is 011010011..., the state of CK_A is held, i.e., into *hold mode*, during the duration of t_d when the data rising-edge transition occurs. Otherwise, the CRC operates as a ring oscillator with operation frequency of $1/T_{CK}$ when RED controls the CRC to enter *oscillation mode*. Figures 4(a), (b), and (c) display the timing diagram in the case of $t_d = T_{CK}/4$, $t_d < T_{CK}/4$, and $t_d > T_{CK}/4$. Here, the rising edge of CK_A will be injection-locked with the edge time that *hold mode* changes into *oscillation mode*, neglecting the delay effect in control path. If t_d approximates to $T_{CK}/4$, the input data, D_{in}, can lead the clock by $T_{CK}/4$, and thereby the CRC can

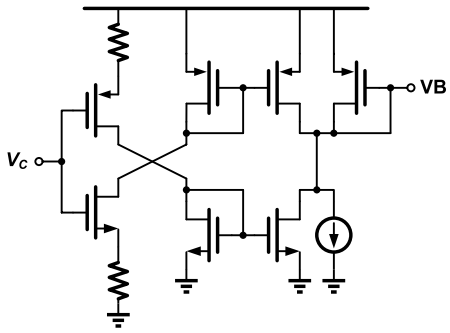


Fig. 5 CRC/VCO bias circuit.

sample the data closer to the middle of the eye in the decision circuit. In this work, t_d is tunable by the external control to get a better sampling point.

3.2 Decision Circuit

The decision circuit is also the high-frequency building block in the CDR. It is made by two D flip-flops. To reduce the supply noise, an emitter-coupled logical (ECL)-like differential structure is used [11]. The maximum speed of the flip-flop is determined by the fanout of the circuit as well as the implementation of the latches.

3.3 PLL

As seen in Fig. 2, the PLL block is composed of a phase/frequency detector (PFD), a charge pump (CP), a loop filters (LP), a divider, and the CRC employed as a VCO. To use the CRC as the VCO in PLL, "low" is applied to the RED input. The task of PLL is to provide a control voltage, V_c, to the CRC for generating desired frequencies, thereby the CRC generates the recovered clock signal which samples input data and operates with the same frequency as that of the VCO in the PLL.

The bias circuit of VCO/CRC uses a voltage-to-current converter, shown in Fig. 5, for biasing the current-starved cells with a wide dynamic input range [12]. The bias voltage is generated by current summing and subtracting. In this configuration, the voltage to current conversion ratio can be adjusted by changing the input transistor size or its source resistance value.

The PLL employs a 1/5 frequency divider to synthesize the 625-MHz clock from the 125-MHz external reference source. The VCO gain is about 125 MHz/V and the pumping current is 220 μA. The PLL has a locking range of 475–650 MHz with frequency range of 95–130 MHz for the reference signal.

4. Experimental Results

The proposed circuit was fabricated in a 0.18-μm N-well CMOS technology. Figure 6 shows the microphotograph of the burst-mode CDR. The chip area is $1.4 \times 1.4\,\text{mm}^2$. To deal proper with the imperfections between the CRC and

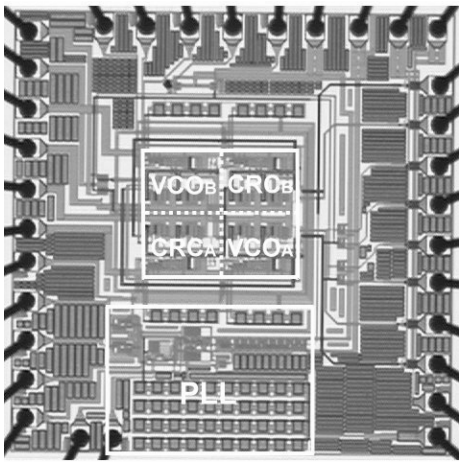


Fig. 6 Test-chip microphotograph.

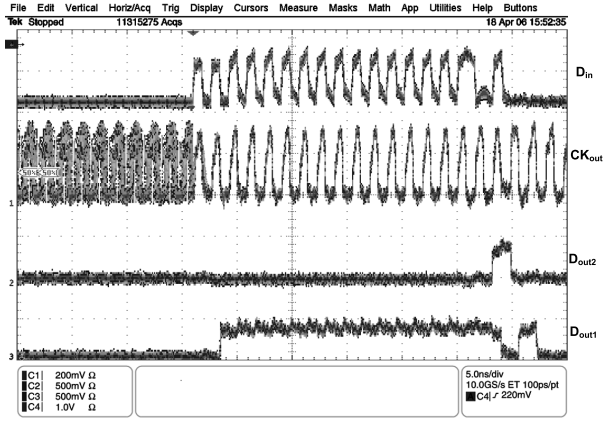
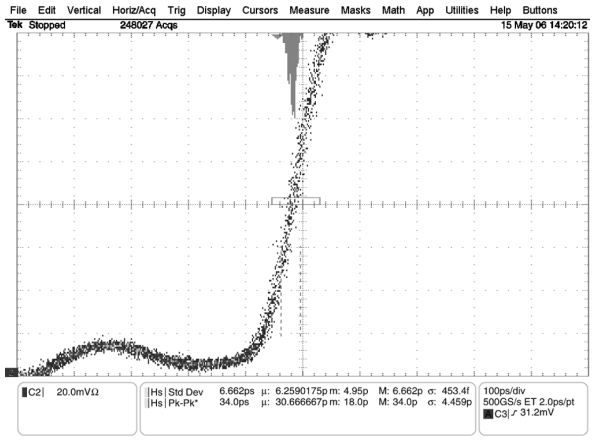
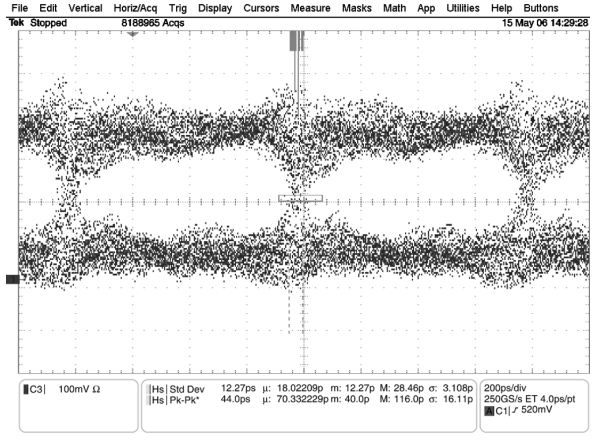


Fig. 7 Measured waveforms for burst testing.



(a)



(b)

Fig. 8 (a) Measured jitter histograms of the recovered clock and (b) the retimed data for 1.25-Gb/s ($2^{31} - 1$ PRBS).

the VCO, it demands many more layout precautions so as to minimize effects of crosstalk, noise, as well as mismatches. A common-centroid configuration is used for the layout of the four delay cells between the CRC and the VCO. The idea is to let the cells be placed diagonally opposite of each other (shown in Fig. 6). The loop filter is fully integrated in the chip by poly resistors and metal-metal capacitors. Each output signal is connected to an open-drain circuit with an externally match resistance of 50 Ω. The tested chip is measured under a supply voltage of 1.8 V.

A 1.25-Gb/s serial data stream is generated by a pulse-pattern generator (Anritsu MP1652A). The waveforms are derived from a digital oscilloscope (TDS 7704B) for measurement. In burst testing, a test pattern using (10101010101010101010101010101011001) followed by 1,000 ZEROs is employed. Figure 7 shows the waveforms of the monitored inputs, the retimed clock, and two recovered output data. The top trace of the recovered clock shows much jitter due to phase error accumulation induced by the absence of data transition. When data transition occurs, the jitter of the recovered clock is obviously reduced. For continuous data measurement, a 1.25-Gb/s serial data stream with a pseudo-random binary sequence (PRBS) of $2^{31} - 1$ is employed. Figure 8(a) shows the jitter histogram of the recovered clock, and Fig. 8(b) illustrates jitter histograms of the retimed data. As can be seen, the measured rms and peak-to-peak jitter of the recovered clock is 6.66 ps and 34.0 ps, respectively. Also, to the retimed data, we add a decision circuit driven by the CRC output, and the measured rms and peak-to-peak jitter is 12.27 ps and 40.0 ps, respectively. The total power consumption of the CDR is measured to be 32 mW, in which the PLL dissipates 11.6 mW. Table 1 gives the performance summary of the proposed burst-mode CDR with those in the literature.

5. Conclusion

This paper describes a 1.25-Gb/s 0.18-μm CMOS half-rate burst-mode CDR. The CDR employs a CRC with fast-locking characteristic by using open-loop realigned oscillation. Moreover, the CRC uses two-stage ring structure combining RED and a ring oscillator for low-power dissipation. The measured results demonstrate the functionality of the CDR with the proposed half-rate CRC.

Table 1 Burst-mode CDR performance summary and comparison.

Reference	This work	[5]	[6]
Technology	0.18-μm CMOS	–	0.35-μm CMOS
Supply voltage	1.8 V	–	3.3 V
Chip size	$1.4 \times 1.4\,mm^2$	–	$2.1 \times 2.1\,mm^2$
Operation range	0.95–1.3 Gb/s	–	400–622 Mb/s
Measured data rate	1.25 Gb/s	155 Mb/s	622 Mb/s
Recovered clock frequency	625 MHz	155 MHz	311 MHz
Power dissipation	CRC: 8.2 mW Decision circuit: 5.0 mW Output buffer: 7.2 mW PLL: 11.6 mW Total: 32 mW	–	130 mW excluding I/O 280 mW including I/O
Jitter performance	Recovered clock: $\Delta T_{r.m.s}$: 6.66 ps ΔT_{pk-pk}: 34.0 ps Retimed data: $\Delta T_{r.m.s}$: 12.27 ps ΔT_{pk-pk}: 40.0 ps (@ $2^{31} - 1$ PRBS)	Recovered clock: $\Delta T_{r.m.s}$: 48.58 ps ΔT_{pk-pk}: 416 ps (@ $2^{31} - 1$ PRBS)	PLL output: $\Delta T_{r.m.s}$: 11.35 ps ΔT_{pk-pk}: 76 ps

Acknowledgments

The authors would like to thank National Chip Implementation Center (CIC) and Taiwan Semiconductor Manufacturing Company (TSMC), Taiwan, for the fabrication of the chip.

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