Microelectronic Circuits (III)

Operational-Amplifier Circuits

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Outline

- The Two-Stage CMOS Op Amp
- The Cascode CMOS Op Amp
- 741 Op Amp Circuit
● OPAMPs are studied in this chapter.

● OPAMP design
  – bipolar OPAMPs can achieve better performance than CMOS OPAMPs.
  – CMOS OPAMPs are adequate for VLSI implementation.
  – BiCMOS OPAMPs combine the advantages of bipolar and CMOS devices.
Two-Stage CMOS Op Amps

Bias generation 1st stage 2nd stage

$I_{REF}$

$Q_8$ $Q_5$ $Q_7$

$+V_{DD}$

$I$

$Q_1$ $Q_2$ $C_C$

$Q_3$ $Q_4$ $Q_6$

$-V_{SS}$

$\nu_0$
• Voltage gain (discussed in Sec. 7.7.1)
  - Voltage gain of 1\textsuperscript{st} stage: \( A_1 = -g_{m1}(r_{o2} \parallel r_{o4}) \)
  - Voltage gain of 2\textsuperscript{nd} stage: \( A_2 = -g_{m6}(r_{o6} \parallel r_{o7}) \)
  - DC open-loop gain: \( A_v = A_1 \times A_2 \)

• Input offset voltage
  - \textit{Random offset}: device mismatches as random in nature
  - \textit{Systematic offset}: due to design technique \( \Rightarrow \) predictable

\[ \Rightarrow \frac{(W / L)_6}{(W / L)_4} = 2 \frac{(W / L)_7}{(W / L)_5} \]
If this condition is not met, a systematic offset will result.

• \( C_C \) is Miller-multiplied by the gain of the second stage to provide the required dominant pole.
Input Common-Mode Range

- The lowest value of $V_{ICM}$ has to be sufficiently large to keep $Q_1$ and $Q_2$ in saturation.

  $$V_{ICM} \geq -V_{SS} + V_{tn} + V_{OV3} - |V_{tp}|$$

- The highest value of $V_{ICM}$ should ensure $Q_5$ in saturation.

  $$V_{ICM} \leq V_{DD} - |V_{OV5}| - V_{SG1}$$

  $$\Rightarrow V_{ICM} \leq V_{DD} - |V_{OV5}| - |V_{tp}| - |V_{OV1}|$$

  $$\Rightarrow -V_{SS} + V_{OV3} + V_{tn} - |V_{tp}| \leq V_{ICM} \leq V_{DD} - |V_{tp}| - |V_{OV1}| - |V_{OV5}|$$

Select the values of $V_{OV}$ as low as possible!!
Output Swing

- Output swing

The extent of the output signal is limited at the lower and by the need to keep \( Q_6 \) saturated and at the upper end by the need to keep \( Q_7 \) saturated.

\[
-V_{SS} + V_{OV6} \leq v_O \leq V_{DD} - |V_{OV7}|
\]

Select the values of \( V_{OV} \) (of \( Q_6 \) and \( Q_7 \)) as low as possible!!

\( f_T \propto V_{OV} \) (in Sec. 6.2.3); the high-frequency performance of a MOSFET improves with the overdrive voltage at which it is operated.

- There must be a substantial overlap between the allowable range of \( V_{ICM} \) and \( v_O \) for an unit-gain amp application.
Example Two-Stage CMOS Op Amp Analysis

Let $I_{REF} = 25\mu A$, $|V_t|$ (for all devices) = 1V, $\mu_n C_{ox} = 20 \mu A/V^2$, $\mu_p C_{ox} = 10 \mu A/V^2$, $|V_A|$ (for all devices) = 25V, $V_{DD} = V_{SS} = 5V$. For all devices evaluate $I_D$, $|V_{GS}|$, $g_m$, and $r_o$. Also find $A_1$, $A_2$, the dc open-loop voltage gain, the input common-mode range, and the output voltage range. Neglect the effect of $V_A$ on bias current.

Solution

1. Dc analysis: Since $Q_8$ and $Q_5$ are matched, $I = I_{REF}$.

   Thus, $Q_1 - Q_4 : I_{D1-4} = 12.5\mu A$.

   $Q_7 : I_{D7} = I_{REF} = 25\mu A$ ($Q_7$ is matched $Q_5$ and $Q_8$).

   $Q_6 : I_{D6} = 25\mu A$.

   With $I_D$ of each device known, we use $I_C = \frac{1}{2}(\mu C_{ox}) (W/L)(|V_{GS}| - |V_t|)^2$ to determine $|V_{GS}|$.

2. Small-signal analysis:

   Transconductance $g_m = \mu C_{ox} (W/L)(|V_{GS}| - |V_t|) = \sqrt{2(\mu C_{ox})(W/L)I_D} = 2I_D/(|V_{GS}| - |V_t|)$

   $r_o$ is determined from $r_o = \frac{|V_A|}{I_D}$.
Summary of the dc and ac parameters:

| $I_D$ ($\mu$A) | $|V_{GS}|$ (V) | $g_m$ ($\mu$A/V) | $r_o$ (M$\Omega$) |
|---------------|----------------|-----------------|-----------------|
| 12.5          | 1.4            | 62.5            | 2               |
| 12.5          | 1.4            | 62.5            | 2               |
| 12.5          | 1.5            | 50              | 2               |
| 12.5          | 1.5            | 50              | 2               |
| 25            | 1.6            | 83.3            | 1               |
| 25            | 1.6            | 100             | 1               |
| 25            | 1.6            | 83.3            | 1               |
| 25            | 1.6            | 83.3            | 1               |

3. Determine the voltage gain:

   Voltage gain of 1$^{\text{st}}$ stage: $A_1 = -g_{m1}(r_{o2} \parallel r_{o4}) = -62.5(2 \parallel 2) = -62.5$ V/V

   Voltage gain of 2$^{\text{nd}}$ stage: $A_2 = -g_{m6}(r_{o6} \parallel r_{o7}) = -100(1 \parallel 1) = -50$ V/V

   The overall dc open-loop gain: $A_v = A_1 \times A_2 = (-62) \times (-50) = 3125$ V/V

4. Operating range:

   The lower limit of the input CM range: $Q_1$ and $Q_2$ leave the saturation region.

   Since the drain of $Q_1$ is at $-5 + 1.5 = -3.5$ V, then the lower limit of the input CM range is $-4.5$ V.

   The upper limit of the input CM range: $Q_5$ leave the saturation region.

   $V_{lcm/max} = V_{DD} - |V_{GS5}| + |V_t| = 5 - 1.6 + 1 - 1.4 = 3$ V

   The output range is determined from $Q_7$ leaving the saturation region,

   $V_{Omax} = V_{DD} - |V_{GS7}| + |V_t| = 5 - 1.6 + 1 = 4.4$ V

   and from $Q_6$ leaving the saturation region,

   $V_{Omin} = -V_{SS} + |V_{GS6}| - |V_t| = -4.5$ V
Input Offset Voltage

- **Random offset**: device mismatches as random in nature
- **Systematic offset**: due to design technique $\Rightarrow$ predictable

If the input stage is perfectly balanced, then $V_{DS4} = V_{DS3} = V_{GS4}$.

$\Rightarrow V_{GS4} = V_{GS6}$, hence $I_6 = \frac{(W/L)_6}{(W/L)_4} I_4 = \frac{(W/L)_6 I}{(W/L)_4 2}$

In order for no offset voltage to appear at the output, then $I_6 = I_7$.

Since $I_7 = \frac{(W/L)_7}{(W/L)_5} I$

$\Rightarrow \frac{(W/L)_6}{(W/L)_4} = 2 \frac{(W/L)_7}{(W/L)_5}$

If this condition is not met, a systematic offset will result.
Voltage Gain

Simplified small-signal equivalent circuit:

- $R_{in} = \infty$
- $G_{m1} = g_{m1} = g_{m2} \Rightarrow G_{m1} = \frac{2(I/2)}{V_{OV1}} = \frac{I}{V_{OV1}}$
- $R_1 = r_{o2} \parallel r_{o4}$
  - $r_{o2} = \frac{|V_{A2}|}{I/2}$
  - $r_{o4} = \frac{V_{A4}}{I/2}$
- Dc gain of 1st stage
  - $A_1 = -G_{m1}R_1 = -g_{m1}(r_{o2} \parallel r_{o4}) = -\frac{2}{V_{OV1}\left(\frac{1}{|V_{A2}|} + \frac{1}{V_{A4}}\right)}$
$A_1$ is increased by

1. $Q_1$ and $Q_2$ at a low overdrive
2. Choosing a longer channel length to obtain larger Early voltage, $|V_A|$

Both action, however, degrade the frequency response of the amplifier. (See Sec. 6.2.3)

- $G_{m2} = g_{m6} = \frac{2I_{D6}}{V_{OV6}}$
- $R_2 = r_{o6} \parallel r_{o7}$ \quad $r_{o6} = \frac{V_{A6}}{I_{D6}}$ \quad $r_{o4} = \frac{|V_{A7}|}{I_{D7}} = \frac{|V_{A7}|}{I_{D6}}$
- Dc gain of 2nd stage

$$A_2 = -G_{m2}R_2 = -g_{m6}(r_{o6} \parallel r_{o7}) = -\frac{2}{V_{OV6} \left( \frac{1}{V_{A6}} + \frac{1}{|V_{A7}|} \right)}$$

- Overall dc gain

$$A_v = A_1A_2 = G_{m1}R_1G_{m2}R_2 = g_{m1}(r_{o2} \parallel r_{o4})g_{m6}(r_{o6} \parallel r_{o7})$$

Generally, $500 \sim 5000$ V/V of $A_{v,\text{max}}$.

- Output resistance $R_o = r_{o6} \parallel r_{o7}$

$R_o$ can be large (the tens-of-kilohms range) for on-chip op amps.
Frequency Response

Small-signal equivalent circuit of the CMOS op amp:

- **Transfer function:** (See Sec. 7.7.1)
  \[
  V_o = \frac{G_m(G_m - sC_C)R_1R_2}{1 + s[C_1R_1 + C_2R_2 + C_C(G_{m2}R_1R_2 + R_1 + R_2)] + s^2[C_1C_2 + C_C(C_1C_2 + C_C(C_1 + C_2))]R_1R_2}
  \]

- **Capacitances:**
  \[
  C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}
  \]
  
  \[
  C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L \quad \text{(Usually, } C_L \text{ is larger than transistor capacitances)}
  \]

- **Miller capacitance:**
  \[
  C_T = (1 + G_{m2}R_2)(C_C + C_{gd6}) \approx G_{m2}R_2C_C
  \]

- **Poles:**
  \[
  \omega_{p1} = \frac{1}{R_1[C_1 + (1 + G_{m2}R_2)C_C]} \approx \frac{1}{G_{m2}R_2C_CR_1}
  \]
  \[
  \omega_{p2} \approx \frac{G_{m2}C_C}{C_1C_2 + C_C(C_1 + C_2)}
  \]

- If \( C_2, C_C \gg C_1 \), then \( \omega_{p2} \approx \frac{G_{m2}}{C_2} \).

- The value of \( \omega_t \) is usually selected to be lower than the frequencies of nondominant poles and zeros. Thus, \( A_0 \omega_{p1} = \omega_t \Rightarrow \omega_t = \frac{G_{m1}}{C_C} \).
Zero: The Miller capacitance $C_C$ introduces a right-half-plane zero.

\[ V_o = 0 \Rightarrow sC_C V_{i2} = G_{m2} V_{i2} \Rightarrow s_z = G_{m2} / C_C \]

- Since $G_{m2}$ is of the same order of magnitude as $G_{m1}$, the zero frequency will be close to $\omega_t$.
- Since the zero is in the right half-plane, it will decrease the phase margin.
  \[ \Rightarrow \text{?? stability} \]

- $f_{p1}$ is the dominant pole formed by the interaction of Miller-multiplied $C_C$ and $R_1$.

The unity-gain frequency:

\[ f_t = |A_v| f_{p1} = \frac{G_{m1}}{2\pi C_C} \]

$f_t$ must be lower than $f_{p2}$ and $f_z$, thus the design must satisfy the following two conditions:

\[ \frac{G_{m1}}{C_C} < \frac{G_{m2}}{C_2} \]
\[ G_{m1} < G_{m2} \]
Simplification Equivalent Circuit Analysis

- The circuit applies for $f \gg f_{p1}$.

An ideal integrator!!
Phase Margin

- Pole-splitting provides a low-frequency dominant pole \( f_{p1} \) and shifts \( f_{p2} \) beyond \( f_t \).
- At \( f_t \), the phase lag exceed 90° caused by \( f_{p1} \) and the excess phase shift due to \( f_{p2} \):
  \[
  \phi_{p2} = -\tan^{-1}\left( \frac{f_t}{f_{p2}} \right)
  \]
  \[
  \phi_z = -\tan^{-1}\left( \frac{f_t}{f_z} \right)
  \]

Phase lag at \( f_t \):
  \[
  \phi_{total} = 90^\circ + \tan^{-1}(f_t / f_{p2}) + \tan^{-1}(f_t / f_z)
  \]

- Phase margin:
  \[
  = 180^\circ - \phi_{total}
  \]
  \[
  = 90^\circ - \tan^{-1}(f_t / f_{p2}) - \tan^{-1}(f_t / f_z)
  \]
- Phase margin & stability (See 8.10.2)
- The right half-plane zero decreases the phase margin.
Improve CMOS Op Amp with the Resistance $R$

Small-signal equivalent circuit of the CMOS op amp with the resistance $R$.

- Find zero:

$$\frac{V_{i2}}{R + 1/sC_C} = G_{m2}V_{i2} \Rightarrow s_z = \frac{1}{C_C(1/G_{m2} - R)}$$

- $R = 1/G_{m2}$, the zero can be placed at infinite frequency.
- $R > 1/G_{m2}$, a left-half plane zero introduces adds to the phase margin.

- Discussion: The second pole is not very far from $\omega_t$. Thus the second pole introduces appreciable phase shift at $\omega_t$, which reduces the phase margin.
Slew Rate

- When large output signal are present, slew-rate limiting can cause nonlinear distortion.
- Slew rate: the maximum rate of change possible at the output of a real op amp.

\[
SR = \left. \frac{dv_o}{dt} \right|_{\text{max}}
\]

- A unity-gain follower with a large step input.
  (the output voltage cannot change immediately.)

\[
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\[
\text{Slew rate: the maximum rate of change possible at the output of a real op amp.}
\]

\[
SR = \left. \frac{dv_o}{dt} \right|_{\text{max}}
\]
Slew Rate of the Two-Stage CMOS Op Amp

Model of the two-stage CMOS op amp when a large differential voltage is applied.

\[ i_{D4} = I \]

\[ v_o(t) = \frac{I}{C_C} t \]

\[ \Rightarrow \quad SR = \frac{I}{C_C} \]
Relationship Between $SR$ and $f_t$

Slew rate \[ SR = \frac{I}{C_C} \]

\[ G_{m1} = g_{m1} = \frac{I}{|V_{GS1}| - |V_t|} \]

\[ \omega_t = \frac{G_{m1}}{C_C} \]

\[ \Rightarrow SR = (|V_{GS1}| - |V_t|)\omega_t = V_{OV1}\omega_t \]

- For a given $\omega_t$, the slew rate is determined by the overdrive voltage at which the first transistor are operated.
- $V_{OV} \uparrow \Rightarrow SR \uparrow$.
  ① For a given bias current $I$, a large $V_{OV}$ is obtained if $Q_1$ and $Q_2$ are $p$-channel devices. (1st stage)
  ② It allows the 2nd stage to employ an $n$-channel device that has a greater transconductance, $G_{m2}$, resulting in a higher second-pole frequency and a corresponding higher $\omega_t$. 
Ex.10.1 Two-Stage CMOS Op Amp Design

Design a dc gain of 4000 V/V in a 0.5-µm CMOS technology.

\[ V_{tn} = |V_{tp}| = 0.5V, \ k'_n = 200 \ \mu A/V^2, \ k'_p C_{ox} = 80 \ \mu A/V^2, \ V'_An = |V'_Ap| = 20V/\mu m, \ V_{DD} = V_{SS} = 1.65V, \ L = 1\mu m \text{ for all devices.} \text{ Let } I = 200\mu A, \ I_{D6} = 0.5mA. \]

If \( C_1 = 0.2pF \) and \( C_1 = 0.2pF \), find the required \( C_C \) and \( R \) to place the transmission zero at \( s = \infty \) for phase margin of 75°.

**Solution**

- **Voltage gain** \( A_v = g_m (r_{o2} \parallel r_{o4}) g_m (r_{o6} \parallel r_{o7}) = \frac{2(I/2) \cdot V_A}{V_{OV}} \cdot \frac{1}{2} \cdot \frac{V_A}{V_{OV}} \cdot \frac{2I_{D6}}{2} = \frac{V_A}{V_{OV}} \)

  \[ A_v = 4000 \text{ and } V_A = 20V \Rightarrow 4000 = \frac{400}{V_{OV}^2} \Rightarrow V_{OV} = 0.316V \]

- **(W/L)_1 and (W/L)_2**:

  \[ I_{D1} = \frac{1}{2} k'_p \left( \frac{W}{L} \right)_1 v_{OV}^2 \Rightarrow 100 = \frac{1}{2} \cdot 80 \left( \frac{W}{L} \right)_1 \cdot 0.316^2 \Rightarrow \left( \frac{W}{L} \right)_1 = \frac{25 \mu m}{1 \mu m} = \left( \frac{W}{L} \right)_2 \]
(W/L)_3 and (W/L)_4:
\[ I_{D1} = \frac{1}{2} k_n \left( \frac{W}{L} \right)_3 v_{OV}^2 \Rightarrow 100 = \frac{1}{2} \cdot 200 \left( \frac{W}{L} \right)_3 \cdot 0.316^2 \Rightarrow \left( \frac{W}{L} \right)_3 = \frac{10 \mu m}{1 \mu m} = \left( \frac{W}{L} \right)_4 \]

(W/L)_5:
\[ I_{D5} = \frac{1}{2} k_p \left( \frac{W}{L} \right)_5 v_{OV}^2 \Rightarrow 200 = \frac{1}{2} \cdot 80 \left( \frac{W}{L} \right)_5 \cdot 0.316^2 \Rightarrow \left( \frac{W}{L} \right)_5 = \frac{50 \mu m}{1 \mu m} \]

(W/L)_6 and (W/L)_7:
\[ \left( \frac{W}{L} \right)_7 = 2.5 \left( \frac{W}{L} \right)_5 = \frac{125 \mu m}{1 \mu m} \quad 500 = \frac{1}{2} \cdot 200 \left( \frac{W}{L} \right)_6 \cdot 0.316^2 \Rightarrow \left( \frac{W}{L} \right)_6 = \frac{50 \mu m}{1 \mu m} \]

Select \( I_{REF} = 20 \mu A \), thus \( \left( \frac{W}{L} \right)_8 = 0.1 \left( \frac{W}{L} \right)_5 = \frac{5 \mu m}{1 \mu m} \)

Input CM range: \(-1.33 \text{ V} \leq V_{ICM} \leq 0.52 \text{ V}\)

Max. signal swing: \(-1.33 \text{ V} \leq v_o \leq 1.33 \text{ V}\)

Input resistance: \( R_i = \infty \)

Output resistance: \( R_o = r_{o6} || r_{o7} = 20 \text{ k}\Omega \)

Determine \( f_{p2} \):
\[ G_{m2} = g_{m6} = \frac{2I_{D6}}{V_{OV}} = \frac{2 \times 0.5}{0.316} = 3.2 \text{ mA/V} \Rightarrow f_{p2} \approx \frac{G_{m2}}{2\pi C_2} = \frac{3.2 \times 10^{-3}}{2\pi \cdot 0.8 \times 10^{-12}} = 637 \text{ MHz} \]
To move the transmission zero to $s = \infty$, we select the value of $R$ as

$$R = \frac{1}{G_{m2}} = \frac{1}{3.2 \times 10^{-3}} = 316\Omega$$

For a phase margin of $75^\circ$, the phase shift due to $f_{p2}$ at $f = f_t$ must be $15^\circ$, that is

$$\tan^{-1} \frac{f_t}{f_{p2}} = 15^\circ$$

$$f_t = 637 \times \tan 15^\circ = 171MHz$$

Determine $C_C$:

$$C_C = \frac{G_{m1}}{2\pi f_t} \quad \text{where} \quad G_{m1} = g_{m1} = \frac{2 \cdot 100 \mu A}{0.316V} = 0.63mA/V$$

$$\therefore C_C = \frac{0.6 \times 10^{-3}}{2\pi \cdot 171 \times 10^6} = 0.6pF$$

Slew rate: [Eq. (9.40)]

$$SR = 2\pi f_t V_{OV} = 2\pi \cdot 171 \times 10^6 \times 0.316 = 340V/\mu s$$
Cascode CMOS Op Amp

Output resistance:
\[ R_o = R_{o2C} \parallel R_{o4C} = (g_{m2C}r_{o2C}r_{o2}) \parallel (g_{m4C}r_{o4C}r_{o3}) \]

Gain:
\[ A_1 = -g_{m1}R_o \]

- Composed of CS + CG.
- A high-gain single-stage op amp
- High output resistance: Increasing \( R_o \) by about two orders of magnitude increases \( A_1 \) by the same factor.
- But the input common-mode range is lower than that obtained in the two-stage amplifier.

Folded-cascode configuration have large common-mode range.
Folded-Cascode CMOS Op Amp

Folded: replace input transistor pairs with a counterpart.
More Complete Circuit for the Folded-Cascode CMOS Op Amp
Input common-mode range:

$V_{ICM}^{max}$ is limited by the requirement that $Q_1$ and $Q_2$ operate in saturation.

$$V_{ICM}^{max} = V_{DD} - |V_{OV9}| + V_{tn}$$

$V_{ICM}^{max}$ should ensure $Q_{11}$ in saturation.

$$V_{ICM}^{min} = -V_{SS} + V_{OV11} + V_{OV1} + V_{tn}$$

$$-V_{SS} + V_{OV11} + V_{OV1} + V_{tn} \leq V_{ICM}^{max} \leq V_{DD} - |V_{OV9}| + V_{tn}$$

$V_{BIAS3}$ should be selected to provide $I$ while operating $Q_{11}$ at a low overdrive voltage.

Output voltage swing:

Upper limit of $v_o$ is determined by the need to maintain $Q_{10}$ and $Q_4$ in saturation.

$$v_{o}^{max} = V_{DD} - |V_{OV10}| - |V_{OV4}|$$

Select $V_{BIAS1}$ so that $Q_{10}$ operates at the edge of saturation:

$$V_{BIAS1} = V_{DD} - |V_{OV10}| - V_{SG4}$$

Lowest $v_o$ is obtained when $Q_6$ reaches the edge of saturation.

$$v_{o}^{min} = -V_{SS} + V_{OV7} + V_{OV5} + V_{tn}$$
- Voltage gain

Small-signal equivalent circuit:

Transconductance

\[ G_m = g_{m1} = g_{m2} \quad G_m = \frac{2(I / 2)}{V_{OV1}} = \frac{I}{V_{OV1}} \]

Output resistance

\[ R_o = R_{o4} \parallel R_{o6} \quad R_{o4} \approx (g_{m4}r_{o4})(r_{o2} \parallel r_{o10}) \quad R_{o6} \approx g_{m6}r_{o6}r_{o8} \]

\[ R_o = \left[ g_{m4}r_{o4}(r_{o2} \parallel r_{o10}) \right] \parallel (g_{m6}r_{o6}r_{o8}) \]

Open-loop gain

\[ A_v = G_mR_o = g_{m1} \left\{ \left[ g_{m4}r_{o4}(r_{o2} \parallel r_{o10}) \right] \parallel (g_{m6}r_{o6}r_{o8}) \right\} \]
- Unity-gain buffer (voltage follower):

Output resistance \[ R_{of} = \frac{R_o}{1 + A_v} \approx \frac{R_o}{A_v} = \frac{R_o}{G_mR_o} = \frac{1}{G_m} = \frac{1}{g_{m1}} \]

- It is not very small for a single-stage op amp (OTA, operational transconductance amplifier).
- An ideal op amp has an zero output resistance!
Frequency response:
Since the primary purpose of CMOS op amps is to feed capacitive loads, $C_L$ is usually large, and the pole at the output becomes dominant.

- **Transfer function**
  \[
  \frac{V_o}{V_{id}} = \frac{G_m R_o}{1 + sC_L R_o}
  \]

- **Dominant pole**
  \[
  f_p = \frac{1}{2\pi C_L R_o}
  \]

- **Unity-gain frequency**
  \[
  f_t = A_v f_p = G_m R_o f_p = \frac{G_m}{2\pi C_L}
  \]

- **Discussion**
  Single-stage op amp: $C_L \uparrow \Rightarrow f_{p1}$, $f_t \downarrow \Rightarrow$ phase margin $\uparrow$
  Two-stage op amp: $C_L \uparrow \Rightarrow f_{p2}$ $\downarrow \Rightarrow$ phase margin $\downarrow$
• Slew Rate: a large differential input signal is applied. \((I_B > I)\)

\[
SR = \frac{I}{C_L} = 2\pi f_t V\text{OV1}
\]
Ex10.2 Design of a folded-cascode op amp.

$I = 200 \mu A$, $I_B = 250 \mu A$, and $|V_{OV}| = 0.25V$ for all transistors. $V_{DD} = V_{SS} = 2.5V$

$K_n' = 100 \mu A/V^2$, $K_p' = 40 \mu A/V^2$, $|V_A'| = 20V/\mu m$. $L = 1\mu m$, $C_L = 5pF$.

- Find $I_D$, $g_m$, $r_o$ and $W/L$ for all transistors.

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2I_D}{0.25}$$

$$r_o = \frac{|V_A|}{I_D} = \frac{20}{I_D}$$

$$\left(\frac{W}{L}\right)_i = \frac{2I_{Di}}{k'V_{OV}^2}$$

Note: for all transistors

$$g_m r_o = 160 \ V / V$$

$$V_{GS} = 1.0 \ V$$
• Find the allowable range of $V_{ICM}$ and of the output voltage swing. (p.9-29)

$$-1.25V \leq V_{ICM} \leq 3V \quad -1.25V \leq v_o \leq 2V$$

• Determine the values of $A_v$, $f_t$, $f_p$, and $SR$. (p.9-30, -32, -33)

$$R_{o4} = 160(200||80) = 9.14M\Omega \quad R_{o6} = 21.28M\Omega$$

$$R_o = R_{o4}||R_{o6} = 6.4M\Omega$$

$$A_v = G_mR_o = 0.8 \times 10^{-3} \cdot 6.4 \times 10^6 = 5120V/V$$

$$f_t = \frac{G_m}{2\pi C_L} = \frac{0.8 \times 10^{-3}}{2\pi \cdot 5 \times 10^{-12}} = 25.5MHz$$

$$f_p = \frac{f_t}{A_v} \left( \text{or} \quad \frac{1}{2\pi C_L R_o} \right) = \frac{25.5MHz}{5120} = 5kHz$$

$$SR = \frac{I}{C_L} = \frac{200 \times 10^{-6}}{5 \times 10^{-12}} = 40V/\mu s$$

• What is the power dissipation of the op amp?

$$P_D = 5V \times 0.5mA = 2.5mW$$
Rail-to-Rail Input Operation (Increasing $V_{ICM}$)

A folded-cascode op amp that employs two parallel complementary input stages to achieve rail-to-rail input CM operation.

$$\Delta i = G_m(V_{id}/2)$$
$$G_m = g_{m1} = g_{m2} = g_{m3} = g_{m4}$$
Output voltage \[ V_o = 2G_mR_oV_id \]

Voltage gain \[ A_v = \frac{V_o}{V_id} = 2G_mR_o \]

Operation analysis:

Over the remainder of the input CM range, only one of two differential pairs will be operational, and the gain drops to half.
Wide-Swing Current Mirror (Increasing the Output Voltage Range)

The minimum voltage allowed at the output is $V_t + 2V_{OV}$.

The minimum voltage allowed at the output is $2V_{OV}$.
Homework-1

- Problems: 3, 5, 6, 8, 11, 13, 15, 17
741 Op-Amp

- 741 op-amp uses a large number of transistors but relatively few resistors and only one capacitor.
  - $R$ and $C$ occupy large silicon area.
  - $C$ needs more fabrication steps.
  - High-quality $R$ & $C$ are not easy to fabricate.
- Circuit Diagram in next page.
741 Op-Amp

Input stage

Bias generation

Bias

2nd gain stage

Protecting

Class AB

Output stage

Microelectrics (III)
Microelectronics (III)

1.9-39
741 Op-Amp Circuit

In keeping with the IC design philosophy the circuit uses a large number of transistors, but relatively few transistors, and only one capacitor. This philosophy is dictated by the economics (silicon area, ease of fabrication, quality of realizable components) of the fabrication of active and passive components in IC form.

741 op-amp consists of three stages

1) Input differential stage
2) Single-ended high-gain stage
3) Output-buffering stage
Bias Circuit: $Q_{11}, Q_{12}, Q_{10}, R_4, Q_8, Q_9, Q_{13}$

- Bias current $I_{REF}$ is generated in the branch, consisting of the two diode-connected transistors $Q_{11}$ and $Q_{12}$ and the resistance $R_5$.
- Using a Widlar current source formed by $Q_{11}$, $Q_{10}$, and $R_4$, bias current for the first stage is generated in the collector of $Q_{10}$.
- Another current mirror formed by $Q_8$ and $Q_9$ takes part in biasing the first stage.
- Double-collector PNP $Q_{13}$:

Current mirror:

$$\frac{I_O}{I_{REF}} \approx \frac{A_{E(Q_A)}}{A_{E(Q_B)}}$$

$A_E$ is emitter area.
The Input Stage: \( Q_1 \sim Q_7, R_1 \sim R_3 \).
- Biased by \( Q_8, Q_9, \) and \( Q_{10} \) provide high input impedance.
- \( Q_3 \) and \( Q_4 \) are lateral PNP (low \( \beta \)) higher emitter-base junction breakdown than NPNs.
  \( \Rightarrow \) protect input transistors \( Q_1 \) and \( Q_2 \) when they are accidentally shorted to supply voltages.
- \( Q_5 \sim Q_7, R_1 \sim R_3 \) provide high-resistance load and single ended output.
- Level shifter: \( Q_3 \) and \( Q_4 \)
The Second Stage: $Q_{16}, Q_{17}, Q_{13B}, R_8, R_9$
- $Q_{16}$ acts as an emitter follower, thus giving
  1. high input resistance
  2. low base current if $R_9$ is large, hence low loading of the first stage.
- $Q_{17}$: common base configuration active load formed by $Q_{13B}$ (active load is better than resistor load).
- $C_C$: Miller capacitor for pole-splitting compensation 30PF area occupied is about 13 times that of a standard NPN transistor.
The Output Stage:
1) provide low output resistance
2) class AB

The 741 uses an efficient class AB output stage, which consists of the complementary pair $Q_{14}$ and $Q_{20}$ with biasing devices $Q_{13A}$, $Q_{18}$ and $Q_{19}$, and an input buffer $Q_{23}$. (where $Q_{20}$ is a substrate $pnp$.)

Short-Circuit Protection Circuitry

Transistors $Q_{15}$, $Q_{21}$, $Q_{24}$, and $Q_{22}$, and resistors $R_6$ and $R_7$ serve to protect the amplifier against output short circuits and these transistors are normally off.
● Device Parameters:

- **The standard transistors:**
  - \( npn \): \( I_S = 10^{-14} \) A, \( \beta = 200 \), \( V_A = 125 \) V
  - \( pnp \): \( I_S = 10^{-14} \) A, \( \beta = 50 \), \( V_A = 50 \) V

- **The nonstandard transistors:** \( Q_{13}, Q_{14}, \) and \( Q_{20} \).
  - \( Q_{13A} \) : \( I_{SA} = 0.25 \times 10^{-14} \) A
  - \( Q_{13B} \) : \( I_{SA} = 0.75 \times 10^{-14} \) A
  - \( Q_{14} \) & \( Q_{20} \) : \( I_S = 3 \times 10^{-14} \) A (have an area three times that of a standard device)

Output transistors usually have large areas in order to be able to supply large load currents and dissipate relatively large amounts of power with only a moderate increase in the device temperature.

Microelectrics (III)
Output Stages (in Chap. 13)

- Class A output stage: Emitter follower

Large power is dissipated in the transistor!!
### Output Stages

- **Class B output stage**

There exists a range of $v_I$ centered around zero where both transistors are cut off and $v_O$ is zero. This dead band results in the **crossover distortion**!
Output Stages

- Class AB output stage
Reference Bias Current & Input-Stage Bias

- Reference bias current

\[ I_{REF} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5} = 0.73 \text{ mA} \]

- Input-stage bias

Widlar current source:

\[ V_{BE11} - V_{BE10} = I_{C10} R_4 \]

\[ \Rightarrow V_T \ln \left( \frac{I_{REF}}{I_{C10}} \right) = I_{C10} R_4 \]

\[ \Rightarrow I_{C10} = 19 \mu A \quad \text{(solved by trial and error)} \]
$I_{C1} = I_{C2} \Rightarrow I_{E3} = I_{E4} \approx I \text{ (High } \beta\text{)}$

$I_{C9} = \frac{2I}{1 + 2/\beta}$  \[\text{pp: 509, Eq.(6.69)}\]

$\Rightarrow 2I \approx I_{C10} \text{ (} \beta\gg 1\text{)}$

For the 741, $I_{C10} = 19 \mu A$, thus $I \approx 9.5 \mu A$.

We have $I_{C1} = I_{C2} \approx I_{C3} = I_{C4} = 9.5 \mu A$
Neglect the base current of $Q_{16}$, then

$I_{C6} \approx I$

Neglect the base current of $Q_7$, then

$I_{C5} \approx I$

Bias current of $Q_7$: (KCL at node-A)

$I_{C7} \approx I_{E7} = \frac{2I}{\beta_N} + \frac{V_{BE6} + IR_2}{R_3}$

Determine $V_{BE6}$: ($I_S = 10^{-14}$ A)

$V_{BE6} = V_T \ln\left(\frac{I}{I_S}\right) = 517 \text{ mV}$

\[ \Rightarrow \quad I_{C7} = 10.5 \mu\text{A} \]
• Input bias current  
\[ I_B = \frac{I_{B1} + I_{B2}}{2} \]

For the 741,  
\[ I_B = \frac{I}{\beta_N} \quad \Rightarrow \quad \text{Using } \beta_N = 200, \text{ yields } I_B = 47.5 \text{ nA}. \]

Much lower input bias currents can be obtained using an FET input stage.

• Input offset currents

Because of possible mismatches in the \( \beta \) mismatch, the input offset current is defined as

\[ I_{OS} = |I_{B1} - I_{B2}| \]

• Input offset voltage

The input offset voltage is determined primarily by mismatches between the two sides of the input stage. In the 741 op amp, the input offset voltage is due to mismatches between \( Q_1 \) and \( Q_2 \), between \( Q_3 \) and \( Q_4 \), between \( Q_5 \) and \( Q_6 \), and between \( R_1 \) and \( R_2 \).

• Input common-mode range

- The input common-mode range is the range of input common-mode voltages over which the input stage remains in the linear active mode.

- In the 741, the input common-mode range is determined at the upper end by saturation of \( Q_1 \) and \( Q_2 \), and at the lower end by saturation of \( Q_3 \) and \( Q_4 \).
Second-Stage Bias

\[ I_{C13B} \approx 0.75I_{REF} \quad (\beta_P >> 1) \]

\[ \Rightarrow I_{C13B} = 550 \, \mu A \quad \text{and} \quad I_{C17} \approx 550 \, \mu A \]

\[ V_{BE17} = V_T \ln \left( \frac{I_{C17}}{I_S} \right) = 618 \, \text{mV} \]

\[ I_{C16} \approx I_{E16} = I_{B17} + \frac{I_{E17}R_8 + V_{BE17}}{R_9} = 16.2 \, \mu A \]
Output-Stage Bias

\[ I_{C13B} \approx 0.25I_{REF} \approx I_{E23} \]
\[ I_{C23} \approx I_{E23} \approx 0.25I_{REF} = 180 \, \mu A \]
\[ V_{BE18} \approx 0.6 \, V \Rightarrow I_{R10} = 15 \, \mu A \]
\[ I_{E18} = 180 - 15 = 165 \, \mu A \approx I_{C18} \]
\[ \Rightarrow V_{BE18} = 588 \, mV \]
\[ I_{B18} = 165 / 200 = 0.8 \, \mu A \]
\[ \Rightarrow I_{C19} \approx I_{E19} = 15.8 \, \mu A \]
\[ V_{BE19} = V_T \ln \left( \frac{I_{C19}}{I_S} \right) = 530 \, mV \]
\[ V_{BB} = V_{BE18} + V_{BE19} = 1.118 \, V \]
\[ V_{BB} = V_T \ln \left( \frac{I_{C14}}{I_{S14}} \right) + V_T \ln \left( \frac{I_{C20}}{I_{S20}} \right) \]
\[ I_{S14} = I_{S20} = 3 \times 10^{-14} \, A \]
\[ \Rightarrow I_{C14} = I_{C20} = 154 \, \mu A \]
## Summary of Dc Bias of the 741 Circuit

<table>
<thead>
<tr>
<th>Q</th>
<th>9.5</th>
<th>Q8</th>
<th>19</th>
<th>Q13B</th>
<th>550</th>
<th>Q19</th>
<th>15.8</th>
</tr>
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<tbody>
<tr>
<td>Q2</td>
<td>9.5</td>
<td>Q9</td>
<td>19</td>
<td>Q14</td>
<td>154</td>
<td>Q20</td>
<td>154</td>
</tr>
<tr>
<td>Q3</td>
<td>9.5</td>
<td>Q10</td>
<td>19</td>
<td>Q15</td>
<td>0</td>
<td>Q21</td>
<td>0</td>
</tr>
<tr>
<td>Q4</td>
<td>9.5</td>
<td>Q11</td>
<td>730</td>
<td>Q16</td>
<td>16.2</td>
<td>Q22</td>
<td>0</td>
</tr>
<tr>
<td>Q5</td>
<td>9.5</td>
<td>Q12</td>
<td>730</td>
<td>Q17</td>
<td>550</td>
<td>Q23</td>
<td>180</td>
</tr>
<tr>
<td>Q6</td>
<td>9.5</td>
<td>Q13A</td>
<td>180</td>
<td>Q18</td>
<td>165</td>
<td>Q24</td>
<td>0</td>
</tr>
<tr>
<td>Q7</td>
<td>10.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Small-Signal Analysis of the 741 Input Stage

The differential signal $v_i$ applied between the input terminals effectively appears across four equal emitter resistances connected in series – those of $Q_1$, $Q_2$, $Q_3$, and $Q_4$.

$$i_e = \frac{v_i}{4r_e}$$

where

$$r_e = \frac{V_T}{I} = \frac{25 \text{ mV}}{9.5 \text{ } \mu\text{A}} = 2.63 \text{ k}\Omega$$

The input differential resistance of the op amp is

$$R_{id} = 4(\beta_N + 1)r_e$$

For $\beta_N = 200$, we obtain $R_{id} = 2.1 \text{ M}\Omega$. 
Small-Signal Analysis of the Input Stage with Load Stage

The output node of the input stage: output current \( i_o = 2\alpha i_e \).

The factor of two indicates that conversion from differential to single-ended is performed without losing half the signal.

Transconductance of the input stage: \( G_{m1} \equiv \frac{i_o}{v_i} = \frac{\alpha}{2r_e} \)

Substituting \( r_e = 2.63 \ \text{k}\Omega \) and \( \alpha \approx 1 \) yields \( G_{m1} = 1/5.26 \ \text{mA/V} \).
Output Resistance of the First Stage

The output resistance of the input stage:

$$R_{o1} = R_{o4} \parallel R_{o6}$$
\[ R_{o4} = r_{o4} + (1 + g_{m4}r_{o4})R'_E \]
\[ \approx r_{o4}(1 + g_{m4}R'_E) \]

where \( R'_E = r_{e2} \parallel r_\pi \) and \( r_o = V_A / I \).

\( V_A = 50 \text{ V}, I = 9.5 \text{ µA}, \)
\( r_{e2} = 2.63 \text{ kΩ}. \)
\( \Rightarrow R_{o4} = 10.5 \text{ MΩ} \)

\[ R_{o6} = r_{o6} + (1 + g_{m6}r_{o6})(R_2 \parallel r_\pi) \]
\[ \approx r_{o6}[1 + g_{m6}(R_2 \parallel r_\pi)] \]
\( \Rightarrow R_{o6} = 18.2 \text{ MΩ} \)

The output resistance of the input stage: \( R_{o1} = R_{o4} \parallel R_{o6} = 6.7 \text{ MΩ} \)
Small-Signal Equivalent Circuit for the Input Stage of the 741 Op Amp

The equivalent circuit is a simplified version of the $y$-parameter model of a two-port with $y_{12}$ assumed negligible.

\[ R_{id} = 2.1 \text{ M\Ohm} \]
\[ G_{m1} = 1/5.26 \text{ mA/V} \]
\[ R_{o1} = 6.7 \text{ M\Ohm} \]
Ex: 10.3 mismatch in the Input Stage

Input stage with both inputs grounded and a mismatch $\Delta R$ between $R_1$ and $R_2$.

\[
\begin{align*}
V_{BE5} + IR &= V_{BE6} + (I - \Delta I)(R + \Delta R) \\
\Rightarrow V_{BE5} - V_{BE6} &= I\Delta R - \Delta I(R + \Delta R) \\
\text{and} \quad V_{BE5} - V_{BE6} &= I_{E5}r_{e5} - I_{E6}r_{e6} \approx \Delta I r_e \\
\Rightarrow \quad \frac{\Delta I}{I} &= \frac{\Delta R}{R + \Delta R + r_e}
\end{align*}
\]

A 2% mismatch between $R_1$ and $R_2$:

- Substituting $R = 1 \, \text{k}\Omega$, $r_e = 2.63 \, \text{k}\Omega$, we have $\Delta I = 5.5 \times 10^{-3} \, I$.
- To reduce this output current to zero, we have to apply an input voltage $V_{OS}$ given by

\[
V_{OS} = \frac{\Delta I}{G_{m1}} = \frac{5.5 \times 10^{-3} I}{G_{m1}}
\]

\[
I = 9.5 \, \mu\text{A}, \quad G_{m1} = 1/5.26 \, \text{mA/V} \quad \Rightarrow \quad V_{OS} \approx 0.3 \, \text{mV}
\]
**Ex: 10.4 CMRR of 741 input stage**

Total resistor at node - Y:

\[ R_o = R_{o9} \parallel R_{o10} \]

KCL at node - Y:

\[ 2i + \frac{2i}{\beta_p} = \frac{v_{icm}}{R_o} \text{, if } \beta_p \gg 1 \]

\[ i \approx \frac{v_{icm}}{2R_o} \]

\[ i_o = \varepsilon_m i \]

\[ G_{mcm} = \frac{i_o}{v_{icm}} = \frac{\varepsilon_m i}{v_{icm}} = \frac{\varepsilon_m}{2R_o} \]

\[ CMRR \equiv \frac{G_{m1}}{G_{mcm}} = 2g_{m1}R_o / \varepsilon_m \]

\[ CMRR = 2g_{m1}(R_{o9} \parallel R_{o10}) / \varepsilon_m \]
2nd stage: Input Resistance & Transconductance

- Input resistance

\[ R_{i2} = (\beta_{16} + 1)[r_{e16} + R_9][(\beta_{17} + 1)(r_{e17} + R_8)] \]

\[ \approx 4 \text{ M}\Omega \]

- Transconductance

\[ i_{c17} = \frac{\alpha v_{b17}}{r_{e17} + R_8} \]

\[ v_{b17} = v_{i2} \frac{R_9 R_{i17}}{(R_9 R_{i17}) + r_{e16}} \]

\[ R_{i17} = (\beta_{17} + 1)(r_{e17} + R_8) \]

\[ \Rightarrow G_{m2} = \frac{i_{c17}}{v_{i2}} = 6.5 \text{ mA/V} \]
Output resistance \( R_{o2} = R_{o13B} \parallel R_{o17} \)

where \( R_{o13B} = r_{o13B} = 90.9 \text{ k}\Omega. \)

Since the resistance between the base of \( Q_{17} \) and ground is relatively small, the base is about grounded.

Thus, \( R_{o17} \approx 787 \text{ k}\Omega, \) and hence \( R_{o2} \approx 81 \text{ k}\Omega. \)
Note that the stage open-circuit voltage gain is $-G_m R_o$. 

$-G_m R_o \omega_{12} = \omega_{02}$.
The output stage is of the AB class, with the network composed of $Q_{18}$, $Q_{19}$, and $R_{10}$ providing the bias of the output transistors $Q_{14}$ and $Q_{20}$.

The emitter follower $Q_{23}$ provides added buffering, which makes the op-amp gain almost independent of the parameters of the output transistors.
Output Voltage Limits

\[ v_{o\text{max}} = V_{CC} - V_{CE\text{sat}} - V_{BE14} \]
\[ v_{o\text{min}} = -V_{EE} + V_{CE\text{sat}} + V_{EB23} + V_{EB20} \]

(neglecting the voltage drop across \( R_8 \))
Small-Signal Model of the 741 Output Stage

the second stage

**Find** $R_{i3}$:

- The input resistance looking into the base of $Q_{20}$, $R_{B20} \approx \beta_{20} R_L = 50 \times 2 \text{ k}\Omega = 100 \text{ k}\Omega$.
- $R_{B20}$ appears in parallel with the series combination of the output resistance of $Q_{13A}$ ($r_{o13A} \approx 280 \text{ k}\Omega$) and the resistance of the $Q_{18} - Q_{19}$ network (very small).
- The total resistance in the emitter of $Q_{23}$, $R_{E23} \approx 100 \text{ k}\Omega \parallel 280 \text{ k}\Omega = 74 \text{ k}\Omega$.
- The input resistance $R_{i3} \approx \beta_{20} R_{E23} = 50 \times 74 \text{ k}\Omega \approx 3.7 \text{ M}\Omega$.

**Open-circuit voltage voltage gain, $\mu$**:

$$\mu = \left. \frac{V_o}{V_{o2}} \right|_{R_L = \infty} \approx 1$$

- With $R_L = \infty$, the gain of the emitter-follower output transistor ($Q_{14}$ or $Q_{20}$) will be nearly unity.
- With $R_L = \infty$ the resistance in the emitter of $Q_{23}$ will be very large.
Find the output resistance, $R_o$:

- Substituting $R_{o2} = 81 \ \text{k}\Omega$, $\beta_{23} = 50$, and $r_{e23} = 25/0.18 = 139\ \Omega$ yields $R_{o23} = 1.73 \ \text{k}\Omega$.
- For an output current of 5mA, $r_{e20}$ is 5 \ \Omega and $R_o = 39 \ \Omega$ with $\beta_{20} = 50$. 
Output Short-Circuit Protection

- If the op-amp output terminal is short-circuited to one of the power supplies, one of the two output transistors could conduct a large amount of current. ⇒ resulting in sufficient heating to cause burnout of the IC.

- Mechanism
  - $R_6$ together with $Q_{15}$ limits the current that would flow out of $Q_{14}$ in the event of a short circuit.
    - If the current in the emitter of $Q_{14}$ exceeds about 20 mA, the voltage drop across $R_6$ exceeds 540 mV, which turns $Q_{15}$ on.
    - As $Q_{15}$ turns on, its collector robs some of the current supplied by $Q_{13A}$, thus reducing the base current of $Q_{14}$.
    - This mechanism thus limits the maximum current that op amp can source to about 20 mA.
  - The relevant circuit is composed of $R_7$, $Q_{21}$, $Q_{24}$, and $Q_{22}$. The current in the inward direction is limited also to about 20 mA.
Microelectrics (III)
Small-Signal Gain of the 741

Cascading the small-signal equivalent circuits of the individual stages for the evaluation of the overall voltage gain

Overall gain:

\[
\frac{v_o}{v_i} = \frac{v_{i2}}{v_i} \frac{v_{o2}}{v_{i2}} \frac{v_o}{v_{o2}} = -G_m \left(R_{o2} \parallel R_{i2} \right) \left(-G_{m2}R_{o2}\right)\mu \frac{R_L}{R_L + R_o}
\]

\[
\frac{v_o}{v_i} = -476.1 \times (-526.5) \times 0.97 = 243,147 \text{ V/V} = 107.7 \text{ dB}
\]
Frequency Response of the 741

Miller compensation technique – to introduce a dominant low-frequency pole

- A 30-pF capacitor ($C_C$) is connected in the negative-feedback path of the second stage. The effective capacitance due to $C_C$ between the base of $Q_{16}$ and ground is

$$C_i = C_C \left( 1 + |A_2| \right)$$

where $A_2 = -515$, and hence $C_i = 15,480$ pF.

- The total resistance between the base of $Q_{16}$ and ground is

$$R_t = (R_{o1} \parallel R_{i2}) = (6.7 \, \text{M}\Omega \parallel 4 \, \text{M}\Omega) = 2.5 \, \text{M}\Omega$$

- The dominant pole:

$$f_p = \frac{1}{2\pi C_i R_t} = 4.1 \, \text{Hz}$$

- Unit-gain bandwidth

$$f_i = A_0 \times f_{3\text{dB}} \approx 1 \, \text{MHz}$$

- Phase margin $= -90^\circ$

In practice, PM $\approx -80^\circ$ due to nondominant pole.

This phase margin is sufficient to provide stable operation of close-loop amplifier with any value of feedback factor $\beta$. 

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Microelectronics (III)

1.9-73
A Simplified Model Based on Modeling the Second Stage as an Integrator

\[ A(s) = \frac{V_o(s)}{V_i(s)} = \frac{G_{m1}}{sC_C} \Rightarrow A(j\omega) = \frac{G_{m1}}{j\omega C_C} \]

Unity-gain frequency: \( \omega_t = \frac{G_{m1}}{C_C} \)

Substituting \( G_{m1} = 1/5.26 \) mA/V and \( C_C = 30 \) pF yields \( f_t = \frac{\omega_t}{2\pi} \approx 1 \) MHz

This model is valid only at frequency \( f >> f_{3dB} \). At such frequencies the gain falls off with a slope of \(-20dB/\)decade, just like that of an integrator.
Slew Rate of the 741

- A unity-gain follower with a large step input

Since the output voltage cannot change immediately, a large differential voltage appears between the op amp input terminal.

- Model for the 741 op amp when a large differential signal is applied

Output voltage:
\[ v_o(t) = \frac{2I}{C_C} t \]

Slew rate:
\[ SR = \frac{2I}{C_C} \]

For the 741, \( I = 9.5 \, \mu A \) and \( C_C = 30 \, \text{pF} \), resulting in \( SR = 0.63 \times 10^6 \, \text{V/s} \).
Relationship Between $f_t$ and $SR$

- $G_{m1}$: $G_{m1} = 2 \frac{1}{4r_e}$

  where $r_e$ is the emitter resistance of each of $Q_1$ through $Q_4$.
  Thus,
  $$r_e = \frac{V_T}{I} \quad \text{and} \quad G_{m1} = \frac{I}{2V_T}$$

- $\omega_t$: $\omega_t = \frac{G_{m1}}{C_C} = \frac{I}{2C_C V_T} \quad \Rightarrow \quad \omega_t = \frac{SR}{4V_T}$

- $SR$: $SR = 4V_T \omega_t$
  For the 741 we have $SR = 4 \times 25 \times 10^3 \times 2\pi \times 10^6 = 0.63 \times 10^6$ V/s.

- A general form for the relationship between $SR$ and $\omega_t$ for an op amp with a structure similar to that of the 741 is
  $$SR = \left( \frac{2}{a} \right) \omega_t$$

  where $a$ is the constant of proportionality relating transconductance of the first stage $G_{m1}$, to the first-stage bias current $I$, $G_{m1} = aI$.
  For a given $\omega_t$, a higher value of $SR$ is obtained by making $a$ smaller;
  $\Rightarrow I = \text{constant}, \ G_{m1} \downarrow$. 

Microelectrics (III)
Home work-2

- Problems: 20, 21, 22, 23, 24, 28, 35, 36, 40, 41, 48, 49, 52