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A CMOS Clock and Data Recovery Circuit with a Half-Rate Three-State Phase Detector

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SUMMARY A clock and data recovery (CDR) circuit using a new half-rate wide-range phase detection technique has been developed. Unlike the conventional three-state phase detectors, the proposed detector is applicable to the Non-Return-to-Zero (NRZ) data stream and also has low jitter and wide capture range characteristics. The CDR circuit was implemented in a 0.35-μm N-well CMOS technique. Experimental results demonstrate that it can achieve the peak-to-peak jitter of the recovered clock and the retimed data about 120 ps and 170 ps, respectively, while operating at the input data rate of 1 Gb/s. The total power dissipation of the CDR is 64.8 mW for the supply 3 V.

key words: *phase-locked loop, phase synchronization, clock and data recovery, phase detector*

1. Introduction

In digital communication systems, information is conveyed by a series of bits — ONEs and ZEROs. To process the data correctly, the receiver usually needs a clock and data recovery (CDR) circuit to synchronize a clock to the data; so the CDR bears a certain phase relationship with respect to data, allowing optimum sampling of the bits by the clock. In order to sampling the data correctly, the clock frequency equals the data rate. For example, a data rate of 1 Gb/s translates to a clock frequency of 1 GHz. The CDR is usually accomplished by a phase-locked loop (PLL), which synchronizes the frequency and phase of clock. In addition, the recovered clock must exhibit a small jitter as it is the principal contributor to the retimed data jitter.

The application of PLL's to CDR's has some special design considerations. Because of the random nature of data, the choice of phase detectors is restricted. One way to recover clock from NRZ data is to convert it to a return-zero (RZ)-like data, and then recovery clock from that RZ data with a PLL [1]. It is also possible to compare the phase of NRZ data directly with a clock. A phase detector, directly applicable to the NRZ data stream, had been developed by Hogge [2]. However, that phase detector employs large jitter due to ripple generated by charging and discharging current on the charge-pump circuit even at in-phase state. This effect has been improved by "tri-wave" method [3], but it still lacks frequency detection characteristics to expand the range of the operating frequency. Thus, most clock recovery circuits require a means of frequency detection in addition to phase detection [4]–[7].

In many applications of PLL's such as clock generators or frequency synthesizers, the three-state phase detector is widely used due to the characteristics both of phase and frequency detection as well as its large figure of merit [8]. The PLL with the three-state phase detector senses the transitions at the input and the output, detects phase and frequency differences, and activates the charge pump accordingly. The loop locks when the phase difference drops to zero and the charge pump remains relatively idle. The three-state phase detector is better than the Hogge's phase detector due to the wide locking range as well as the little ripple on the filter. However, this type of phase detector won't work while employing the data stream with missing pulses.

In this paper, a novel three-state phase detector using a half-rate clock is developed to the random data stream. The proposed phase detector has the same operation as the conventional three-state one, which has low jitter at in-phase state and also has large locking range due to its characteristic of phase detection. It is an important concern to achieve a relatively wide capture range without any mean used to aid acquisition so that the circuit can lock to the input in the presence of temperature and process variations. The paper is organized as follow. Section 2 describes the basic concept of the half-rate CDR structure. Section 3 and Sect. 4 present the implementation and the measurement of the system, respectively, and Sect. 5 gives the conclusion at last.

2. Half-Rate Clock Recovery Architecture

Generally, a CDR synchronizes a clock to the data, so the clock frequency equals the data rate. However, it may be difficult to design a very high-speed oscillator that provides an adequate tuning range with reasonable jitter. For this reason, a CDR may sense the input data at full rate but employ a voltage-controlled oscillator (VCO) running at half the input rate [9], [10]. The generic structure of the CDR with a half-rate phase detector is shown in Fig. 1. It contains a half-rate phase detector (PD), a charge pump, a low-pass filter (LPF), a VCO and a decision circuit. The phase detector compares the phase of the incoming random data at a speed of 1 Gb/s to that of the 500-MHz clock signal generated by the VCO, and produces an error that is proportional to the phase difference between its two inputs. It is interesting to note that

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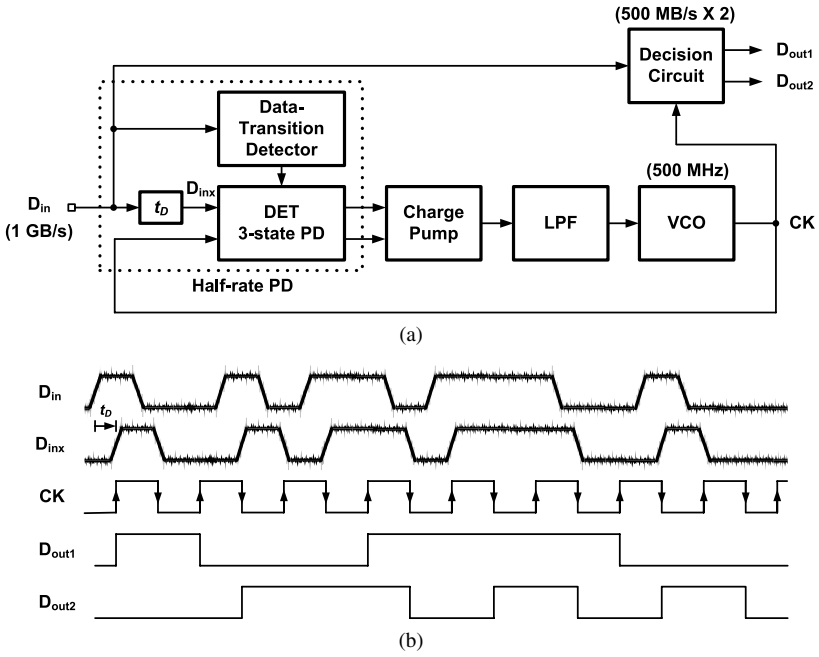


Fig. 1 (a) Generic half-rate CDR architecture with a clock recovery circuit and a data decision circuit. (b) Corresponding waveforms.

the phase detector operates at a half-rate speed because both clock edges sample the data waveforms. The error is then applied to a charge pump and a low-pass filter so as to generate the oscillator control voltage. In advance to reduce the jitter of the incoming data, the generated clock signal drives a decision circuit and retimes the data, generating two 500-Mb/s sequences, D_{out1} and D_{out2}. In a CDR the phase detector, which is formed by a delay element, a data-transition detector and a three-state phase detector, is the key element for providing the phase lock between the clock signal and the input data sequence. The task of the phase detector is to provide information about the timing distance between the zero crossing of the data and the clock. This information is used to set the control voltage of the VCO at a value required by the VCO to oscillate at the frequency of interest. When phase lock is achieved, this voltage stays constant and the phase detector output does not corrupt that. In this work, the delay element provides a delay time of about quarter period of the VCO, i.e., $t_D = T_{CK}/4$. Here, D_{inx} and CK are in phase as PLL is in lock. The phase detector locks such that the input data, D_{in}, leads the clock by $T_{CK}/4$, thereby the VCO can sample the data closer to the middle of the eye in the decision circuit. The detail operation of the half-rate phase detector will be discussed in the next section.

3. Circuit Description

A half-rate CDR scheme as well as a high-speed half-rate three-state phase detector, which reduces the clocking frequency by a factor of two, is described in this section.

3.1 Half-Rate Phase Detector for Random Data Stream

Three-state phase detectors are widely used in charge-pump PLL's. The circuit of these phase detectors can be realized in various forms. In designing a phase detector, there are usually two major concerns, including the inherent dead zone in the vicinity of the equilibrium point of the transfer curve and its maximum operating frequency. The former one should be taken care of in many PLL applications, such as frequency synthesizers, while the latter one is more crucial to CDR's since there is no frequency divider in their feedback paths to lower the operation frequency of the phase detectors. Conventional three-state phase detectors are composed of static logic gates. They suffer from the larger dead zone and low operation frequency. When the phase error is within in the dead zone, the charge pump does not effectively charge the filter, and the phase jitter may appear [11]. To improve these problems, a high-speed dynamic CMOS three-state phase detector is adopted in [12]. Since there is very short reset path within the phase detector, it can reduce the effect of a dead zone and operate at higher frequencies. However, these conventional three-state phase detectors are only applied to periodic input signals, and do not work while the input is with missing pulses [13]. The phase detector for random data must provide two essential functions: data transition detection and phase difference detection.

A half-rate CDR topology requires a phase detector that provides a valid output while sensing a full-rate random data stream and a half-rate clock. A half-rate phase detector for random data can provide two essential functions: (1) data transition detection in both positive and negative

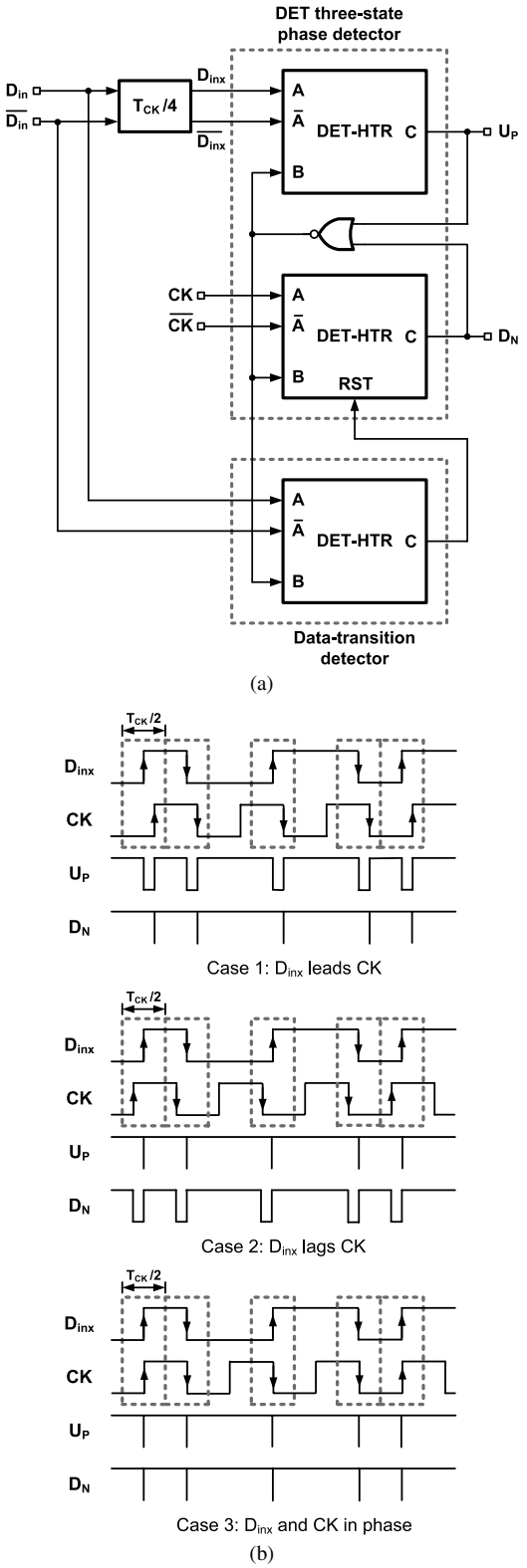


Fig. 2 Proposed half-rate phase detector for data stream. (a) Scheme. (b) Timing diagram.

edges, and (2) phase difference detection in a reasonable window. The proposed phase detector, developed to the random data stream with missing pulses, can be built with a

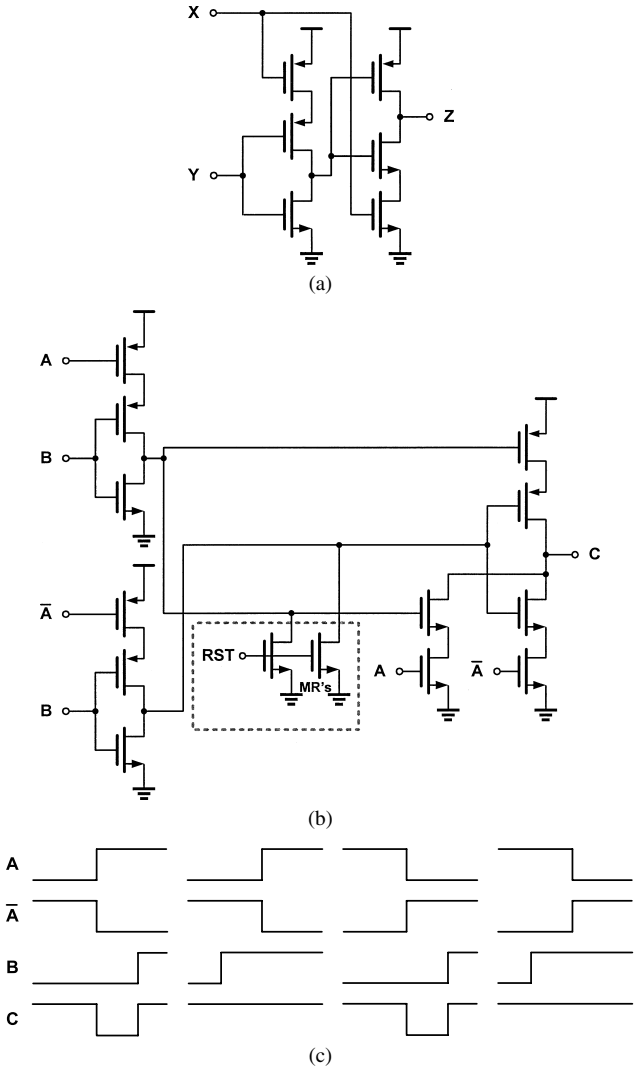


Fig. 3 (a) SET-HTR. (b) DET-HTR. (c) Timing diagram of (b).

delay cell, a standard three-state phase detector with an enable control signal and a data-transition detector as shown in Fig. 2(a). To arrive at a half-rate behavior, both positive and negative types of data transitions may be detected if both edges of the half-rate clock are utilized to sample the data as well as the detected window needs a width of $T_{CK}/2$, where T_{CK} is the period of the VCO. The conceptual operation of a half-rate phase detector is shown in Fig. 2(b).

Starting from the technique of the single-edge triggered (SET) half-transparent register (HTR) in Fig. 3(a) [14], we evaluate a prototype of a dynamic double-edge triggered (DET) HTR implementation. The dynamic DET-HTR circuit shown in Fig. 3(b) is based on the connection of two dynamic SET-HTR's grouped into a module. Figure 3(c) shows the timing diagram of DET-HTR. The DET-HTR with a reset is also shown in Fig. 3(b), and the control signal is applied only to pull-down NMOSFETs, MRs. If the MR's are biased active with a high input voltage, the appropriate drain nodes are pulled to low level, disabling the action of the HTR thereby the output of the HTR becomes high. Due

to the dynamic CMOS technique with small parasitic inherently, the phase detector can overcome the speed limitation and reduce the dead zone.

How does the phase detector detect data transitions? The data-transition detector senses the rising and falling edges of input data, D_{in}, generates a low signal (RST) and activates the three-state phase detector. If the operation of the phase detector is active, it will sense the transitions and detect the phase differences between the both inputs, D_{inx} and CK, where D_{inx} is a delay replica of the input data. Considering the delay cell with a delay, equal to a quarter period of the generated clock, $T_{CK}/4$, the phase detector has the largest locking phase range from $-\pi$ to $+\pi$. If the phase detector is disable, i.e., the control signal RST is high, all the outputs are set to high. Following edge detection, the phase detection is accomplished by the three-state phase detector, which measures the phase difference between the data and the clock and driving it toward the desired value as shown in Fig. 2(b).

3.2 Charge Pump and Loop Filter

The charge pump [15] and the associated low-pass filter are shown in Fig. 4. A common problem in the charge pump circuits is the phase offset resulting from the charge injecting errors induced by the parasitic capacitance of the switches and current source transistors. To mitigate this problem, the current source transistors are connected to the output node. In addition, the switching transistors are removed from the controlled voltage toward power supplies. In this way, the controlled voltage is isolated from the switching noise induce by the gate-to-drain overlap capacitance of the switching transistors. The low-pass filter is utilized to extract the DC component of the signals from the phase detector for the following VCO. It is realized in second order passive form and the overall system performance of a PLL is greatly affected by the loop filter design.

3.3 VCO

A VCO circuit shown in Fig. 5(a) is a multi-stage ring oscillator. In this circuit, a differential structure is selected for duty balanced clock pair generation, and device size and silicon layout are carefully done for the circuit matching. The ring oscillator is a fully integrable VCO that depends on a series of delay stages and an inversion in the signal path to produce the desired periodic output signal. Note that the signal eventually exhibits rail-to-rail swings. The oscillation frequency is determined by the propagation delay of the delay cells, which are simplified inverter form. Here the oscillation frequency can be found as

$$f_{osc} = \frac{1}{T_{CK}} = \frac{1}{2t_D} \tag{1}$$

where t_D is the overall delay time of the delay cells. Since the VCO is built with two symmetric blocks of the dashed box in Fig. 5(a), which employs a delay time of $t_D/2$, i.e., $T_{CK}/4$, this is the replica delay of the phase detector in Fig. 2(a). The VCO needs a current-starved delay cell, as shown in Fig. 5(b), for tuning frequencies. MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. Since the current sources limit

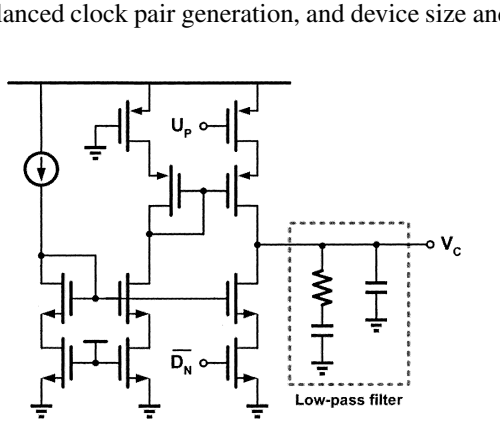
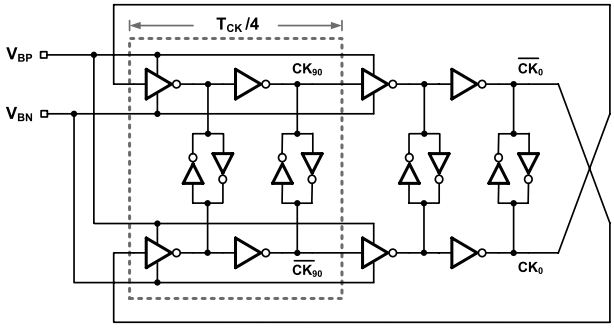
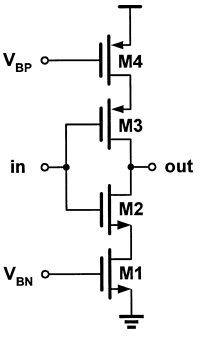


Fig. 4 Charge-pump scheme with a low-pass filter.



(a)



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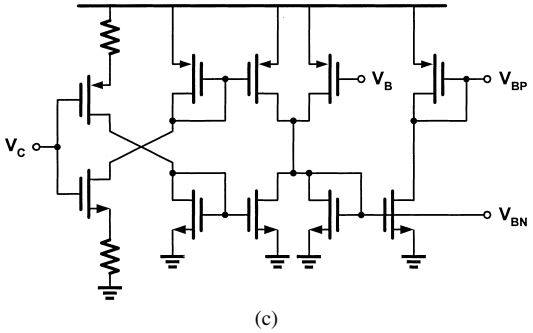


(c)

Fig. 5 VCO scheme. (a) Ring oscillator. (b) Delay component with bias control. (c) Bias circuit.

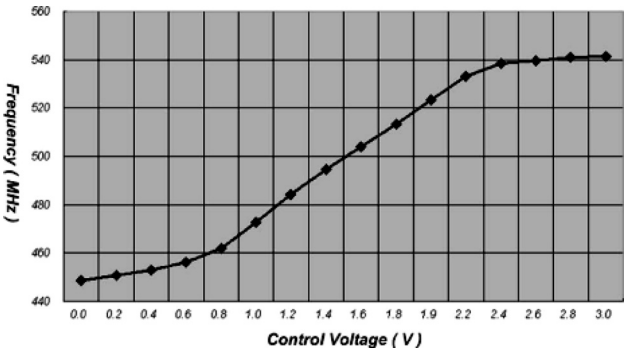


Fig. 6 Measured tuning characteristics of the VCO.

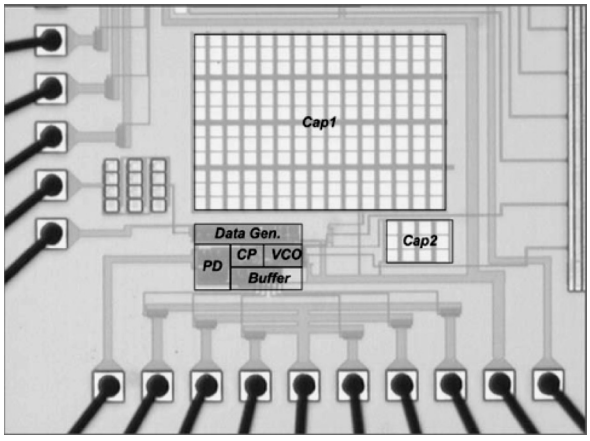


Fig. 7 Test-chip microphotograph.

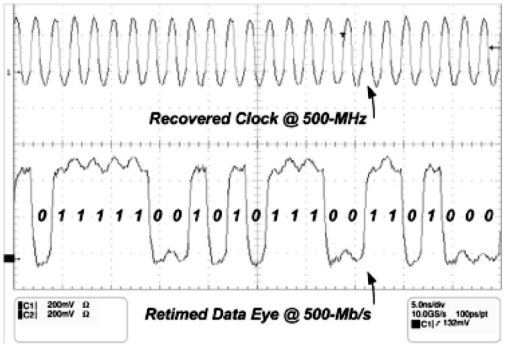
the current available to the inverter, the inverter is starved and its delay is controlled by the current. In the VCO, the latching action of the cross-coupled inverters is applied in each node. It can regenerate the analog signal into a full-scale digital signal. Figure 5(c) is a voltage-to-current converter for biasing the current-starved cells with a wide dynamic input range [16]. The bias voltage is generated by current summing and subtracting. In this configuration, the voltage to current conversion ratio can be adjusted by changing the input transistor size or its source resistance value. By the way, the external bias, V_B, is used to tune the operating range if the process varies. Figure 6 shows the measured VCO transfer function by varying the controlled voltage. The measured VCO has a monotonic frequency range of 448–541 MHz.

3.4 Decision Circuit

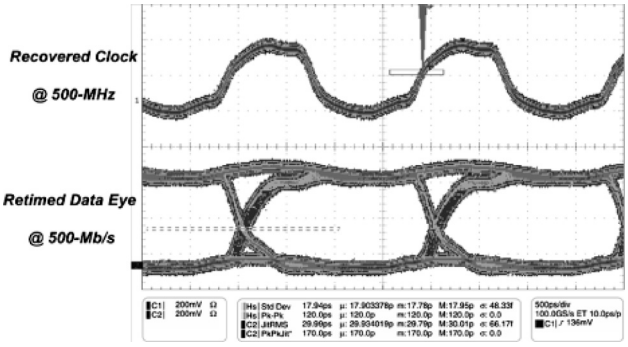
The decision circuit is made by TSPC DFF's of Yuan and Svensson [17], in which power consumption should be considered to be reduced.

4. Experimental Results

To verify the performance of the half-rate CDR as previously described, the proposed circuit has been fabricated



(a)



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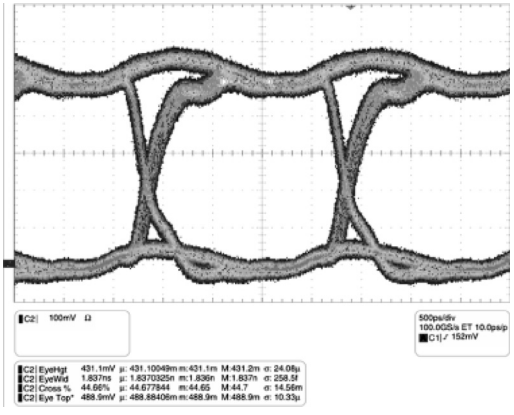

(c)

Fig. 8 Measured results for 1 Gb/s ($2^7 - 1$ PRBS). (a) Waveforms of the recovered clock and the retimed data. (b) Clock jitter and data eye diagram. (c) Data eye diagram analysis.

in a 0.35-μm double-poly N-well CMOS technology. Figure 7 shows the microphotograph of the half-rate CDR test chip. The loop filter is fully integrated in the chip by a poly resistor, 4.9 KΩ, and two double-poly capacitors, 200 pF and 13.3 pF. The core circuit occupies an active area of $750 \times 900\,\mu m^2$ excluding the output buffers and I/O pads. Each output signal is connected to a open-drain circuit with an externally match resistance of 50 Ω. The CDR is measured by using NRZ data with a pseudo-random binary sequence (PRBS) of $2^7 - 1$. The PRBS generator is built in the core chip. Figure 8 illustrates the recovered clock and the retimed data at 1-Gb/s data input. As can be seen, the measured rms and peak-to-peak jitter of the recovered clock

Table 1 Performance summary of the half-rate CDR @ 1-Gb/s $2^7 - 1$ PRBS.

Technology	0.35-μm CMOS
Supply voltage	3 V
Power	64.8 mW
VCO frequency range	448–541 MHz
Recovered-clock jitter	rms jitter : 17.9 ps pk-pk jitter: 120 ps
Retimed-data jitter	rms jitter : 29.9 ps pk-pk jitter: 170 ps
Active area	$750 \times 900\,\mu m^2$

is 17.9 ps and 120 ps, respectively. Also, to the retimed data, we add a decision circuit locked by the VCO output, and the measured rms and peak-to-peak jitter is 29.9 ps and 170 ps, respectively. The total power consumption of the CDR is measured to be 64.8 mW at a supply voltage of 3 V, in which the VCO dissipates 36.2 mW. Table 1 summarizes the overall specifications of the CDR.

5. Conclusion

PLL's incorporating sequential-logic with the three-state phase detectors have been widely used in recent years. However, they fail to work in the CDR's due to the input data stream with missing pulses. In this work, the three state-state phase detector is improved and realized for the NRZ random data stream. The choice of the CDR architecture is primarily determined by the speed limitation as well as the power dissipation and jitter requirement of the system. Unlike the traditional CDR structures, the half-rate CDR structure, where the half-rate phase detector is employed and the VCO runs at a frequency equal to half of the input data rate, is adopted in this work. A 1-Gb/s CDR incorporating the proposed half-rate three-state phase detector is realized in a 0.35-μm standard CMOS technology. The measured results demonstrate the functionality of the CDR with the proposed half-rate detector.

Acknowledgments

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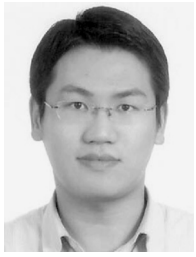

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