A Sub-1V Bandgap Reference Circuit Using Subthreshold Current

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Abstract — **A bandgap reference circuit employing subthreshold current is proposed. Only a small fraction of V_{BE} is utilized to generate the reference voltage of 170mV. Since the subthreshold current of MOSFET's is used as the current source, the circuit only consumes 2.4µW at supply voltage of 1V. It was fabricated using 0.18µm CMOS triple-well technology on chip area of 0.029*mm*^{2}. Both of the measurement and the simulation demonstrate the reference voltage variation is 1.3mV from -20°C to 100°C and is 1.1mV per volt for supply voltage from 0.95V to 2.5V.**

I. INTRODUCTION

The reference voltage generator is required in many analog and mixed-signal circuits, such as ADC, DAC, DRAM and flash memories, and so forth. It provides a constant reference voltage independent of process, temperature, and supply voltage variation. The bandgap reference (BGR) is the most stable and popular reference voltage generators [1][2]. However, the reference voltage is usually about 1.2V which requires the supply voltage to be over 1.5V, and thus limits the applications at very low supply voltages. Even though many efforts have been done to reduce the reference voltage lower then 1.2V for sub-1V operation [3][4], they required operational amplifiers (OP) which result in larger power consumption, larger chip area and more difficult OP design. The new trend tries to employ the subthreshold characteristics of MOSFET's to generate low reference voltages for sub-1V operation [5][6]. However, due to mobility and threshold voltage variation with temperature and process corners, the reference voltage variation is much larger than the BGR.

This work proposes a simple BGR circuit using subthreshold current without OP's for low-power sub-1V operation. The key idea is that a small fraction of V_{BE} in parasitic bipolar transistors and the difference of two V_{BE} 's are combined to generate the reference voltage of 170mV.

II. THE PROPOSED BGR CIRCUIT

Fig. 1 illustrates the simplified sub-1V BGR core circuit. The area ratio of NPN transistors Q_1 to Q_2 is *N*. The current source can be provided by a subthreshold current generator. If the base current of Q_2 is much smaller than the current through R1 and R2, the node voltage V_1 can be approximated as

$$V_1 = V_{BE2} + \frac{R1}{R2} V_{BE2} \tag{1}$$

Note that V_1 is proportional to V_{BE2} which has the negative temperature coefficient. If V_1 is subtracted from V_{BE1}, the reference voltage Vref (V_{CE2}) can be expressed as

$$\begin{aligned} V_{ref} &= V_1 - V_{BE1} \\ &= V_{BE2} + \frac{R1}{R2} V_{BE2} - V_{BE1} \\ &= \Delta V_{BE} + \frac{R1}{R2} V_{BE2} \end{aligned} \tag{2}$$

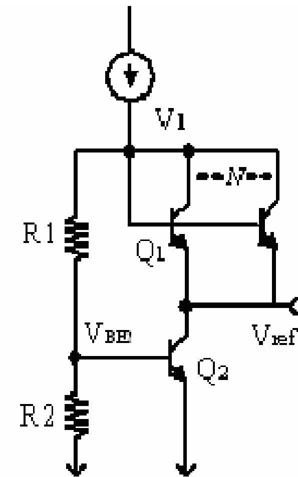

Fig. 1 The simplified BGR core circuit

If Q_1 is diode-connected and Q_2 is operated at forward active mode or near saturation, as long as the ratio (β) of the collector current (I_{C2}) to the base current (I_{B2}) is large enough, due to $I_{E1}= I_{C2}$, we may have

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \frac{KT}{q} \ln\left(\frac{\beta+1}{\beta} N\right) \approx \frac{KT}{q} \ln N \tag{3}$$

In our mixed-mode 0.18µm CMOS technology, the deep n-well process is a standard built-in layer for the p-type substrate wafers in order to have individual well potentials for any N-MOS and P-MOS transistors. Thus, there is no extra cost to have NPN parasitic transistors.

Since the NPN transistors are the parasitic components, the current gain $\beta = I_C/I_B$ can be expected not

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to be high. To verify β of the NPN transistor Q_2 is high enough, Fig. 2 demonstrates the β value is around 17 at room temperature when V_{BE} is 0.7V and V_{CE} is over 0.16V. In our design, the reference voltage equal to V_{CE} of Q_2 is 0.17V, which makes Q_2 close to saturation. Even though the β value is still quite close to the β = 18 at forward active mode, the BGR circuit still works well. However, if V_{CE} is chosen to be lower than 0.14V, the BGR circuit could not work normally, because Q_2 enters deep saturation and the base current in Q_2 is no longer negligible compared to the current through R1 and R2.

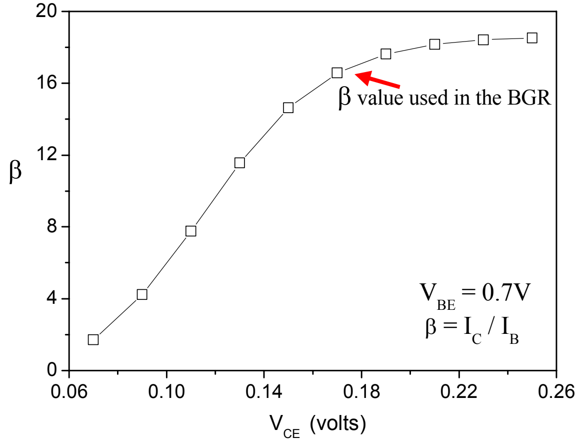

Fig. 2 The ratio (β) of the collector current (I_C) to the base current (I_B) is a function V_{CE} when V_{BE} = 0.7V.

After Eqn. (3) is substituted into Eqn. (2), the reference voltage is obtained.

$$V_{ref} = \frac{KT}{q} \ln N + \frac{R1}{R2} V_{BE2} \tag{4}$$

Since the ratio R1/R2 can be chosen to be smaller than one in order to have a fractional portion of bandgap reference, which is around 1.25V, the transistor ratio N can be smaller to generate low reference voltage, Vref. In our design, R1/R2=13/80 and N = 8. That is why it can be operated at supply voltage lower than 1V.

The complete BGR circuit shown in Fig. 3 includes the start-up circuit using M_6, M_7 and C_P, the subthreshold current generator composed of M_1 to M_4 and R_S, and the BGR core circuit utilizing M_5, Q_1, Q_2, R1 and R2. The detailed dimensions of the devices are listed in Table I.

The N-MOSFET's in the subthreshold current generator can be operated in strong or weak inversion depending on the current through M1 and M2. The smaller current can make them in weak inversion. Since the drain current in weak inversion can be expressed as [7]

$$V_{GS} = n\frac{KT}{q} \ln \frac{I_D}{(W/L)I_{D0}} \tag{5}$$

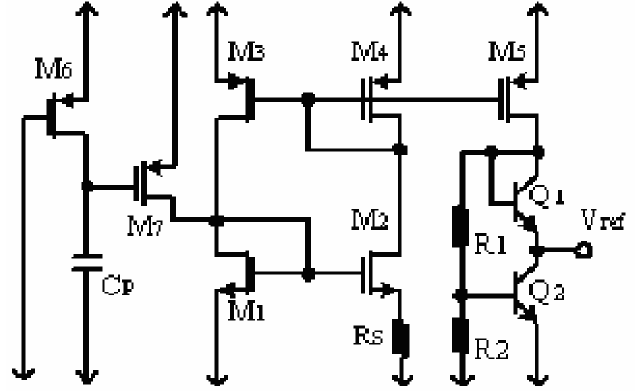

Fig. 3 The complete sub-1V BGR circuit including the start-up circuit

Thus, the voltage drop across RS is

$$V_{RS} = \Delta V_{GS} = V_{GS1} - V_{GS2} = n\frac{KT}{q} \ln\left[\frac{(W/L)_2 I_1}{(W/L)_1 I_2}\right] \tag{6}$$

where $n = 1 + C_d / C_{OX}$, C_d is the surface depletion capacitance, C_{OX} is the gate oxide capacitance. If I_1 is chosen to be equal to I_2 by using current mirrors of M_3 and M_4, the current through RS can be written as

$$I_2 = \frac{V_{RS}}{R_S} = \frac{n}{R_S}\frac{KT}{q} \ln\left[\frac{(W/L)_2}{(W/L)_1}\right] \tag{7}$$

Therefore, the currents through M_1 and M_2 are nearly independent of the supply voltage. Even though the current may be slightly increased as the temperature is increased, the currents in the NPN transistors are also increased. The more important point is the voltage drop in the NPN transistors is a logarithmic function of current. The reference voltage can still keep nearly constant for small current variations.

Table I The device parameters for Fig. 3

Device	W/L	Device	Resistance
M_1	2/2	R1	130 KΩ
M_2	100/2	R2	800 KΩ
M_3	25/6	RS	350 KΩ
M_4	25/6	Device	Emitter area
M_5	28/2	Q_1	2μm×2μm×8
M_6	1/20	Q_2	2μm×2μm
M_7	60/1		

The other important issue in the subthreshold current generator is the existence of bi-stable bias points, one of which may turn off the current generator. Therefore, the start-up circuit was used to drive the circuit to the desired bias point when the supply is turned on. The operation is that M_6 provides a current to charge C_P. If the gate voltage of M_7 is not high enough, the drain current of M_7 charges

the gate voltages of M_1 and M_2 to the desired bias level. M_7 stops conducting current until its gate voltage is high enough, so the start-up circuit does not consume any power after the BGR circuit reaches the steady state.

III. SIMULATION AND MEASUREMENT RESULTS

The sub-1V and subthreshold BGR circuit was designed and fabricated using 0.18μm triple-well CMOS technology. The parasitic n+/p-well/deep n-well structure provides the NPN bipolar transistors. Even though the forward active current gain (I_C/I_B) is only around 18, it is good enough in our applications. Note that the triple well structure makes Q_1 stacking on Q_2 possible, since either their collectors or their emitters do not have to be connected together. Unlike the parasitic p+/n-well/p-substrate PNP transistors, any two collectors must be tied together. For the three resistors with large resistance, the n-well was used to minimize the chip area. To measure the reference voltage, an extra unity gain buffer was also included. Fig. 4 shows the die microphotograph. The chip area without pads is about 0.029mm^2.

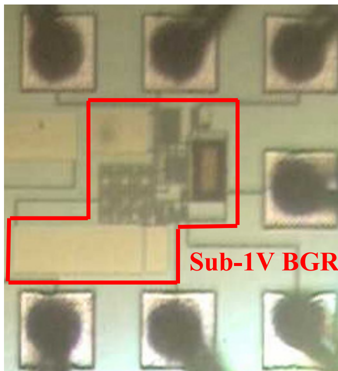

Fig. 4 Microphotograph of the proposed BGR circuit occupying the chip area of 0.029 mm^2 without pads

Fig. 5 demonstrates the waveform of the sub-1V BGR circuit when the power supply is just turned on. The time for the reference voltage reaches 170mV within 15ms which is shorter than the supply voltage switching time of 20ms, since the circuit starts to work at the supply voltage lower than 1V.

In Figs. 6 and 7, FF, TT and SS represent the simulated results of the fast, typical and slow process corners at -20°C, 25°C, and 100°C, respectively. The measurement results well agree with the simulation data. Note that the measured data increased and decreased by steps is due to the resolution limitation of our oscilloscope. In Fig. 6, the measured reference voltages confined in the FF and SS corners almost keep the same value of 170mV for supply voltage from 0.95V to 2.5V. Fig. 7 shows the variation of reference voltages as functions of temperature at supply voltage of 1V. Even though there are small deviations between the measured and simulated data, the measured values are within the same range and with the same trend of simulated results. It is worth noting that the variations of reference voltages for different process corners are much smaller than those using threshold voltages [5][6] instead of bandgap.

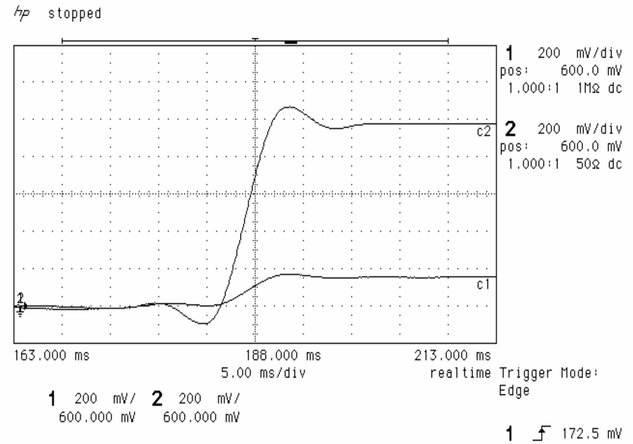

Fig. 5 The waveform of the reference voltage when the power supply is just turned on

Table II summarizes the performance.

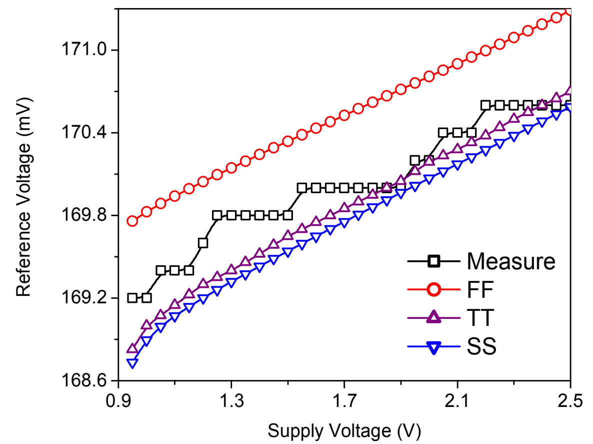

Fig. 6 The measured data are within the variation of different process corners at room temperature.

IV. CONCLUSIONS

The proposed simple bandgap voltage reference circuit using parasitic NPN transistors without OP's achieves sub-1V and low-power operation. The circuit was fabricated using 0.18μm CMOS triple-well technology on chip area of 0.029mm^2. The variation of reference voltage is very small for various temperatures, supply voltages and process corners. The measurement results confirm those superior characteristics. It should be very useful to be applied to many analog circuits for sub-1V operations.

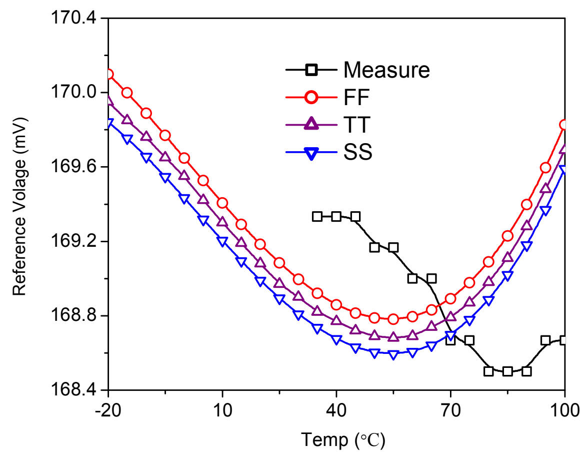

Fig. 7 Comparison of Measurement and data from different process corners for various temperatures at 1V supply voltage

Table II The specifications of the proposed CMOS BGR circuit design

Technology	0.18μm CMOS
Supply voltage	0.95V ~ 2.5V
Reference voltage	169.4mV
Voltage variation (-20°C ~ 100°C at V_{DD}=1V)	0.76%
Voltage variation (V_{DD} = 1V ~ 2.5V)	1.1mV/V
Total current (V_{DD}=1V)	2.4μA
Total resistance	1280KΩ
Total Number of NPN transistors (One is 8 times larger than the other.)	2
Area	$0.029mm^2$

ACKNOWLEDGMENT

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