

A High-Voltage Tolerant Interface Circuit for Embedded CMOS Non-volatile Memories

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1. Introduction

The advanced CMOS technologies push nano-scale geometries of MOSFETs. To avoid high electric field stresses, the operating voltages become lower and lower. However, in some applications high-voltage interfaces are still required, such as MEMS device control, power convertor switching, embedded non-volatile memory control circuits, and so on. The on-die high-voltage interface in the standard CMOS processes is a key component to make the system perform correct functions.

To design a high-voltage interface circuit, the voltage drops between any two electrodes of a MOSFET have to be well controlled for good reliability. The high-voltage drivers using large capacitors had been reported^{1,2)}. The interface with tri-state was designed for $3V_{DD}$ output³⁾, but the voltage drops between drain and source may have risks of overstress. Besides, it needs four transistors in series instead of three at the output stage. The voltage drops between the gate and the body of the other I/O driver⁴⁾ also have overstress issues. In this abstract, a high-voltage tolerant interface is proposed for embedded CMOS non-volatile memories⁵⁾. Due to grounded bodies of NMOS transistors in the $0.35\mu\text{m}$ twin-well CMOS process, we propose an special interface circuit without large capacitors and overstress with good driving capability.

2. Circuit Structure

Figure 1 shows the interface marked by the bolded lines is placed between the high-voltage source such as 7V generated by the charge pump and the multiple-time-program (MTP) cells in the standard $0.35\mu\text{m}$ CMOS process⁵⁾. The bit-line of the memory cell requires 7V or 0V during program or erase, and is floated during read. Note that the bias for the floated bit-line (Vout) is less than V_{DD} .

The proposed interface consists of a level shifter and a driver with a select signal (S) to drive the bit-line as shown in Fig. 2. It requires two voltage sources, $V_{DD} = 3.5\text{V}$ and $V_{DDH} = 7\text{V}$, one input signal (V_{in}) and one controlling signal (S). When $S = 0\text{V}$, the output (Vout) is floated. On the other hand, if $S = V_{DD}$, the output will be V_{DDH} or 0 according to the input signal (V_{in}).

3. The high-Voltage Driver and the Level Shifter

Figure 3 illustrates the high-voltage driver has a pair of two NMOS and two PMOS transistors in series with two nodes n1 and n2 determined by two PMOS transistors Mp3 and Mp4. V_{DDH} was selected as $2V_{DD}$ in our design. Note that the bodies of all NMOS transistors have to be grounded owing to the twin-well process. Therefore, some

of the NMOS transistors were replaced by PMOS transistors if possible for both circuits in Fig. 3 and 4. For example, Mp3 is a PMOS transistor with its source tied to body instead of a NMOS transistor. The only possible risk of overstress is the reverse PN junction bias between the drain of Mn2 and its body, which should be fine in the our design using the $0.35\mu\text{m}$ CMOS process.

The node voltages of three possible operation situations are listed in Table I. For $S = V_{DD}$ and $V_{in} = V_{DD}$, Mn1, Mn2 and Mp3 are on to make Vout grounded, and n1 is set to V_{DD} to avoid overstress of the four PMOS transistors. For $S = V_{DD}$ and $V_{in} = 0$, Mp1, Mp2 and Mp4 are on to raise $V_{out} = V_{DDH}$, and n2 becomes V_{DD} to control overstress, too. The third case is $S = 0$ and $V_{in} = V_{DD}$, Mp2 and Mn2 are off, so Vout is floated, which allows Vout varying from 0 to V_{DD} .

The proposed level shifter provides the control signals of the driver as shown in Fig. 4. The transistors on the right hand side and the left hand side of the two dash lines can make sure the swings of I_s and I_{sb} are between V_{DD} and V_{DDH} . Beside, they can generate large swing signal I_{sd} for the driver. Since the level shifter does not need high current driving capability, the device sizes can be selected as small as possible.

4. Simulation and Measurement Results

The post-layout simulated waveforms of the proposed circuit are shown in Fig. 5 with the output capacitance 0.5pF at 50MHz . The node voltages are well controlled to avoid overstress within any transistors at steady states.

The microphotograph of the die for the proposed interface is given in Fig. 6. The measured waveforms of the output and the input with $S = V_{DD}$ are demonstrated in Fig. 7. The output is successfully switched between 0 and V_{DDH} . Note that the longer delay is due to loading effect in the measurement environment. The delay time should be much shorter if the interface circuit is used within the chip.

To test the floated status with S varying between 0 and V_{DD} , the output is connected to an external resistor with the other electrode biased at 1V. The measured waveforms are shown in Fig. 8. It can be observed that the output gradually becomes 1V when $S = 0$. Since the external resistance is large, the variation is also slow.

5. Conclusions

The high-voltage tolerant tri-state interface circuit for embedded CMOS non-volatile memories is proposed and fabricated. The measurement results demonstrate the correct functions. The output stage of the driver only needs two transistors in series for pull-up or pull-down, which helps enhance driving ability. In addition, the limitation of

grounded body bias of NMOS transistor was overcome by using the PMOS transistors. It is convinced that it is a good reliable interface circuit for many higher-than- V_{DD} swing embedded applications using the standard CMOS technologies.

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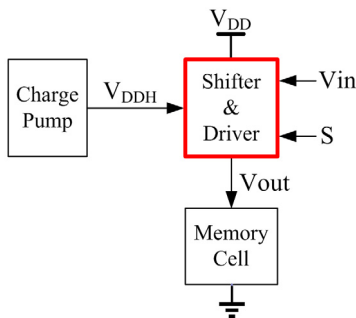


Fig. 1 The role of the interface circuit used in the embedded memory

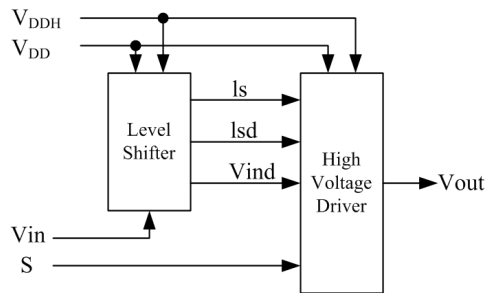


Fig. 2 The interface circuit consists of two circuit blocks.

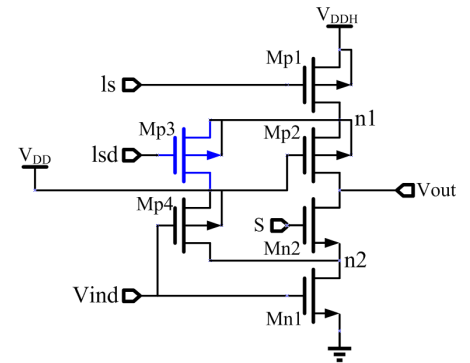


Fig. 3 The high-voltage driver for the bit-line of memory cell

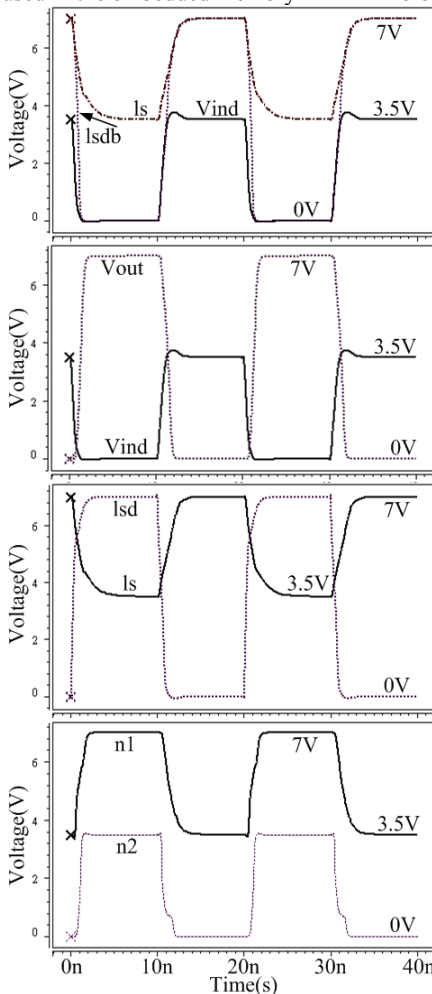


Fig. 5 Simulated waveforms of the node voltages with the output capacitance of 0.5pF at 50MHz

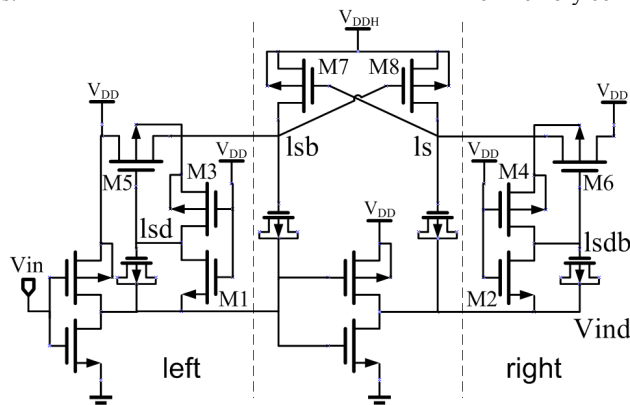


Fig. 4 The level shifter provides the three control signals (lsd, ls and Vind) for the driver.

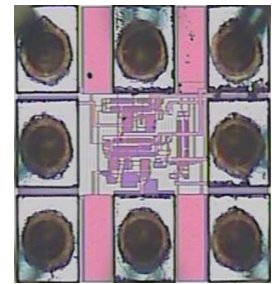


Fig. 6 Microphotograph of the proposed interface circuit.

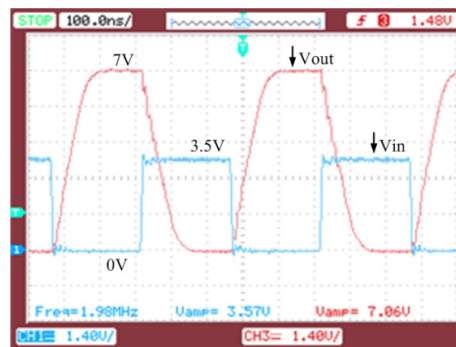


Fig. 7 The measured input and output waveforms at 2MHz

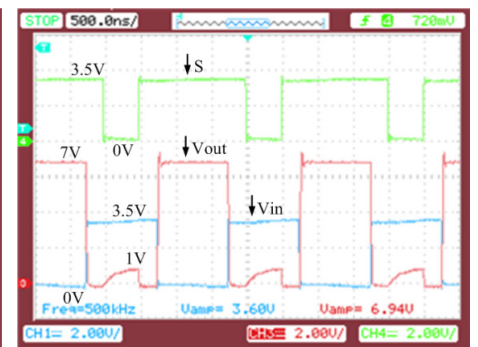


Fig. 8 The measured waveforms with the floated output are demonstrated at 500kHz.

Table I The corresponding node voltages for different output statuses in the interface circuit

Vin	S	Vind	ls	lsd	n1	n2	Vout
V_{DD}	V_{DD}	V_{DD}	V_{DDH}	0	V_{DD}	0	0
0	V_{DD}	0	V_{DD}	V_{DDH}	V_{DDH}	V_{DD}	V_{DDH}
V_{DD}	0	V_{DD}	V_{DDH}	0	V_{DD}	0	Floated