A High-Voltage Tolerant Interface Circuit for Embedded CMOS Non-volatile Memories

ChihYang Huang and Hongchin Lin

Dept. of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan
Phone: 886-4-2284-0688 ext. 250 e-mail: hclin@dragon.nchu.edu.tw

1. Introduction
The advanced CMOS technologies push nano-scale geometries of MOSFETs. To avoid high electric field stresses, the operating voltages become lower and lower. However, in some applications high-voltage interfaces are still required, such as MEMS device control, power converter switching, embedded non-volatile memory control circuits, and so on. The on-die high-voltage interface in the standard CMOS processes is a key component to make the system perform correct functions.

To design a high-voltage interface circuit, the voltage drops between any two electrodes of a MOSFET have to be well controlled for good reliability. The high-voltage drivers using large capacitors had been reported1,2). The interface with tri-state was designed for 3V DD output3), but the voltage drops between drain and source may have risks of overstress. Besides, it needs four transistors in series in stead of three at the output stage. The voltage drops between the gate and the body of the other I/O driver also have overstress issues. In this abstract, a high-voltage tolerant interface is proposed for embedded CMOS non-volatile memories5). Due to grounded bodies of NMOS transistors in the 0.35μm twin-well CMOS process, we propose an special interface circuit without large capacitors and overstress with good driving capability.

2. Circuit Structure
Figure 1 shows the interface marked by the bolded lines, the voltage drops between any two electrodes of a MOSFET have to be well controlled for good reliability. The high-voltage drivers using large capacitors had been reported1,2). The interface with tri-state was designed for 3V DD output3), but the voltage drops between drain and source may have risks of overstress.

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3. The high-Voltage Driver and the Level Shifter
Figure 3 illustrates the high-voltage driver has a pair of two NOMS and two PMOS transistors in series with two nodes n1 and n2 determined by two PMOS transistors Mp3 and Mp4. V DDH was selected as 2V DD in our design. Note that the bodies of all NMOS transistors have to be grounded owing to the twin-well process. Therefore, some of the NMOS transistors were replaced by PMOS transistors if possible for both circuits in Fig. 3 and 4. For example, Mp3 is a PMOS transistor with its source tied to body instead of a NMOS transistor. The only possible risk of overstress is the reverse PN junction bias between the drain of Mn2 and its body, which should be fine in the our design using the 0.35μm CMOS process.

4. Simulation and Measurement Results
The post-layout simulated waveforms of the proposed circuit are shown in Fig. 5 with the output capacitance 0.5pF at 50MHz. The node voltages are well controlled to avoid overstress within any transistors at steady states.

The microphotograph of the die for the proposed interface is given in Fig. 6. The measured waveforms of the output and the input with S = V DD are demonstrated in Fig. 7. The output is successfully switched between 0 and V DDH. Note that the longer delay is due to loading effect in the measurement environment. The delay time should be much shorter if the interface circuit is used within the chip.

To test the floated status with S varying between 0 and V DD, the output is connected to an external resistor with the other electrode biased at 1V. The measured waveforms are shown in Fig. 8. It can be observed that the output gradually becomes 1V when S = 0. Since the external resistance is large, the variation is also slow.

5. Conclusions
The high-voltage tolerant tri-state interface circuit for embedded CMOS non-volatile memories is proposed and fabricated. The measurement results demonstrate the correct functions. The output stage of the driver only needs two transistors in series for pull-up or pull-down, which helps enhance driving ability. In addition, the limitation of
grounded body bias of NMOS transistor was overcome by using the PMOS transistors. It is convinced that it is a good reliable interface circuit for many higher-than-\(V_{DD}\) swing embedded applications using the standard CMOS technologies.

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**References**