A Reduced-Ripple PMOS Charge Pump Circuit with Small Filtering Capacitors

Boy-Ying Jaw and Hongchin Lin

Dept. of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan
Phone: 886-4-2284-0688 ext. 250 e-mail: hclin@dragon.nchu.edu.tw

1. Introduction
The charge pump (CP) circuit has been widely used in MEMS, flash memories, EEPROM, and so on. It is usually used as a simple on-die DC-DC voltage converter, to provide voltages higher than the supply voltage. Most of the charge pumps are based on the Dickson structure using MOS transistors\(^3\). The PMOS based versions\(^2,3,4\) can effectively reduce the degradation due to threshold voltage and body effect. Besides, the simple CP\(^2,3,4\) enhance the performance without device reliability issues. However, all the existing CP circuits require large filtering capacitance at the output to reduce ripples, so extra chip area is needed if the CP is embedded on the chip. The parallel CP\(^5\), which may suffers from reliability, splits the CP into \(N\) parallel modules to minimize ripples. However, it needs the complex delay clock circuit and high \(N\) values to reduce reverse charging leakage. In this abstract, two two-step clock patterns at the last stage were designed for the two-phase PMOS CP\(^2,3,4\). The results show the ripple of output voltage is significantly reduced without degrading pumping ability.

2. Clock Scheme for Ripple Reduction
The two-stage PMOS CP circuit with two out-of-phase clocks \(\phi_1\) and \(\phi_{1b}\) with amplitudes varying from 0 to \(V_{DD}\) is shown in Fig. 1. The first stage of the PMOS CP consists of six transistors, a pair of boosting capacitors, \(C_1\) and \(C_2\), and a pair of auxiliary capacitors, \(C_{a1}\) and \(C_{a2}\). \(\phi_{a1}\) and \(\phi_{a2}\) are generated using \(\phi_1\) and \(\phi_{1b}\) to produce two-fold amplitudes of clocks. The second stage is identical to the first stage, except the two special two-step clocks \(N_{ck1}\) and \(N_{ck2}\) are used to replace \(\phi_1\) and \(\phi_{1b}\) in our previous work\(^2,3,4\). The reason is that when the transistor \(M_o\) or \(M_{12}\) is fully turned on, charges instantaneously transfer to the filtering capacitor (\(C_o\)) at the output. The theoretical maximum value can be expressed as

\[
V_o = \frac{T}{2(C + C_o)} I_L
\]

(1)

where \(T\) is the period; \(I_L\) is the output current; \(C\) is the boosting capacitance.

Without increasing \(C_o\), if the turn-on resistance \(r_{on}\) of the PMOS transistors is increased, the ripple can be reduced, but the charge in \(C\) may not be transferred to \(C_o\) completely, which could influence pumping ability and have to be controlled carefully. Note that \(r_{on} \approx L/\mu C_w W_{on}\), where \(V_{on}\) is equal to \(|V_{GS}| - |V_t|\). The proposed clocks \(N_{ck1}\) and \(N_{ck2}\) shown in Fig. 2 can adjust \(V_{on}\) during charge transferring so that the ripple can be reduced effectively without degredation of voltage gain and driving capacity. These two clocks stay at the voltage levels \(V_{L1}\) and \(V_{L2}\) for a while before returning to zero. Therefore, \(r_{on}\) is higher in the beginning of charge transfer than in the rest of the turn-on period.

3. The Clock Generation Circuit
The boosting capacitors of second stage are driven by the two-step clocks \(N_{ck1}\) and \(N_{ck2}\) shown in Fig. 2. The circuits to generate \(N_{ck1}\) and \(N_{ck2}\) are sketched in Fig. 3. The control signals \(\phi_1\), \(\phi_2\), \(Q_1\), \(Q_2\), \(A_1\) and \(B_1\) are illustrated in Fig. 2. The overlapping time \(T_D\) between \(\phi_1\) and \(\phi_2\) is equal to \(T_1\) and \(T_2\). According to Fig. 2, \(Q_1, Q_2, A_1\) and \(B_1\) are obtained using simple logic gates with \(\phi_1\) and \(\phi_2\) as the inputs.

During time \(T_1\), the signals \(\phi_1\), \(Q_1\), and \(A_1\) are low, \(Q_2\), is high. \(M_{k1}\) and \(M_{k2}\) are on to transfer charges from \(V_{DD}\) to \(C_{i1}\) and \(C_{i2}\), respectively, while \(M_{k3}\) and \(M_{k4}\) are off, so \(N_{ck1}\) goes to \(V_{DD}\). At time \(T_2\), \(\phi_1\) and \(A_1\) are high, while \(Q_2\) is low, thus \(M_{k1}\) is off and \(M_{k2}\) transfers charges from \(C_{i2}\) to \(C_{i1}\). By adjusting the ratio between \(C_{i1}\) and \(C_{i2}\), the voltage level \(V_{L1}\) and \(V_{L2}\) can be determined. During time \(T_1\), \(A_1\) is 0 and \(Q_1\) goes to \(V_{DD}\), therefore, \(N_{ck2}\) drops to 0. In the time interval \(T_D\), since \(\phi_1\) and \(Q_1\) are lowered to 0, \(N_{ck1}\) becomes \(V_{DD}\). \(N_{ck2}\) can be generated via the other circuit in Fig. 3 with the similar operation of \(N_{ck1}\).

4. Simulation and Measurement Results
The proposed reduced-ripple PMOS charge pump was designed and fabricated using the twin-well 0.35\(\mu\)m CMOS process. The boosting, auxiliary, and filtering capacitors of \(5\ pF, 0.5\ pF\), and \(5\ pF\) were used. Figure 4 shows the waveforms of \(N_{ck1}\) and \(N_{ck2}\) as well as compares the simulated output waveforms of the existing CP\(^2,3,4\) and the proposed CP with \(I_{out} = 20\mu A\) at 10MHz and \(V_{DD} = 1.8V\). The proposed CP has smoother rising edges than the existing CP does. It also has reduced ripples with two humps in one half cycle of a period due to the two-step clocks.

Figure 5 compares the simulated output ripples of the existing CP\(^2,3,4\) and the proposed CP with \(T_D = 10\)ns for different output currents at a frequency of 10MHz and \(V_{DD} = 1.8V\). For higher output current, the improvement of ripple reduction is even more pronounced.

Figure 6 shows the chip microphotograph of the proposed CP on the area of 0.182mm\(^2\). Figure 7 demonstrates the output ripple measured using the AC-coupled method at \(V_{DD} = 2.2V\) with fitting curves in dash lines. Figure 8 plots the measured output voltages of the proposed CP for various supply voltages at 10MHz and \(I_{out} = 0\). That indicates the CP has good pumping ability for \(V_{DD}\) from 1.4V to 3.0V. Figure 9 illustrates the measured ripples of output voltage for different \(T_D\)'s and \(I_{out} = 20\mu A\) and \(40\mu A\) at 10MHz and \(V_{DD} = 1.8V\). The ripples are decreased when \(T_D\) is increased from 0ns to 10ns. Due to parasitic effects of the package and the testing fixture, the
ripples are higher in measurement.

5. Conclusions
The proposed clock scheme for the PMOS CP fabricated in the 0.35μm CMOS process saves chip area of on-die filtering capacitors and can efficiently reduce ripples which can be adjusted by the overlapping time $T_D$. Experimental results reveal that the ripples are reduced by about 50% at 10 MHz and $V_{DD} = 1.8V$ using small filtering capacitors. We can expect that the more area reduction will be achieved if the boosting capacitors are larger to provide higher output current.

Acknowledgements --- The authors would like to acknowledge the Chip Implementation Center (CIC) of the National Applied Research Laboratories (NARL) of Taiwan for the support in chip fabrication. This work was supported by National Science Council of Taiwan (NSC 98-2221-E-005-078).

References