A 20/40-GHz Dual-Band Voltage-Controlled Frequency Source in 0.13-μm CMOS

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***Abstract*—An LC-type voltage-controlled oscillator (VCO) and a push–push frequency doubler are presented for 20/40-GHz dual-band design in standard 0.13-μm CMOS. Combining the varactor with the transconductance-tuned regime, the VCO is realized to arrive at the range extension for high-frequency operation. In addition, a technique using sensitivity distribution is adopted to achieve linear tuning range. The VCO provides the tuning range of 19.8–22.6 GHz, and the measured phase noise at 21.2-GHz frequency is −105.7 dBc/Hz at a 1-MHz offset. The doubler following the VCO can provide twice the frequency over the tuning range and generate output with better fundamental rejection resulting from the notch characteristic. The measured phase noise of the doubler at 42.4-GHz frequency is −94.6 dBc/Hz at a 1-MHz offset while dissipating 8 mW in the whole circuit.**

***Index Terms*—Frequency doubler, fundamental rejection (FR), mutual negative resistance, voltage-controlled oscillator (VCO).**

I. Introduction

VOLTAGE-CONTROLLED oscillators (VCOs) and frequency doublers are important components in microwave and millimeter-wave communications [1]. Since it is difficult to achieve low phase-noise oscillators at high frequencies, an active doubler preceded by a lower frequency high-spectral-purity VCO is a practical way to build a cost-effective and stable source [2]–[5]. Moreover, since the VCO is based on a narrowband regime, the narrowband analog frequency doubler may be more suitable for this application to reduce power consumption and increase the maximum operation frequency. With a half-rate feature, the VCO can provide more reasonable tuning range and lower power consumption.

Fig. 1 depicts the receiver architecture with two down-conversion stages, using a first local oscillator (LO) frequency of $2\omega_0$ and a second LO frequency of ω_0. Based on the dual-conversion architecture, the receiver can employ a single LO to simplify the frequency planning and the design of the building blocks. The architecture has also several advantages over typical homodyne or heterodyne counterparts, which was discussed in [6]. The LO-related challenges prove so severe at millimeter-wave frequencies that the choice of the receive (RX) and transmit (TX) topologies becomes closely intertwined with the LO design. For example, the 60-GHz receiver shown in Fig. 1 requires generation of the first LO at 40 GHz and the second LO at 20 GHz is the division of f_{LO1} [7]. However, a difficult task exists in the oscillation circuit because inductor Q's begin to saturate and varactor Q's are likely to fall to low levels at such high frequencies. To ameliorate this difficulty, a simple and low-cost solution to the receiver can employ a 20-GHz oscillator for the second LO and a frequency doubler for the first LO. In addition, the issue on a tuning range is also the other challenge of high-frequency LO design because the tuned component, e.g., varactor, suffers from a tradeoff between the tuning range and the operating frequency. In order to maximize both the tuning range and the operating frequency, the capacitances existing in the VCO's tank become crucially designed factors. The capacitances of the tank can be formed from an effective parasitic capacitor and a varactor, and their values can be viewed as the sum of a voltage-controlled variable capacitance and a nonvariable capacitance. The nonvariable one is mainly contributed by the parasitic effects from the inductor, varactor, and transistors, and limits the tuning ranges and reduces the operating frequency. As a result, the VCO suffers from a tradeoff between the tuning range and the operation frequency [27]. Thus, a half-rate VCO combined with a frequency doubler can provide more reasonable tuning range than a full-rate VCO with a divide-by-2 circuit.

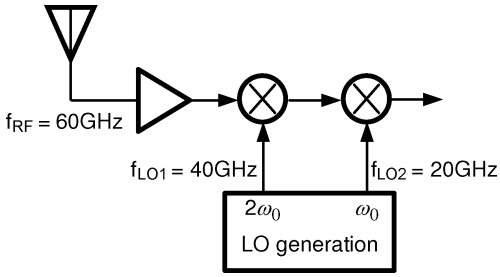

Fig. 1. Receiver architecture with an example of frequency planning.

In this study, the VCO and doubler are demonstrated in a 0.13-μm CMOS process for 20/40-GHz dual-band design. In the circuits, several features exist to improve the prior circuits. First, the VCO combining mutual-negative-resistance [8]–[10]

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and negative-transconductance techniques is developed to extend the operating frequency range. Secondly, to achieve linear tuning, the VCO introduces a method of distributed sensitivities. In addition, the frequency doubler behind the VCO uses a push–push structure with a notch filter to achieve a good fundamental rejection (FR).

This paper is organized as follows. The proposed VCO using mutual-negative-resistance and negative-transconductance techniques is developed in Section II, and its range-extended functionality is illustrated. Section III addresses the notch frequency doubler. Section IV shows the chip implementation and the measurement of the circuits. Section V gives the conclusion.

II. Frequency-Extended VCO

In order to maximize both tuning range and operating frequency, the capacitances existing in the VCO's tank become crucial design factors. The capacitances can be formed from an effective parasitic capacitor and a varactor, and their values can be viewed as the sum of a voltage-controlled variable capacitance and a nonvariable capacitance. The nonvariable one is mainly contributed by the parasitic effects from the inductor, varactor, and transistors, and it limits the tuning range and reduces the operating frequency. In this work, a mutual-negative-resistance VCO with a frequency-extended regime is presented.

A. VCO Schematic

In order to overcome the limitations of wide-range design at high frequencies, a VCO combining mutual-negative-resistance and negative-transconductance techniques is developed in Fig. 2(a). The scheme is divided into two parts: a mutual-negative-resistance circuit and a negative-transconductance circuit. Besides the effective values of the inductor and capacitor in the tank, the oscillation frequency also depends upon the transconductance of the active components, as will be discussed next.

B. Oscillation Analysis

The oscillator could be viewed as two independent VCOs with the cross-coupling mechanism to synchronize the two half-circuit VCOs into differential operation. Due to $v_{o+} = -v_{o-}$, the equivalent half circuit is shown in Fig. 2(b). Note that g_{m1} and g_{m2} are the transconductances of $M_{1\mathrm{A}} - M_{1\mathrm{B}}$ and $M_{2\mathrm{A}} - M_{2\mathrm{B}}$ transistors, respectively, and L_1, L_2, C_1, and C_2 are the inductances and effective capacitances in each node. R_1 and R_2 represent the series parasitic resistances associated with the primary and secondary coils and are included to account for the losses in the coils, and the inductive coupling coefficient between two coils is modeled by k_1. It is interesting to note that the negative resistance $-1/g_{m1}$ generated by the negative transconductance circuit is determined by a control bias. The circuit of Fig. 2(b) with open-loop analysis can be exploited to construct the equivalent circuit in Fig. 3. The transfer function in the circuit of Fig. 3 yields

$$T(s) = \frac{v_o}{v_i} = \frac{s g_{m2} k_1 L_1}{s^4 A_4 + s^3 A_3 + s^2 A_2 + s A_1 + (1 - g_{m1} R_1)} \tag{1}$$

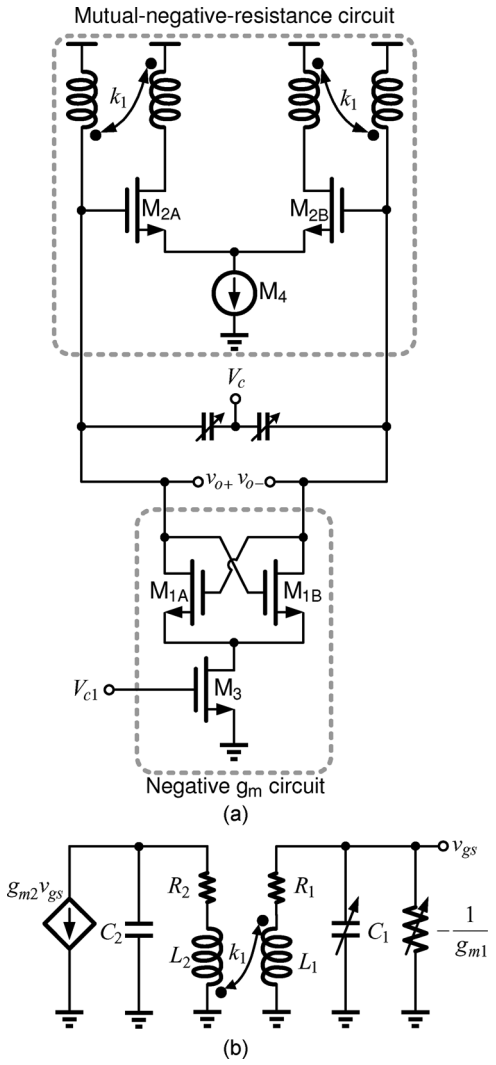

Fig. 2. (a) Proposed VCO combining negative-transconductance and mutual-negative-resistance circuits. (b) Half-circuit equivalent.

where

$$A_4 = \left(1 - k_1^2\right) L_1^2 C_1 C_2 \tag{2}$$

$$A_3 = 2R_1 L_1 C_1 C_2 - g_{m1}\left(1 - k_1^2\right) L_1^2 C_2 \tag{3}$$

$$A_2 = L_1(C_1 + C_2) + R_1^2 C_1 C_2 - 2 g_{m1} R_1 L_1 C_2 \tag{4}$$

and

$$A_1 = R_1(C_1 + C_2) - g_{m1}\left(L_1 + R_1^2 C_2\right). \tag{5}$$

Substituting $s = j\omega_0$ gives

$$T(j\omega_0) = \frac{j\omega_0 g_{m2} k_1 L_1}{\omega_0^4 A_4 - \omega_0^2 A_2 + 1 - g_{m1} R_1 - j\omega_0\left(\omega_0^2 A_3 - A_1\right)}. \tag{6}$$

When oscillation occurs, the real part in the denominator of (6) must drop to zero and the oscillation frequency ω_0 can be calculated by

$$\omega_0^2 \approx \frac{1}{L_1(C_1 + C_2)} \cdot \frac{1 - g_{m1} R_1}{\left(1 + \frac{R_1^2}{L_1} \cdot \frac{C_1 C_2}{C_1 + C_2} - g_{m1} R_1 \cdot \frac{2C_2}{C_1 + C_2}\right)} \tag{7}$$

if k_1 is approximated to unity.

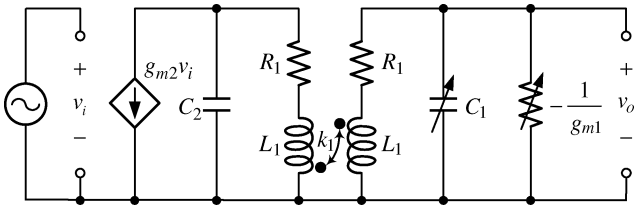

Fig. 3. Open-loop equivalent circuit from Fig. 2(b).

C. Extended Tuning

In (7), the oscillation frequency obviously depends on the inductances and capacitances of the tank, as well as the transconductance of g_{m1}. To arrive at a tuning technique, besides varying C_1, g_{m1} is also a variable that can be controlled by the varied bias currents. We can rewrite (7) as

$$\omega_0^2 = \omega_T^2(C_1) \cdot \alpha^2(C_1, g_{m1}) \tag{8}$$

where

$$\omega_T^2 = \frac{1}{L_1(C_1 + C_2)} \tag{9}$$

and

$$\alpha^2 = \frac{1 - g_{m1}R_1}{1 + \frac{R_1^2}{L_1} \cdot \frac{C_1C_2}{C_1+C_2} - g_{m1}R_1 \cdot \frac{2C_2}{C_1+C_2}}. \tag{10}$$

ω_T is the intrinsic resonance frequency with a lossless tank for $R_1 = 0$, and α is used to represent the frequency-extended factor. The above expressions prove to be a useful illustration in studying the behavior of ω_0 as a function of C_1 and g_{m1}. Differentiating (9) and (10) gives

$$\frac{\partial \omega_T^2}{\partial C_1} = -\frac{1}{L_1(C_1 + C_2)^2} \tag{11}$$

$$\frac{\partial \alpha^2}{\partial C_1} = -\frac{(1 - g_{m1}R_1) \cdot \frac{R_1C_2}{(C_1+C_2)^2} \cdot \left(2g_{m1} + \frac{R_1C_2}{L_1}\right)}{\left(1 + \frac{R_1^2}{L_1} \cdot \frac{C_1C_2}{C_1+C_2} - g_{m1}R_1 \cdot \frac{2C_2}{C_1+C_2}\right)^2} \tag{12}$$

and

$$\frac{\partial \alpha^2}{\partial g_{m1}} = -\frac{R_1 \cdot \left(1 + \frac{R_1^2}{L_1} \cdot \frac{C_1C_2}{C_1+C_2} - \frac{2C_2}{C_1+C_2}\right)}{\left(1 + \frac{R_1^2}{L_1} \cdot \frac{C_1C_2}{C_1+C_2} - g_{m1}R_1 \cdot \frac{2C_2}{C_1+C_2}\right)^2}. \tag{13}$$

Provided $C_1 > C_2$ and $g_{m1}R_1 < 1$ in typical design cases, the values in (11)–(13) are all negative. From (8), it is apparent that the values of oscillation frequency ω_0 and the factor α both decrease, not only as C_1 increases but also as g_{m1} does. Therefore, the tuning range can be extended tuning g_{m1} along with the varactor.

D. Validation of Proposed VCO

To validate the proposed VCO with extendable range introduced above, Spectre RF simulation was performed by using a 1.2-V 0.13-μm CMOS process. An accumulation MOS (A-MOS) is employed as a varactor. The physical layout parameters of the transformer are: the number of turns $N = 3$, the linewidth $W = 3\ \mu$m, and the inner radius $R = 15\ \mu$m. Table I shows the main dimensions and features for the active components of the VCO. The tuning characteristics in the circuit of Fig. 2(a) are plotted in Fig. 4, while using the control voltages V_c and V_{c1} as variables. It proves to be a useful illustration in studying the behaviors of the tuning range for the VCO with different tuned regimes. For example, the solid curve displays the VCO's characteristics varied with only V_c if $V_{c1} = 0$, i.e., g_{m1} disable, whereas the dotted curve implies that the VCO's characteristics are tuned by only V_{c1} if $V_c = 0$. The dashed curve illustrates the overall behavior in this study combining the varactor with the tuned g_{m1}, if connecting both control nodes together, i.e., $V_c = V_{c1}$. As a result, the tuning range can be extended.

TABLE I
DIMENSIONS OF THE ACTIVE COMPONENTS FOR THE VCO

Transistors ($W \times L$) in μm	
M_{1A}, M_{1B}	21×0.13
M_{2A}, M_{2B}	60×0.13
M_3	18×0.6
M_4	90×0.6
A-MOS	40×0.4

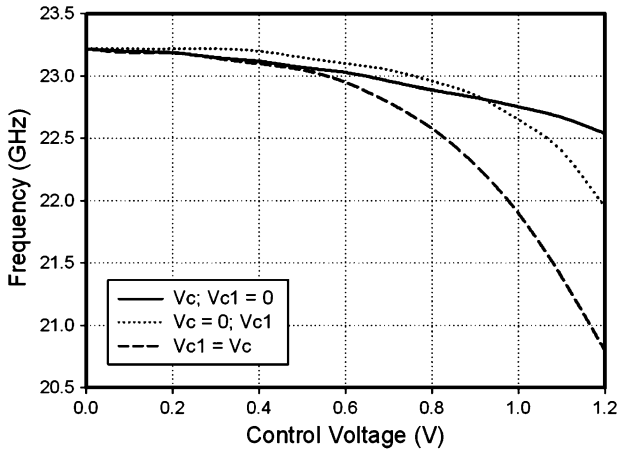

Fig. 4. Simulated tuning characteristics of the proposed VCO.

E. Linearization of Tuning Sensitivity

As known from the VCO design, the tuning curve is highly nonlinear because the control bias allows a high tuning range over a small voltage. However, many phase-locked loop (PLL) applications require VCOs that have tuning characteristics over most of their total tuning ranges. Improving the tuning control linearity of the tuned components for the VCOs can improve the consistency of loop dynamics in PLLs.

Using the separated components for tuning, a simplified way of achieving linear tuning range is through sensitivity ratio averaging. The idea is that the original tuned components with a high variance of sensitivity are divided into many parts, and each part is dynamically biased by the different controlled voltages. Generally, the overall sensitivity can be given by

$$\overline{K_{\rm vco}}(V_c) = k_1 \cdot K_{\rm vco}(V_1) + k_2 \cdot K_{\rm vco}(V_2) + \cdots + k_j \cdot K_{\rm vco}(V_j) \tag{14}$$

where $\overline{K_{\rm vco}}(V_c)$ denotes the average sensitivity, and $k_i \cdot K_{\rm vco}(V_i)$ is the sensitivity contributed by each tuned circuit and $k_i < 1$.

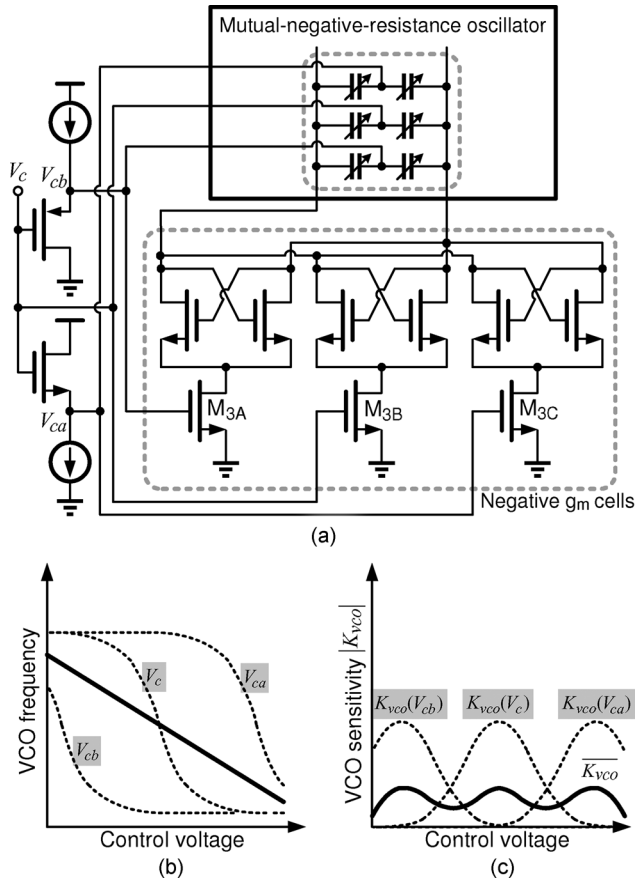

Fig. 5. Simplified linearization of the tuning sensitivity. (a) Schematic. (b) Transfer curves. (c) Tuning-frequency sensitivities with different control voltages.

An obvious solution for this is the insertion of a circuit block in front of the VCO, as shown in Fig. 5(a), to compensate the nonlinear VCO gain. The input control voltage V_c not only is applied, but also is shifted to the other voltages (V_{ca} and V_{cb}) to tune three-segment biases for the varactor cells and the transconductance cells of g_{m1}. The product of this transfer curve with the VCO tuning sensitivity should be as constant as possible to achieve a linear overall tuning, as illustrated via the solid line in Fig. 5(b). The dotted curves represent each transfer characteristic of the VCO [see Fig. 2(a)] whose biased transistor M_3 and varactor are tuned by V_{ca}, V_c, and V_{cb}, respectively, as shown in 5(a). The solid line of Fig. 5(c) illustrates the improved sensitivity of the VCO using the tuned component array with the averaging method.

III. Frequency Doubler

A. Basic Concepts

With the differential output phases provided at the fundamental frequency, the 40-GHz VCO can be realized by a push–push stage as the frequency doubler. Fig. 6(a) shows a general push–push frequency doubler [24], [25]. To maximize the conversion gain, the transistors are in a common-source configuration, while their output node is matched at the second harmonic frequency. The push–push operation shows a strong nonlinear effect due to the large output in the VCO. Thus, the

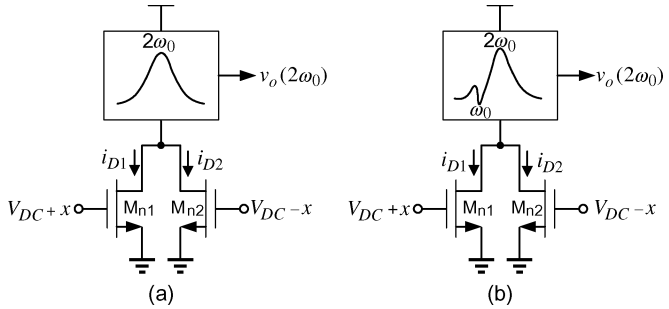

Fig. 6. Push-push frequency doublers using a: (a) general $2\omega_0$ resonator and (b) proposed $2\omega_0$ resonator with a notch at ω_0.

nonlinearity is modeled with polynomials empirically. The drain current of a MOSFET is modeled as

$$i_D = g_0 + g_1 x + g_2 x^2 + \cdots. \tag{15}$$

It follows that

$$i_{D1} + i_{D2} = 2(g_0 + g_2 x^2 + \cdots). \tag{16}$$

If $x = A cos \omega_0 t$, considering terms only up to second order, we then have

$$i_{D1} + i_{D2} \approx (2g_0 + g_2 A^2) + g_2 A^2 \cos 2\omega_0 t. \tag{17}$$

Thus, the output ac current is $i_o = g_2 A^2 \cos 2\omega_0 t$, which operates at twice the fundamental frequency.

However, the phase and amplitude errors due to device mismatch and layout asymmetry are inevitable in practical circuit implementation. The influence on the frequency doubler performance is evaluated by introducing a phase error ϕ and an amplitude error δ in the differential signals at the fundamental frequency. The ac current at the doubler output can be obtained as [24]

$$i_o \approx g_1 A \phi \cos(\omega_0 t + \theta_1) + g_2 A^2 \cos(2\omega_0 t + \theta_2) \tag{18}$$

where $\theta_1 = \tan^{-1}(A\phi/\delta)$ and $\theta_2 = \tan^{-1}(\delta\phi/A)$. Due to the phase and amplitude errors, the doubler output current consists of components at the fundamental and twice the fundamental frequencies. As indicated in (18), the FR decreases as the phase error increases. Thus, symmetric layout design is necessary to ensure sufficient suppression of the fundamental component for the frequency doubler. Furthermore, in order to suppress the fundamental component due to the phase and amplitude errors, a push–push frequency doubler with a notch at ω_0 is adopted, as shown in Fig. 6(b).

B. Proposed Doubler With a Fundamental Notch

The configuration of the proposed doubler is shown in Fig. 7, consisting of two common-source transistors in parallel, a symmetric transformer, and a matched inductor. The differential VCO signals are directly fed into the gates of the transistors in order to effectively generate the second harmonic components $v_o(2\omega_0)$. In Fig. 7, the symmetric spiral inductor acting as a transformer provides the effective inductance of $(1 + k_2)L_N$ in odd-mode operation, while the effective inductance is decreased

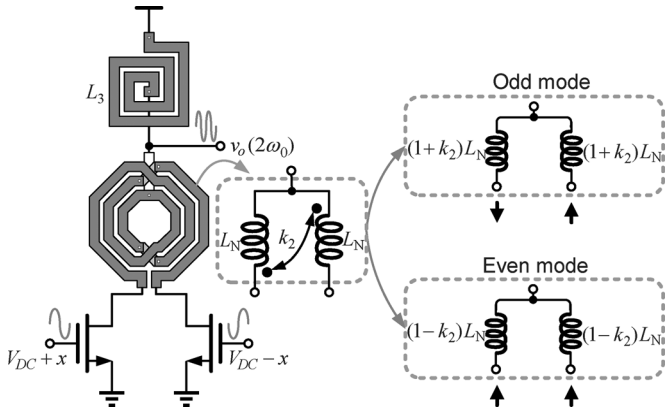

Fig. 7. Realization of proposed doubler.

to $(1-k_2)L_N$ in even-mode operation. On the other hand, considering the output feedthrough into the push–push stage, the doubler output can be viewed as a even-mode component that can be self-removed by the transformer through the coupling factor in the opposite direction.

The push-pull circuit has even-mode operation, which should be sustained, and odd-mode operation, which should be suppressed. The common nodes of the two identical half-circuit oscillators are virtually grounded at the odd mode and open at the even mode. Thus, the odd-mode operation can be suppressed by the notch circuit, which offers a transmission zero at ω_0 and degrades the gain of the transistor. Fig. 8(a) shows the simplified equivalent circuit of the push–push stage, where $2R_1$ is equal to r_{ds} for the transistors, the T-equivalent network of the coupled inductors is illustrated to model the symmetric transformer, and the effective capacitive components are included. In (17), we observe two components: the dc current and ac current at carrier frequency $2\omega_0$. The ac equivalent circuits of the push–push circuit can be developed in Fig. 8(b) to calculate the output voltage v_o, where i_i is used to represented the sum of currents produced by the MOSFETs in response to the gate voltages, and $L_2 = (1-k_2)L_N/2$ because the doubler output is contributed by the input even-mode components. Straightforward analysis yields the transfer function

$$\frac{v_o}{i_i} = -\frac{s\left(s^2 L_2 C_2 + s\frac{L_2}{R_2} + 1\right) L_3}{s^4 \cdot B_4 + s^3 \cdot B_3 + s^2 \cdot B_2 + s \cdot B_1 + 1} \tag{19}$$

where

$$B_4 = L_2 L_3 (C_1 C_2 + C_2 C_3 + C_1 C_3) \tag{20}$$

$$B_3 = L_2 L_3 \left(\frac{C_2 + C_3}{R_1} + \frac{C_1 + C_3}{R_2} + \frac{C_1 + C_2}{R_3}\right) \tag{21}$$

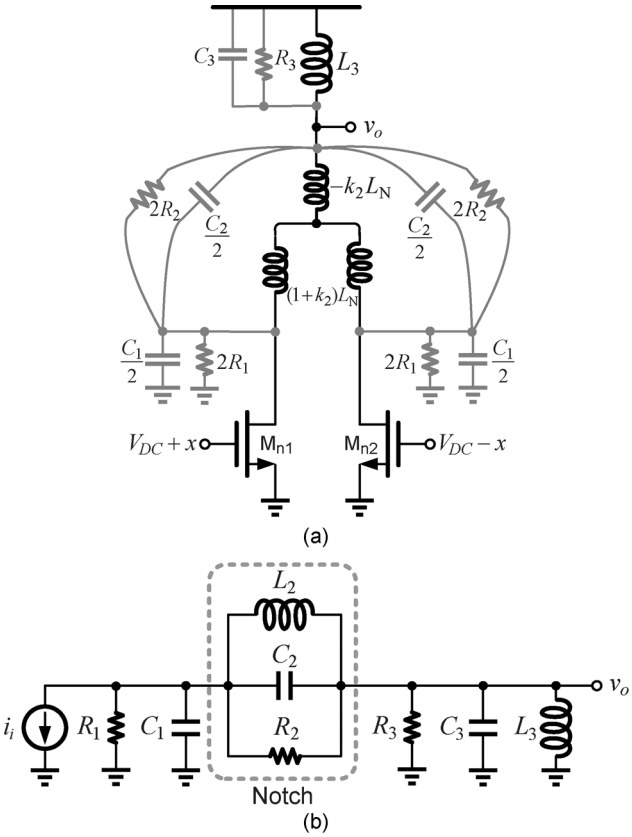

Fig. 8. (a) Equivalent circuit analysis. (b) Measuring the output voltage of the equivalent circuit for frequency-doubled signals.

$$B_2 = L_2 L_3 \left(\frac{1}{R_1 R_2} + \frac{1}{R_2 R_3} + \frac{1}{R_1 R_3}\right) + [L_2(C_1 + C_2) + L_3(C_1 + C_3)] \tag{22}$$

and

$$B_1 = \frac{L_2 + L_3}{R_1} + \frac{L_2}{R_2} + \frac{L_3}{R_3}. \tag{23}$$

Ideally, neglecting the resistance effect, the coefficients of odd-order polynomials in (19) are zero, and thereby (19) can be calculated as (24), shown at the bottom of the page.

If manipulated judiciously, (24) reveals several interesting points about the doubler. While the denominator appears rather complicated, it can yield intuitive expressions for two duplicate poles. In addition to poles, in (24) one transition zero is located at $\omega_z = 1/\sqrt{L_2 C_2}$, caused by the infinite impedance of the LC notch circuit.

C. Validation of Proposed Doubler

Using the extracted RF circuit models provided by the foundry, the transformer and matched inductor of the proposed

$$\frac{v_o}{i_i} = -\frac{s(s^2 L_2 C_2 + 1) L_3}{s^4 L_2 L_3 (C_1 C_2 + C_1 C_3 + C_2 C_3) + s^2 [L_2(C_1 + C_2) + L_3(C_1 + C_3)] + 1} \tag{24}$$

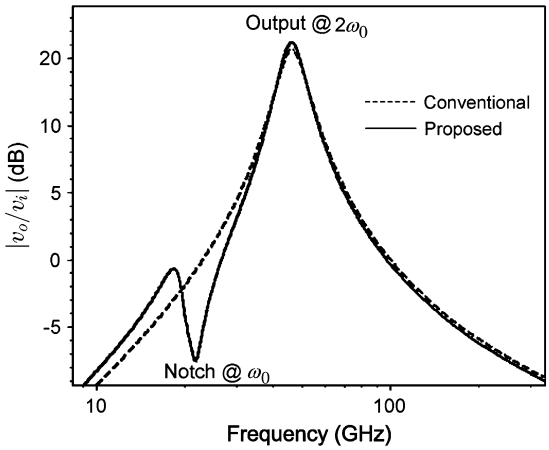

Fig. 9. Simulated transfer characteristic of the conventional and proposed doublers operating at the same desired output frequency.

doubler were carefully designed with the help of Spectre simulation. Both the transformer and matched inductor are made by planar spiral inductors. The resulting layout parameters of the transformer for the notch circuit are: the number of turns $N = 3$, the linewidth $W = 3$ μm, and the inner radius $R = 40$ μm, while those of the matched inductor are: $N = 2$, $W = 9$ μm, and $R = 15$ μm. For comparison, the inductor of the conventional circuit was redesigned with $N = 1$, $W = 9$ μm, and $R = 15$ μm for the same desired output frequency. The capacitance component parallel to the inductor can arise from the fringe field between adjacent turns. While it is desirable to use large fringing capacitance in the spiral inductor to explore the notch design option, the spiral winding wires through the topmost two metal levels is built and the adjacent turns are spaced by the minimum allowed by the technology. As a result, the self-oscillation frequency of the spiral inductor is mainly affected by the fringing capacitance instead of the substrate effect. Fig. 9 shows the simulated characteristics of the conventional and proposed circuits. The fundamental component in the proposed circuit is reduced, resulting from the added transition zero, compared with the conventional circuit. The peak of the spectrum in the proposed circuit is about 46.5 GHz, while the notch and the next peak are located at 21.7 and 18.6 GHz, respectively.

To demonstrate the performance of FR, the conventional push–push doubler and the proposed circuit were simulated with the $1 - V_{\mathrm{pk-pk}}$ amplitude of 21.66-GHz differential inputs. With mismatch between inputs, different phase errors and amplitude errors are given from 0° to 8° and from 0 to 80 mV, respectively. As indicated in (18), the FR decreases as the phase error increases or the amplitude error increases. Fig. 10(a) and (b) depicts the plots of the FR for the conventional circuit and the proposed circuit, respectively. For example, if the phase error is 8° and the amplitude error is 80 mV in the differential signals at the fundamental frequency, the simulated FRs of the conventional doubler and the proposed doubler are 20.86 and 27.38 dB, respectively. As a result of the notch at the fundamental frequency, the proposed doubler can provide better FR than the conventional circuit.

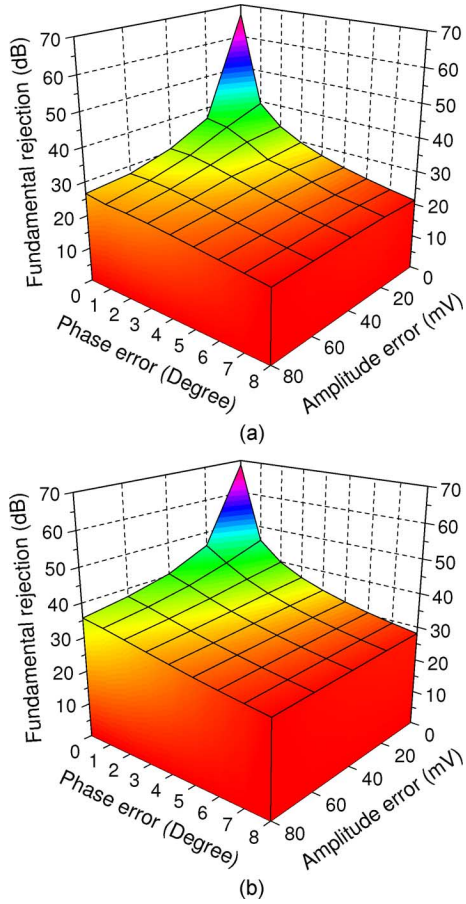

Fig. 10. Simulated FR for: (a) the conventional push–push doubler and (b) the proposed circuit.

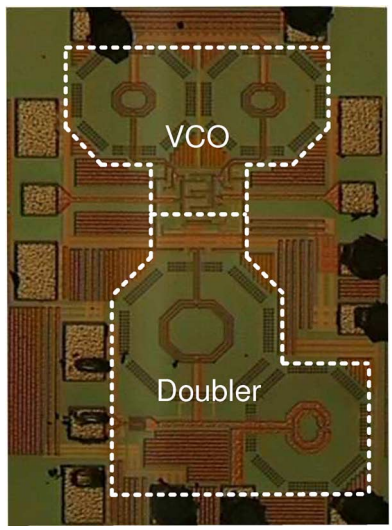

Fig. 11. Die photograph of the fabricated VCO and doubler.

IV. Chip Implementations and Measurement Results

The proposed circuits were fabricated in standard 0.13-μm CMOS technology with a nominal voltage of 1.2 V. Open-drain buffers were employed at each output to drive the 50-Ω input-impedance of testing instruments. Fig. 11 shows the microphotograph of the test chip with an area of 900×600 μm^2 including

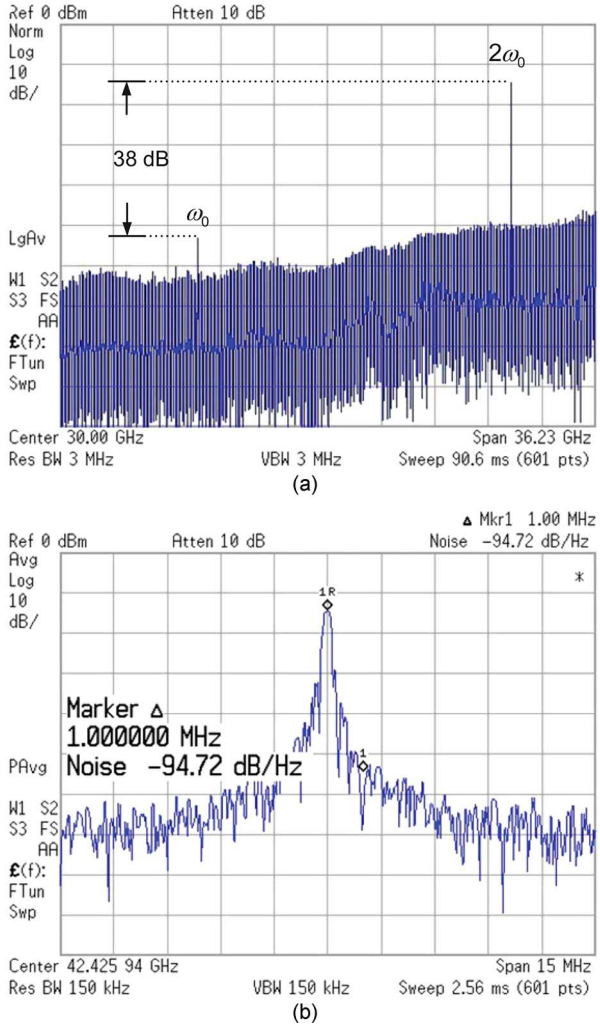

Fig. 12. Output spectra of the frequency doubler. (a) Whole spectrum. (b) Closed-in spectrum.

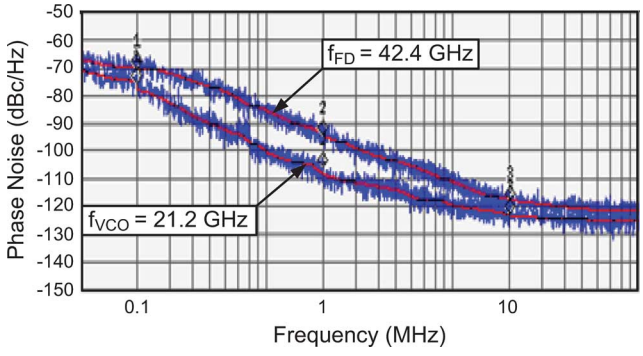

Fig. 13. Phase-noise plots of VCO at 21.2-GHz frequency and frequency doubler at 42.4-GHz frequency, respectively.

output buffers and input/output (I/O) pads. The VCO can provide the range of 19.8–22.6 GHz, while the doubler generates twice the frequency of the VCO. The measured middle-band spectrum of the buffered output for the doubler is shown in Fig. 12 at the 42.4-GHz carrier frequency. The whole spectrum and the closed-in spectrum are shown in Fig. 12(a) and (b), respectively, with the output power of −13.3 dBm. With

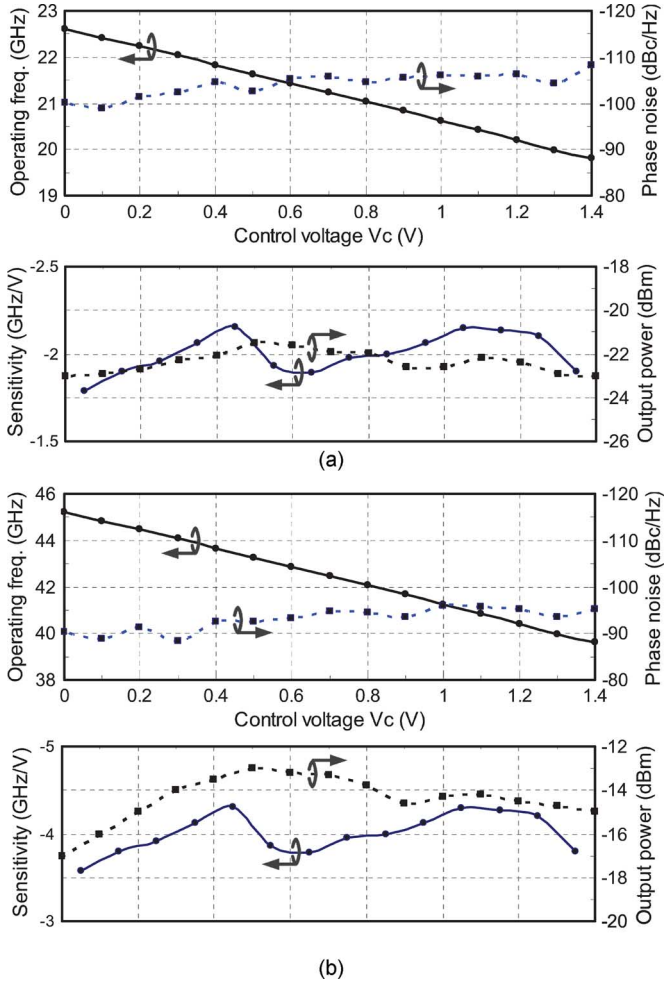

Fig. 14. Measured frequency tuning range, phase noise @ 1-MHz offset, output power, and calculated sensitivity ($K_{\rm vco}$) versus control voltage (V_C). (a) VCO. (b) Doubler output.

careful design of the frequency doubler utilizing a notch at the fundamental frequency, the 42.4-GHz output signal exhibits an FR of 38 dB. In Fig. 12(b), the measured phase noise of the doubler at 1-MHz offset is −94.72 dBc/Hz. Simultaneously, Fig. 13 shows a logarithmic plots of outputs for the VCO and frequency doubler. The VCO operates at 21.2 GHz with the phase noise of −75.6 dBc/Hz at 100-kHz offset, −105.7 dBc/Hz at 1-MHz offset, and −122.7 dBc/Hz at 10-MHz offset, while the frequency doubler provides 42.4 GHz with the phase noise of −68.9 dBc/Hz at 100-kHz offset, −94.6 dBc/Hz at 1-MHz offset, and −116.6 dBc/Hz at 10-MHz offset. The whole measured phase-noise data at 1-MHz offset are plotted in Fig. 14. The measured phase noise of the doubler (at 1-MHz offset) is approximately 11 dB worse than that of the VCO. Provided a conversion gain of 0 dB for the frequency doubler, the output phase noise is theoretically increased by 6 dB in an ideal case [11]. However, due to the losses of the matching networks and the noise sources from the transistors, the noise power density at a specific offset frequency is generally higher than the theoretical prediction in a practical design. Furthermore, the measured frequency tuning characteristic is also shown in Fig. 14, and the tuning range is 13.2% (19.8–22.6 GHz and 39.6–45.2 GHz,

TABLE II
COMPARISON OF PERFORMANCE WITH PRIOR VCOs

Refs	Technology [μm]	VDD [V]	Freq. [GHz]	$\Delta f_{\rm TUNE}$ [GHz]	Power [mW]	PN[dBc/Hz] @1MHz	FoM [dB]	$FoM_{\rm T}$ [dB]
[14]	0.13 CMOS	1.2	26.3	6	43	-92.6	-164.7	-171.8
[15]	0.13 CMOS	0.9	18.8	2.4	5.4	-110.5	-188.67	-193.1
[16]	0.18 CMOS	1	17	2.67[a]	5	-110	-187.6	-191.5
[17]	0.18 CMOS	1.8	19.9	0.51	32	-111	-181.9	-170.1
[18]	0.18 CMOS	2.4	21.3	0.6	9.6	-105.9	-182.8	-171.5
[19]	0.25 BiCMOS	4.5	19.4	5	13.5	-105[b]	-172.7	-180.6
[20]	0.25 BiCMOS	3.2	21.5	1.06	13.0	-113[b]	-178.4	-172.3
[21]	SiGe	1.9	25	1.25	4.5	-93.3	-174.7	-168.7
[22]	HBT	3	17	0.42	13.14	-110.4	-184.3	-171.8
[23]	HBT	4	21.6	0.4	28	-106	-178.2	-163.4
This work	0.13 CMOS	1.2	21.2	2.8	4.8	-105.7	-185.4	-187.8

[a]Including a switched-capacitor array to extend the tuning frequency
[b]Phase noise @2 MHz

TABLE III
COMPARISON OF PERFORMANCE WITH PRIOR MULTIBAND FREQUENCY SOURCES

Refs	Technology [μm]	VDD [V]	Freq. [GHz]	$\Delta f_{\rm TUNE}$ [GHz]	Power [mW]	PN[dBc/Hz] @1MHz	FoM [dB]	$FoM_{\rm T}$ [dB]	FR [dB]
[24]	0.18 CMOS	2	15	0.25	52	-112.2	-178.0	-162.5	
			30	0.5		-104.1	-176.5	-161.0	14.8
[25]	0.18 CMOS	1.8	11	1.19	11.8	-118.67	-188.0	-188.9	
			22	2.17	40.3	-111.67	-181.5	-181.8	12.2
			44	4.34	94.9	-102	-174.0	-174.4	N/A
[26]	HBT	5	18	0.18	40.0	-102.6	-171.7	-151.7	
			36	0.36	70.0	-96.6	-169.3	-149.3	8
This work	0.13 CMOS	1.2	21.2	2.8	4.8	-105.7	-185.4	-187.8	
			42.4	5.6	8	-94.6	-181.1	-183.5	38

respectively,) for the control voltage of 0 to 1.4 V. Since the measured tuning range of the VCO is 22.6–19.8 GHz with the control voltage 0–1.4 V, the ideal sensitivity for the VCO is -2 GHz/V. As shown in Fig. 14(a), the calculated sensitivity of the VCO with the linearized circuit is -1.97 GHz/V with a deviation of -180 MHz/V (9.1%).

A widely accepted figure of merit (FoM) for VCOs is given by [12]

$$\mathrm{FoM} = L(\Delta\omega) - 20\log\left(\frac{\omega_o}{\Delta\omega}\right) + 10\log\left(\frac{P_{\rm diss}}{1\ \rm mW}\right). \quad (25)$$

This FoM normalizes the phase noise at a given offset $(\Delta\omega)$, the center frequency (ω_o), and the power consumption $(P_{\rm diss})$ in milliwatts. Considering the tuning range, the FoM can be modified by [13]

$$\mathrm{FoM_T} = \mathrm{FoM} - 20\log\left(\frac{\mathrm{FTR}}{10}\right) \quad (26)$$

where FTR is the frequency tuning range in percent. The FoMs of the VCO alone and the doubler together with VCO are -185.4 and -181.1 dB, and their $\mathrm{FoM_T}$s are -187.8 and -183.5 dB, respectively. Tables II and III summarize the overall specifications in this study and the prior comparable. The results of this comparison with other VCOs working around 20 GHz are shown in Table II [14]–[23], and the comparable with dual/triple-band frequency sources are listed in Table III [24]–[26]. As shown in Table III, the presented doubler with the notch provides the performance on the FR much better than the other prior studies.

V. CONCLUSION

Implemented by a 0.13-μm CMOS technology, a 20/40-GHz dual-band circuit consisting of a VCO and a doubler is presented. Conventional varactor-tuned VCOs suffer from a tradeoff between the tuning range and the operating frequency for high-frequency designs. To satisfy both criteria, using the varactor- and transducer-tuned concepts for the LC-type VCOs is adopted in this study to enlarge the operating frequency range. The designed VCO is continuously tunable from 19.8 to 22.6 GHz with a tuning range of 13.2%. The VCO output phase noise at 21.2-GHz middle-band frequency is -105.7 dBc/Hz at 1-MHz offset. In addition, a linearized technique using sensitivity distribution with the separated tuning components can achieve a linear tuning feature through sensitivity ratio averaging, and the deviation of the sensitivity $K_{\rm vco}$ is below 10%.

Employing a notch at the fundamental frequency, the doubler generates twice the frequency of the VCO with better FR. The measured phase noise at 42.4-GHz middle-band frequency is -94.6 dBc/Hz at 1-MHz offset, while the FR can achieve 38 dB.

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REFERENCES

[1] T. Copani, B. Bakkaloglu, and S. Kiaei, "A BiCMOS voltage controlled oscillator and frequency doubler for K-band applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2008, pp. 537–540.

[2] T. Hiraoka, T. Tokumitsu, and M. Akaike, "A miniaturized broad-band MMIC frequency doubler," *IEEE Trans. Microw. Theory Tech.*, vol. 38, no. 12, pp. 1932–1937, Dec. 1990.

[3] T. Takenaka and H. Ogawa, "An ultra-wideband MMIC balanced frequency doubler using line-unified HEMTs," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 10, pp. 1935–1940, Oct. 1992.

[4] J.-J. Hung, T. M. Hancock, and G. M. Rebeiz, "A high-efficiency miniaturized SiGe Ku-band balanced frequency doubler," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2004, pp. 219–222.

[5] K. Y. Lin, J. Y. Huang, C.-K. Hsieh, and S.-C. Shin, "A broadband balanced distributed frequency doubler with a sharing collector line," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 2, pp. 110–112, Feb. 2009.

[6] A. Zolfaghari and B. Razavi, "A low-power 2.4-GHz transmitter/receiver CMOS IC," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 176–183, Feb. 2003.

[7] B. Razavi, "A millimeter-wave CMOS heterodyne receiver with on-chip LO and divider," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 477–485, Feb. 2008.

[8] A. Worapishet, "Extended phase noise performance in mutual negative resistance CMOS LC oscillator for low supply voltages," *IEICE Trans. Electron.*, vol. e89-c, no. 6, pp. 732–738, Jun. 2006.

[9] A. Worapishet, I. Roopkom, and P. Khumsat, "A top-biased mutual negative resistance LC oscillator technique," in *Proc. Asia–Pacific Microw. Conf.*, Dec. 2007, pp. 1–4.

[10] C.-H. Chang and C.-Y. Yang, "A 0.18-μm CMOS 16-GHz varactorless LC-VCO with 1.2-GHz tuning range," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2007, pp. 107–110.

[11] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, no. 2, pp. 329–330, Feb. 1966.

[12] P. Kinget, *Integrated GHz Voltage Controlled Oscillators*. New York: Kluwer, 1999.

[13] J. Kim, J. Plouchart, N. Zamdmer, M. Cherony, Y. Tan, M. Yoon, R. Trzcinski, M. Talbi, J. Safran, A. Ray, and L. Wagner, "A power-optimized widely-tunable 5-GHz monolithic VCO in a digital SOI CMOS technology on high resistivity substrate," in *Proc. Int. Low Power Elect. Design Symp.*, Aug. 2003, pp. 434–439.

[14] K. Kwok and J. R. Long, "A 23-to-29 GHz transconductor-tuned VCO MMIC in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2878–2886, Dec. 2007.

[15] S.-L. Jang, Y. J. Song, and C.-C. Liu, "A differential clapp-VCO in 0.13 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 6, pp. 404–406, Jun. 2009.

[16] A. W. L. Ng and H. C. Luong, "A 1-V 17-GHz 5-mW quadrature CMOS VCO based on transformer coupling," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1933–1941, Sep. 2007.

[17] H.-H. Hsieh and L.-H. Lu, "A low-phase-noise K-band CMOS VCO," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 10, pp. 552–554, Oct. 2006.

[18] C.-C. Li, T.-P. Wang, C.-C. Kuo, M.-C. Chuang, and H. Wang, "A 21 GHz complementary transformer coupled CMOS VCO," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 4, pp. 278–280, Apr. 2008.

[19] B. Jung and R. Harjani, "High-frequency *LC* VCO design using capacitive degeneration," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2359–2370, Dec. 2004.

[20] M. Bao, Y. Li, and H. Jacobsson, "A 21.5/43-GHz dual-frequency balanced Colpitts VCO in SiGe technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1352–1355, Aug. 2004.

[21] J.-H. C. Zhan, J. S. Duster, and K. T. Kornegay, "A 25-GHz emitter degenerated *LC* VCO," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2062–2064, Nov. 2004.

[22] H. Shin and J. Kim, "A 17-GHz push–push VCO based on output extraction from a capacitive common node in GaInP/GaAs HBT technology," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 11, pp. 3857–3863, Nov. 2006.

[23] D. Baek, J. Kim, and S. Hong, "A dual-band (13/22-GHz) VCO based on resonant mode switching," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 10, pp. 443–445, Oct. 2003.

[24] H.-H. Hsieh, Y.-C. Hsu, and L.-H. Lu, "A 15/30-GHz dual-band multiphase voltage-controlled oscillator in 0.18-μm CMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 3, pp. 474–483, Mar. 2007.

[25] S. Ko, J.-G. Kim, T. Song, E. Yoon, and S. Hong, "K- and Q-bands CMOS frequency sources with X-band quadrature VCO," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2789–2800, Sep. 2005.

[26] D. Baek, J. Kim, and S. Hong, "Low phase noise Ku band frequency multiplied and divided MMICs using InGaP/GaAs HBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2003, pp. 2193–2196.

[27] B. Razavi, *Design of Integrated Circuits for Optical Communications*. New York: McGraw-Hill, 2003, ch. 7.

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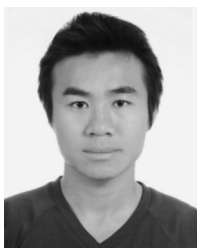

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