A 5-GHz Direct Digital Frequency Synthesizer Using an Analog-Sine-Mapping Technique in 0.35-μm SiGe BiCMOS

Ching-Yuan Yang, *Member, IEEE*, Jun-Hong Weng, *Student Member, IEEE*, and Hsuan-Yu Chang

***Abstract*—A direct digital frequency synthesizer (DDFS) using an analog-sine-mapping technique is presented in a 0.35-μm SiGe BiCMOS process. We intend to apply the translinear principle to develop a triangle-to-sine converter (TSC) that can achieve outputs with low harmonic content. The TSC is introduced for the DDFS to translate phase data to sine wave. Using this analog-interpolating technique, the DDFS, with 9 bits of phase resolution and 8 bits of amplitude resolution, can achieve operation at 5-GHz clock frequency and can further reduce power consumption and die area. The spurious-free dynamic range (SFDR) of the DDFS is better than 48 dBc at low synthesized frequencies, decreasing to 45.7 dBc worst case at the Nyquist synthesized frequency for output frequency band (0–2.5 GHz). The DDFS consumes 460 mW at a 3.3-V supply and achieves a high power efficiency figure of merit (FOM) of 10.87 GHz/W. The chip occupies 1.5×1.4 mm^2.**

***Index Terms*—BiCMOS integrated circuits, digital-to-analog converter, direct digital frequency synthesizer, translinear, triangle-to-sine converter.**

I. Introduction

HIGH synthesized frequencies can be achieved using phase-locked loops (PLLs). However, most PLLs inherently exhibit limited voltage-controlled oscillator tuning range, internal loop delay, and relatively narrowband control loop, thereby limiting the tuning range, tuning speed, and modulation capability. Nowadays, fast frequency switching is becoming critically important in modern wireless communication systems such as in spread-spectrum communication systems [1]. To achieve fast switching, direct digital frequency synthesizer (DDFS) has become as an alternative to PLL frequency synthesizer since it does not use a feedback loop and hence can provide fast frequency switching. In DDFS, all of the signal-processing operations that synthesize and tune the sine wave are performed digitally. For state of the art digital communication systems, DDFS can not only provide fine frequency resolution, allow fast settling time and fast frequency hopping performance and direct phase and frequency modulation in the digital domain, but also has the advantage of low phase noise (roughly equal to that of the input clock) over PLL approaches. While DDFS can provide the above features, it is considered a power-hungry circuit, especially for high clock frequencies, resulting in reduced usability for portable wireless communication applications. Thus, it requires entirely new ways of doing electronic circuit design to lower power dissipation.

Microwave DDFS circuits are mostly designed using indium phosphide (InP) HBT and silicon germanium (SiGe) HBT technologies. Although there are several DDFSs implemented in InP HBT technologies that have been reported to operate at clock frequencies from 9 to 30 GHz [2]–[4], the best power-efficiency figure-of-merit (FOM) of those DDFSs is 3.39 GHz/W [4]. On the other hand, SiGe BiCMOS DDFSs reported in [5]–[8] can work with multiple gigahertz clock speed, and the best power-efficiency FOM of those SiGe DDFSs arrives at 6.47 GHz/W [6]. All of the above DDFSs used a nonlinear digital-to-analog converter (DAC) as a sine-to-amplitude converter to achieve the goal of high speed and low power. However, the nonlinear DAC in DDFS requires a sine interpolation algorithm for amplitude transfer in the hybrid digital and analog domain, leading to a complex and cumbersome design and even lower output spur noise performance for DDFS.

An alternative approach is to combine a linear DAC and an analog-sine-mapping circuit in order to replace the role of the existing nonlinear DAC. Compared to the nonlinear DAC architecture for DDFS, design of the linear DAC is more simplified and can maintain reasonable spur noise performance with a given amplitude resolution. The DDFS architecture, using such an approach, may have the benefits of low power consumption and high speed operation by mitigating the DAC's complexity. In [9], a 9-bit DDFS uses the nonlinear function of a simple bipolar differential pair to perform an analog triangle-to-sine conversion. This particular DDFS was processed using 0.25-μm BiCMOS technology and achieved a power efficiency of 19.48 GHz/W at 6 GHz. However, while using the nonlinear transformation of the differential pair for DDFS, both the peak value and common-mode level of the input triangulated wave become very critical to the quality of the sinusoid output. As a result, due to these transfer errors on the differential pair, the SFDR presented in [9] was merely below 30 dBc for most output synthesis frequencies. Moreover, the nonlinear transfer function of the fabricated circuit deeply depends upon the variations on process, supply voltage and temperature (PVT), resulting in DAC linearity that is hard to control.

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The authors are with the Graduate Institute of Electrical Engineering and the Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan (e-mail: ycy@dragon.nchu.edu.tw).

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In this work, the analog-sine-mapping conversion circuit is designed through the translinear principle to provide low harmonic content for sine output. The proposed conversion circuit has better noise performance with differential current-mode operation. The output circuits immunity from power-supply-injected and substrate-injected noise sources. For comparison, the proposed DDFS, with 9 bits of phase resolution and 8 bits of amplitude resolution, can achieve a power-efficiency FOM of 10.87 GHz/W and produce the spurious-free dynamic range (SFDR) of larger than 45.7 dBc in wide output band. This DDFS employs 0.35-μm SiGe BiCMOS, which is less expensive, more compact, and consumes less power than aforementioned counterparts.

The paper is organized as follows. Existing DDFS architectures are summarized in Section II. A new DDFS is proposed that employs the development of a linear DAC and an analog sine-function circuit. The sine-function core, presented in Section III, is based on the translinear principle, which will be shown to provide low harmonic content. This core is composed of only 10 BJTs. The proposed architecture is shown to have significant area and power savings at high clock rates. Design consideration of the other building blocks will be discussed in Section IV. Section V presents measured results of the DDFS, as well as a comparison with recently published works. Finally, concluding remarks are drawn in Section VI.

II. DDFS Architectures

A. Conventional DDFS

In the past few years, improvements in DAC technology have made DDFS feasible at RF frequencies by synthesizing and tuning the sine wave via digital signal processing operations. The conversion from digital to analog takes place at the output of the synthesizer. The DDFS was originally developed by Tierney *et al.* [10]. A basic DDFS is depicted in Fig. 1 and is composed of a phase accumulator, a phase to amplitude ROM, and a linear DAC. The phase accumulator converts a frequency control word (F_{CW}) into phase data, and a look-up table (ROM) translates the data to amplitude data. Using the phase-to-amplitude sine mapping technique in the digital domain, the DDFS can output an analog signal through a linear DAC. As depicted in Fig. 1, a large ROM and high-resolution DAC are usually required to improve the spectral purity of a sine wave output. However, this kind of large ROM look-up table means higher power dissipation, lower reliability, slower access time, and larger die area. Although more efforts have been made to reduce the ROM size using different compression techniques [11], these techniques may not result in significant reduction in overall power dissipation nor in improvement in higher-frequency operation.

To reduce power dissipation, increase operating speed and further reduce the die area, an alternative DDFS with a nonlinear DAC using the amplitude-to-amplitude sine mapping methodology has been proposed to replace the ROM look-up table and the linear DAC, as depicted in Fig. 2 [12]–[14]. In this architecture, the function of the nonlinear DAC is to convert the digital phase information from the phase accumulator directly into an analog sine output voltage. This approach has been shown to

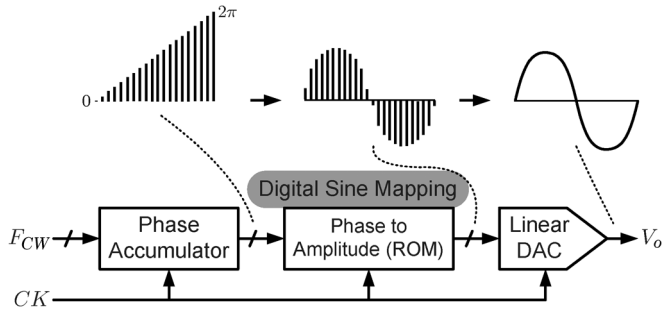

Fig. 1. Conventional ROM-based DDFS.

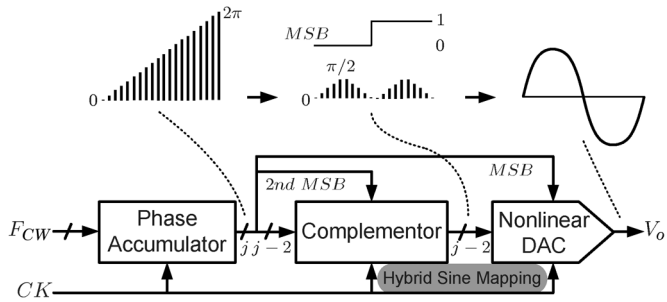

Fig. 2. General ROM-less DDFS using a nonlinear DAC.

provide considerable power and area savings compared to the conventional approach by virtue of the removal of the ROM. There are usually two ways to implement the nonlinear DAC. The first uses a resistive string, which consumes less power but occupies significant area due to the larger number of transistors and resistors used. The second implementation of the nonlinear DAC uses the current-mode technique, which can enhance speed at the expense of power consumption. However, to implement accurate sine function in a DAC, both techniques discussed call for complicated design for digital and analog circuits. Increasing phase resolution may increase power dissipation and area. For example, in [12], it was observed that the number of DAC cells doubles when the number of phase resolution bits increase by one. Moreover, the resolution performance for a nonlinear DAC will be degraded due to inherent nonlinear distortion, compared to the linear DAC counterpart with the same input bits.

B. DDFS Using Analog Sine Interpolation

For a DDFS with a j-bit frequency control word (F_{CW}) and k-bit phase resolution DAC, the output frequency of the synthesized sine waveform is $f_{out} = (F_{CW}/2^j)f_{CK}$. In a conventional DDFS, as shown in Fig. 1 and Fig. 2, the output of the phase accumulator is truncated into k bits to fit the inputs of the DAC. Usually the phase resolution of the DAC is much less than the resolution of the phase accumulator, then $j-k$ bits are discarded, which introduces F_{CW} dependent spurs. If the DAC is assumed to be ideal or close to ideal, the contribution of phase-truncation-related spurs is considered to be a dominant factor to the DDFS output total spurs and noise. For a nonlinear DAC (in Fig. 2), the situation is more complicated. To reduce the effect of the amplitude error, the ultrahigh-speed DDFS requires drastic speed and resolution improvements to the ROM

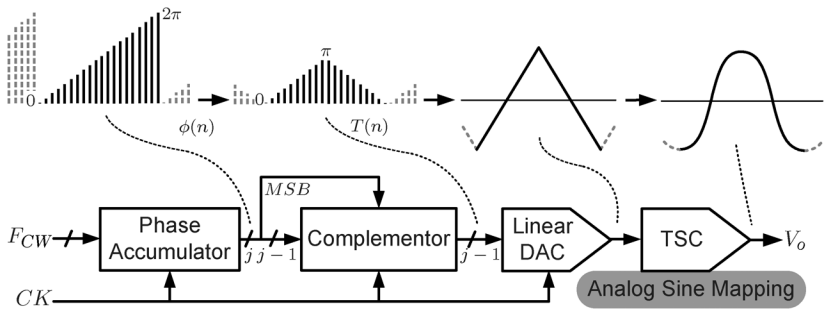

Fig. 3. ROM-less DDFS using a linear DAC and an analog sine-function interpolator to replace the nonlinear DAC.

and both DAC designs whether the linear or nonlinear DAC is used.

Unlike the sine mapping in digital or hybrid digital/analog domains, in Fig. 3, the combination of a linear DAC and a triangle-to-sine converter (TSC) employed in a DDFS is proposed to replace either the role of ROM/DAC in Fig. 1 or the role of nonlinear DAC in Fig. 2. In this architecture, the DDFS adopts an analog sine-mapping methodology, and thereby can easily overcome the limitations of the maximum operating power consumption because only the linear design for DAC is considered and it still retains the advantage of ROM-less DDFS in Fig. 2.

Using analog interpolative features on some analog circuits, a nonlinear transformation is utilized to convert the triangulated wave to a sine waveform in nonlinear-transfer-function-based signal generators [15]–[17]. An example using the BJT differential pair to achieve triangle-to-sine wave conversion is depicted in Fig. 4 [9], [18]. MOS transistors can also be used to realize the nonlinear function [19]. Because a triangulated wave can easily be generated by the digital phase-to-amplitude converter and DAC, such a nonlinear regime can provide a simple realization for a sinusoid signal generator.

III. Analog Translinear Sine-Function Circuit

The translinear principle, hinging on the precise exponential current-voltage characteristic of the bipolar transistors, has been useful in the design of analog integrated circuits [20]. The result of this investigation demonstrates that an approximated triangle-to-sine conversion capable of moderate precision can be designed by the translinear circuit without the need of more complex compensated circuits.

A. Mathematical Transfer Function

The base idea in sine-amplitude approximation is called *parabolic approximation*. The sine function can be approximated by a rational function [21]:

$$z = \frac{x(1-x^2)}{1+x^2}. \tag{1}$$

As can be seen, the zero slope of z is located at $x = \pm\alpha$, where $\alpha = \sqrt{\sqrt{5}-2}$. To achieve triangle-to-sine conversion, the parabolic-approximated function of (1), whose maximum and x-axis intersections are the same as that of the sine half-period, is generated for $-\pi/2 \le \phi \le \pi/2$. And the input triangulated waveform can be driven by $|x| \le \alpha$, as shown in Fig. 5. With

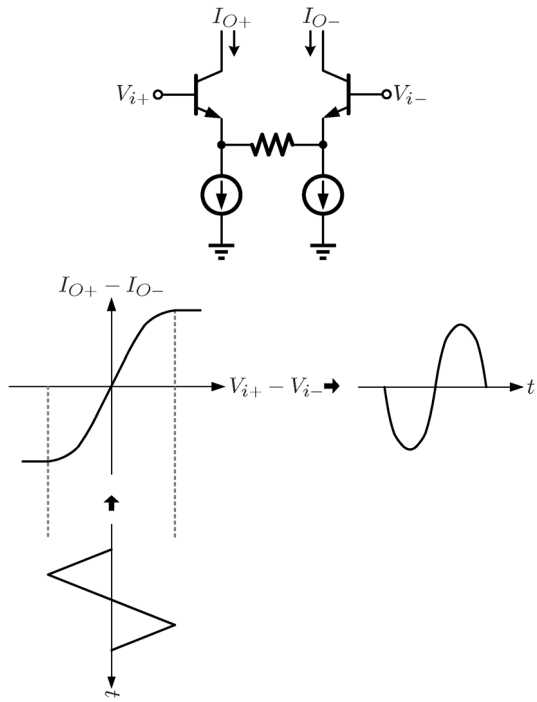

Fig. 4. Prior work using a BJT differential pair for triangle-to-sine signal conversion.

$z(\alpha) = 1/\beta$ for the peak value, we normalize the z function as a sine function, that is,

$$z_1(x_1) = \beta \cdot z(2\alpha \cdot x_1) \approx \sin(\pi x_1),\ |x_1| \le 0.5. \tag{2}$$

A complete period of an ideal sinusoid and the employed mathematical function of (2) are graphed in Fig. 6, which shows the calculated deviation from an ideal sine wave and the maximum difference in percent as 1.23%.

B. Translinear Sine-Function Converter

After defining the mathematical description of the translinear sine approximation, the most important point is how it will be electronically realized. The TSC is realized by the NPN BJT topology, as shown in Fig. 7. The circuit is connected with normalized common inputs and outputs in differential mode. A translinear loop exists between base-emitter junctions of transistors Q_1 to Q_6, that is,

$$V_{BE1} + V_{BE4} + V_{BE6} = V_{BE2} + V_{BE3} + V_{BE5}. \tag{3}$$

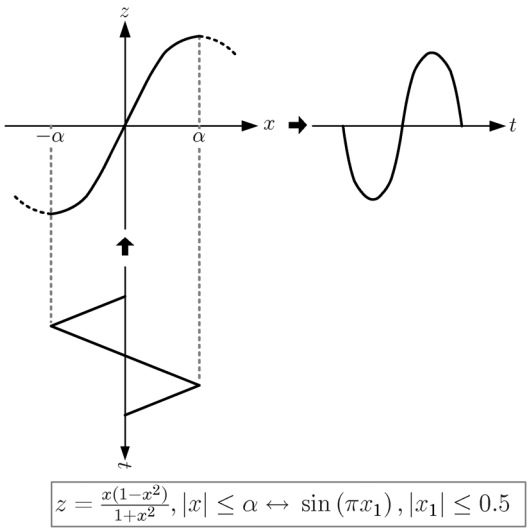

Fig. 5. Concept of translinear sine conversion.

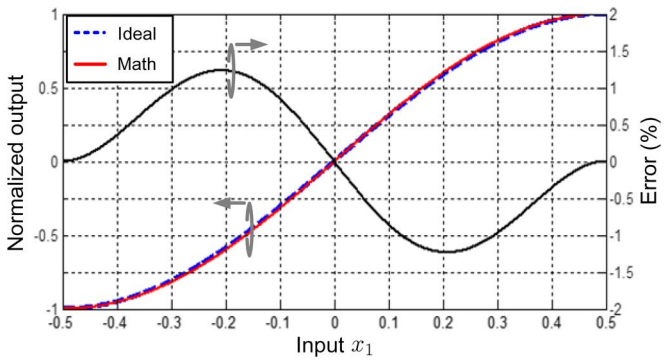

Fig. 6. General concept of the new initial guess for a half period of the ideal sinusoid and the mathematical transfer function of the translinear sine conversion, and their amplitude error.

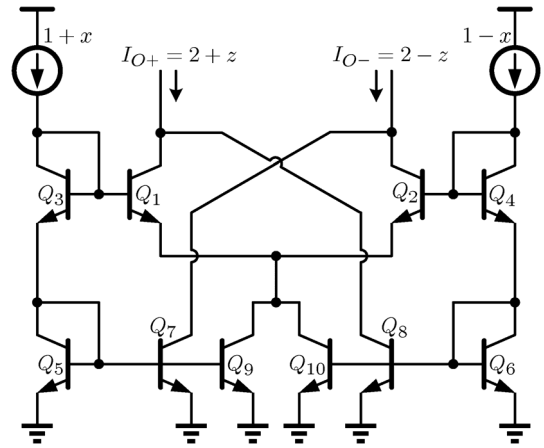

Fig. 7. Translinear sine converter.

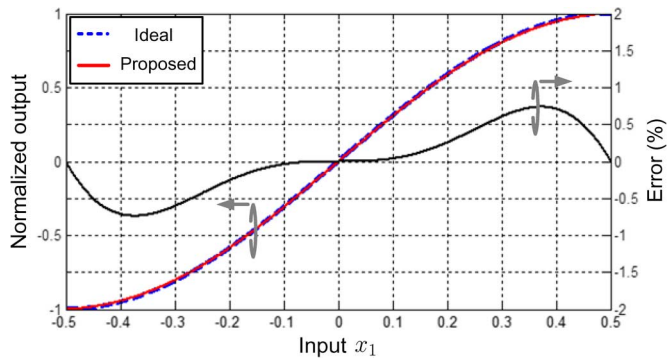

Fig. 8. Modified transfer curve of the proposed TSC in theoretical analysis and the amplitude error, compared with the ideal sinusoid.

Using the exponential current-voltage relationship in the bipolar transistors and neglecting the base current for simplicity, we have

$$I_{C1} \cdot I_{C4} \cdot I_{C6} = I_{C2} \cdot I_{C3} \cdot I_{C5} \tag{4}$$

where $I_{C3} = I_{C5} = 1+x$ and $I_{C4} = I_{C6} = 1-x$. In addition, since Q_9 and Q_{10} are connected as a push-push structure and mirrored by the input currents, the AC signals at their emitters cancel each other and then provide a constant current for the emitter-coupler pair of Q_1 and Q_2, that is,

$$I_{C1} + I_{C2} = 2. \tag{5}$$

Considering $I_{C7} = 1+x$ and $I_{C8} = 1-x$, the output currents can be calculated as $I_{O+} = 2+z$ and $I_{O-} = 2-z$, respectively. With differential operation, the effective output current can be represented by $i_o = I_{O+} - I_{O-} = 2z$, which is an approximated sine function as shown in (1).

C. Validation of Proposed Circuit

Since the input range of the TSC is dependent on the DAC output, the amplitude of its triangulated waveform is fixed for practical realization. For an intuitive understanding, we can normalize the amplitude of its triangulated waveform to 1, and then compute the specific common-mode level of input triangulated waveform for optimization. The common-mode level is defined by $1+\delta$, where δ represents a desired level-shift value and it is small in practice. Employing the foregoing development with the differential inputs of $(1+\delta)+x_1$ and $(1+\delta)-x_1$, in Fig. 7, we can now derive the modified sine-approximated transfer function:

$$z_2(x_1) = \frac{x_1\left[(1+\delta)^2 - x_1^2\right]}{(1+\delta)^2 + x_1^2} \propto \frac{\sin \pi x_1}{\pi}, \quad |x_1| \le 0.5 \tag{6}$$

δ is realized in the DAC through tuning the dc current with a ratio, which will be discussed in Section IV-C. Specifically, taking into account that $z_2(0.5) = 1/\pi$, we have $\delta = 0.5 \cdot \sqrt{(\pi+2)/(\pi-2)} - 1$. Computing the amplitude error, as depicted in Fig. 8, the maximum difference in percent is 0.74% only, which is much smaller than that shown in Fig. 6. It indicates that (6) can improve the TSC with better performance than (1) through finely tuning the input common-mode level. This is an important and useful result for us to design the DAC in the DDFS.

To validate the proposed triangle-to-sine converter, HSPICE simulation was performed by using a 3.3-V 0.35-μm BiCMOS process. The typical β value for the bipolar transistors is 160 at the emitter current of 30 μA. The circuit is carefully designed

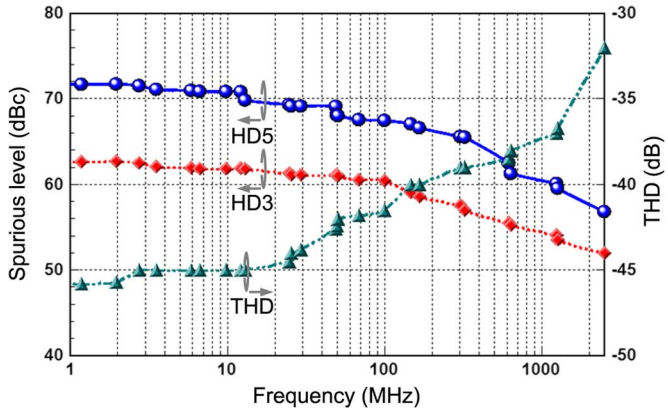

Fig. 9. Simulated performance of impurity harmonics (including the third and the fifth harmonics) and total harmonic distortion versus the input frequency.

with the help of HSPICE simulation. Odd harmonics mainly appeare in the spectrum due to the differential symmetrical structure. Fig. 9 shows the dependence of impurity harmonics, including the third and fifth harmonics, and the total harmonic distortion (THD), versus the operating frequencies. In 2.5-GHz bandwidth, the third and fifth harmonic effects are larger than 52 dBc and 56.8 dBc, respectively.

IV. DDFS Circuit Implementation

A. DDFS Architecture

Most conventional ROM-less DDFSs with a nonlinear DAC, as shown in Fig. 2, need to employ the most significant bit (MSB) and second MSB of the phase accumulator output to process one-quarter of the sine waveform data that are stored in the sine-weighted DAC. The MSB is used to provide the mirroring of the sine waveform at the π phase point. The second MSB is used to invert the second and fourth quadrants of the sine wave. In Fig. 3, only the MSB is required to generate the triangulated data by mirroring at the π phase point.

Referring to Fig. 3, the simplified block diagram of the ROM-less DDFS introduces a 9-bit accumulator, an 8-bit linear DAC and a TSC to directly generate the sine waveform. The DDFS output V_o is produced by the TSC from a triangulated waveform of DAC output. The TSC was described in Section III, which is used to perform triangle-to-sine conversion. The DAC output is a function of $T(n)$, which is triangulated data. The MSB output of the phase accumulator is used to invert the phase data of the sine waveform from π to 2π. The DDFS comprises a 9-bit pipeline accumulator. Since the output frequency cannot not exceed the Nyquist rate, an 8-bit F_{CW} is fed into a 9-bit accumulator with the MSB of the accumulator input tied to zero internally. Thus, the DDFS requires only 8-bit inputs and the output of accumulator provides a 9-bit phase word (j). In studies of the published microwave DDFSs, the nonlinear DACs at most have 8-bit amplitude resolution [2]–[6], [9]. The approach using a linear DAC and a TSC to replace the nonlinear DAC is attractive for microwave DDFS design because it can provide drastic speed, power and area improvements to the conventional ROM- or ROM-less-based DDFSs. To reduce the effect of the transfer amplitude error, introduced spurs in the DAC and TSC need to be taken into account during the design. As illustrated in Fig. 9,

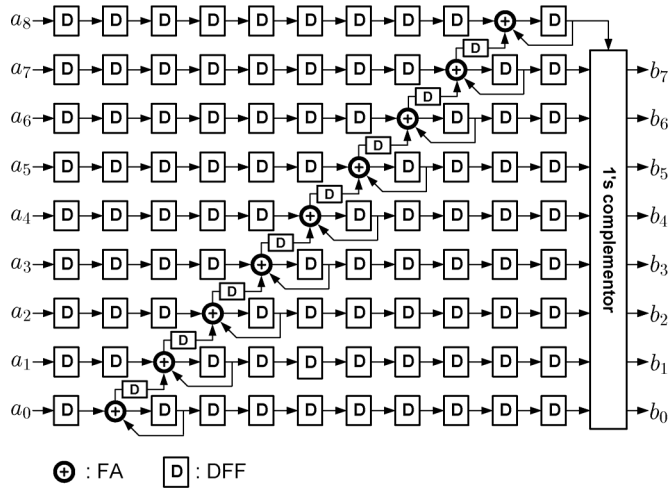

Fig. 10. Pipelined phase accumulator and 1's complementor.

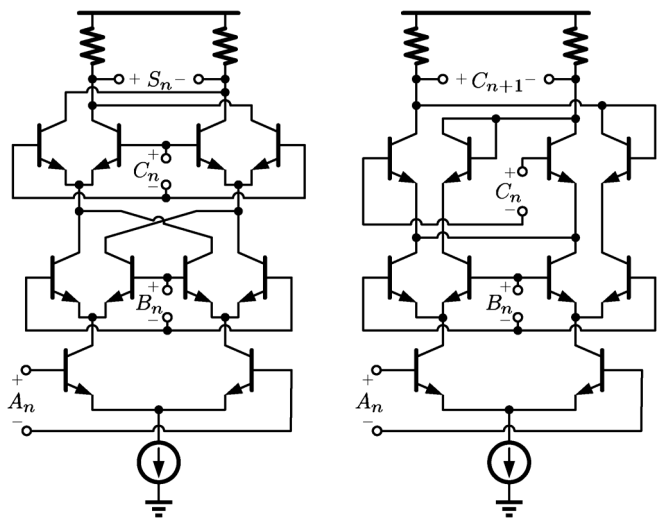

Fig. 11. CML full adder.

when a triangulated wave was provided, the third harmonic effect for the TSC output was more than 52 dBc and the THD was below -32 dB. In a word, to fit the DDFS requirement, the DAC is designed by 8 bits while the TSC should be verified to achieve more than 8-bit resolution.

B. Phase Accumulator

The accumulator integrates the input F_{CW} to derive phase information. In practice, the phase accumulator at multiple gigahertz clock rates cannot complete the 9-bit addition in a short single clock period because of the delay caused by the carry bits propagating through the adder. In order to achieve maximum operating speed, a pipelined approach for an accumulator is shown in Fig. 10. The speed can achieve up to the propagation delay of a 1-bit adder cell. Thus, the critical delay in the accumulator is determined by the propagation delay of the full adder (FA) and the D flip-flop (DFF). However, since the pipelined architecture cannot avoid using so many DFFs as shift registers, the DFF circuits demand substantial circuit area and power, and would impact the loading of the clock distribution network. Thus, the circuit design is focused on the reduction of power consumption in FA and DFF configurations.

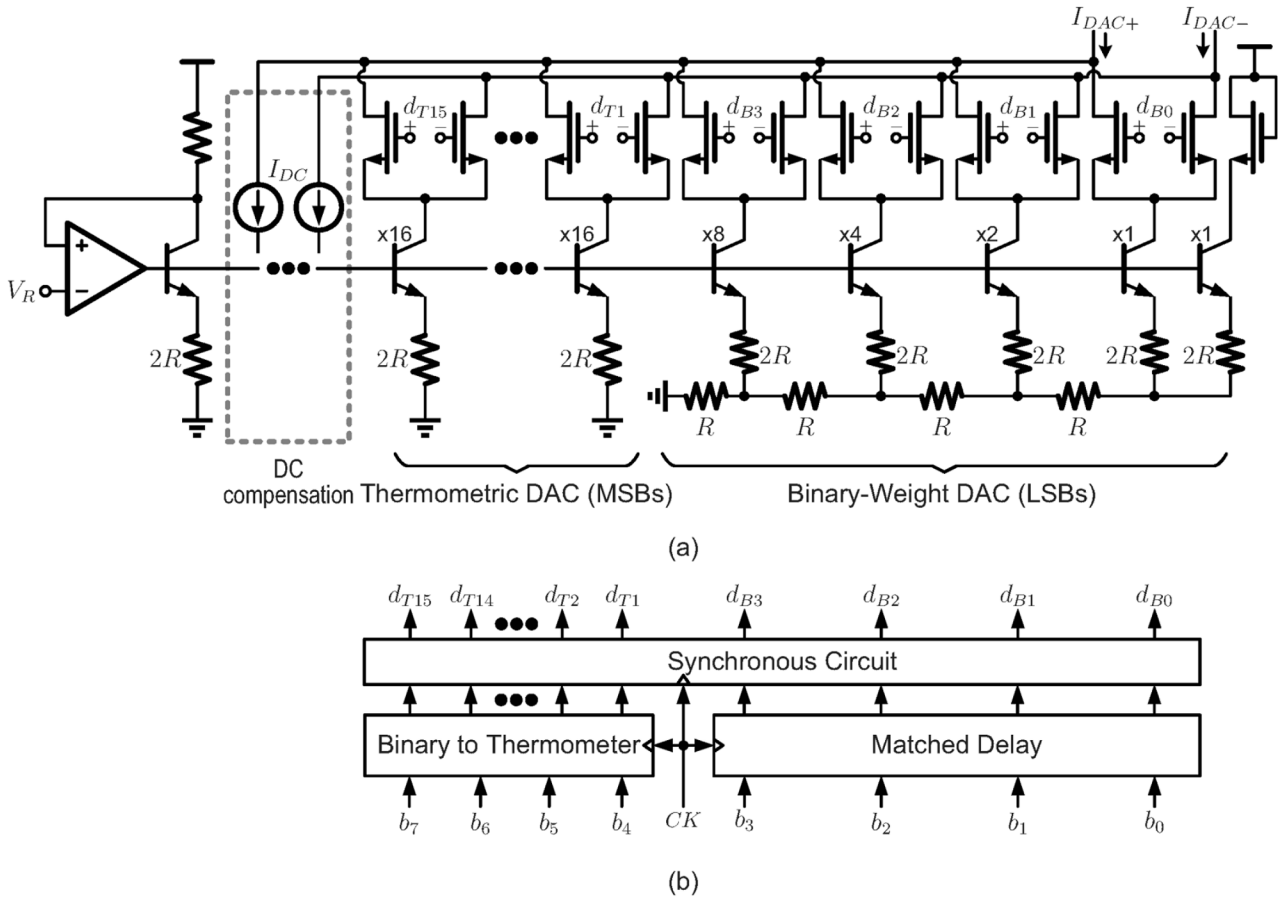

Fig. 12. (a) Segmented DAC schematic, and (b) decoded, matched and synchronous digital circuits.

The accumulator is built from 1-bit adder and register circuits. These circuits are based on a current-mode logic (CML) topology with differential output swings of 350 mV. The 1-bit adder is composed of sum and carry circuits, as shown in Fig. 11, where a single-stage telescopic cascode topology is introduced to minimize the propagation delay and power consumption [6].

C. DAC

The high-speed segmented DAC using current-steering operation is shown in Fig. 12(a). Fig. 12(b) depicts the digital decoder used to generate binary and thermometric codes for the DAC, and a synchronous circuit to avoid skewing effect on delay paths. The segmented architecture can obtain a high-resolution DAC by combining the operation of a 4-bit thermometric DAC implemented in a unary way for MSBs and a 4-bit R-2R ladder DAC for LSBs. The thermometric and binary-weighted currents are directly related to the reference current, almost independently of the supply voltage and V_{BE}. Also observe that the op amp supplies the base currents of all the BJTs. Besides, the matched delay circuit exhibiting in the LSBs can compensate the delay resulting from the thermometric decoder.

It is essential to note that the DAC provides differential current-mode output and that the TSC also works in differential current-mode operation, resulting in output that is immune to power-supply-injected and substrate-injected noise sources. In generating a low-distortion sine wave using wave-shaping circuits, one normally starts with a symmetrical triangulated wave signal of constant amplitude, and modifies the waveform by passing it through a nonlinear wave shaping circuit. The symmetry of the initial triangulated wave is generated by the DAC with respect to the phase accumulator. In addition, the common-mode value of the triangulated wave signal will affect the converted quality of the TSC, as depicted in Section III-C. As a result, in order to optimize the performance of the TSC, a compensated DC current [as shown in the dotted rectangle of Fig. 12(a)] is desired to inject into the DAC output. Since the designed DAC and TSC operate in current mode, the interference between DAC and TSC can be matched with the current ratio as the desired amplitude, independent of process and temperature variations.

V. Experiment Results

The proposed DDFS was fabricated in 0.35-μm SiGe BiCMOS technology. Fig. 13 shows the microphotograph of the test chip with an area of 1.5×1.4 mm^2 including the I/O pads. The test setup diagram is illustrated in Fig. 14. The entire DDFS test chip was measured powered by a 3.3-V supply voltage. The differential clock signals were generated by the Anritsu pulse-pattern generator. The DAC directly drove the TSC with an on-chip current mirror circuit. With current-mode operation in TSC, the internal resistors were connected as output loads and the emitter followers were used as the output buffers. External transformers were employed to convert the differential signals to single-end signals. The waveforms of

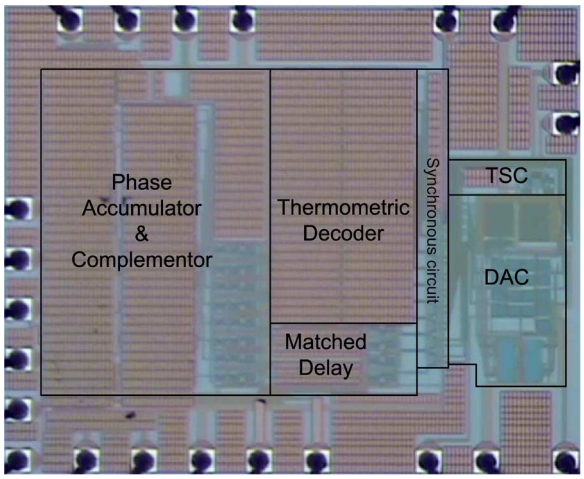

Fig. 13. Die micrograph of the DDFS.

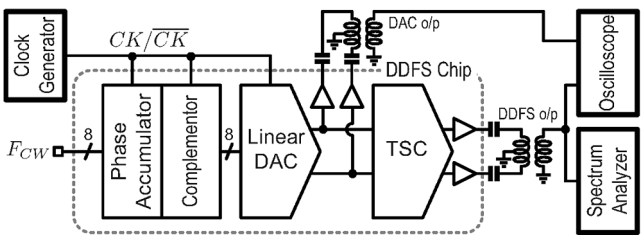

Fig. 14. Test setup.

the DAC and DDFS were obtained using a Tektronix digital phosphor oscilloscope, and the Agilent spectrum analyzer was used to measure the spectrum of DDFS output. At 5-GHz clock frequency, the DDFS was able to synthesize outputs in 256 steps of 9.765625 MHz per step. Fig. 15(a) and Fig. 15(b) illustrate the measured DDFS output spectrum for $F_{CW} = 1$ and the waveforms of DAC and DDFS output, respectively. At this frequency, the SFDR was measured to be 48.9 dBc, where the worst spurs are the third, fifth and seventh harmonics. The DDFS fulfills the requirement of an 8-bit static linearity in the DAC.

A DDFS's worst case close to carrier spurs at wideband typically occurs at Nyquist bandwidth. At Nyquist synthesized frequency ($F_{CW} = 255$), the measured SFDR is 45.7 dBc at a generated frequency of 2.49 GHz in Fig. 16, where the clock frequency is 5 GHz. Fig. 17 shows SFDR as a function of clock frequency for Nyquist synthesized operation. The frequency control word F_{CW} is set to a constant 255, and the clock is swept over a range of frequencies from 10 MHz to 6 GHz. The DDFS can operate to 5 GHz clock frequency, after which it no longer produces the better sine output due to bandwidth limitations for analog circuits and internal timing problems for digital circuits.

For a fixed clock frequency of 5 GHz, the sweep of SFDR versus the synthesized frequency is shown in Fig. 18. The SFDR is better than 48 dBc at low synthesized frequencies, decreasing to 45.7 dBc at Nyquist synthesized frequency. Fig. 19 shows the output waveforms of DAC and DDFS for frequency switching when F_{CW} is changed between 1 and 127. As can be seen, the DAC outputs a triangulated wave, then the TSC converts that output into a sine wave. At 5-GHz clock frequency, the whole power consumption of the DDFS is approximately 460 mW.

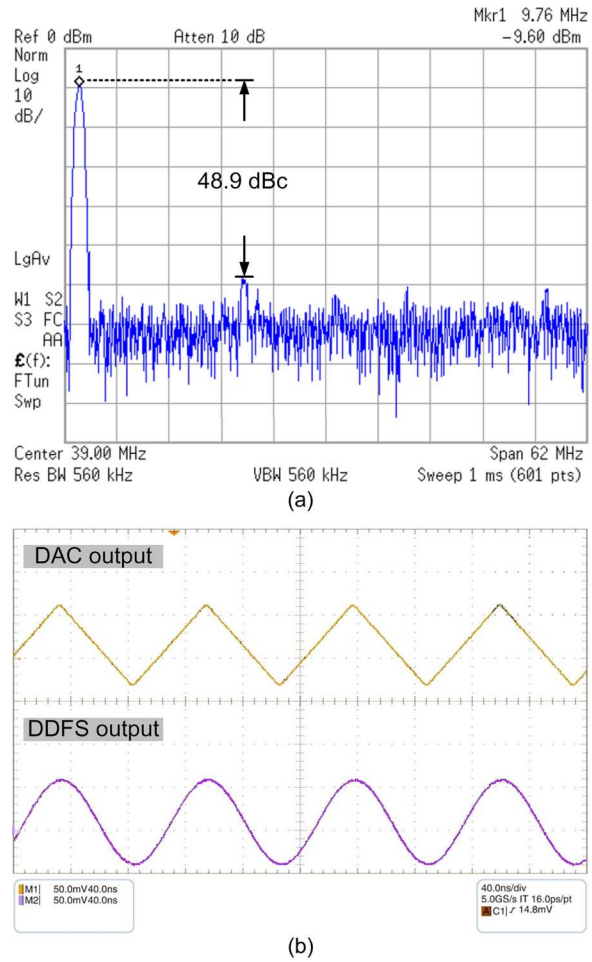

Fig. 15. (a) Measured DDFS output spectra for $F_{CW} = 1$, and (b) waveforms of DAC and DDFS outputs.

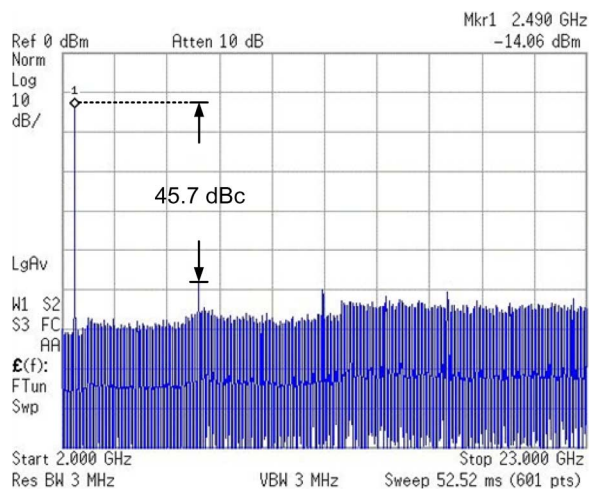

Fig. 16. Measured DDFS output spectra at Nyquist rate ($F_{CW} = 255$): the output frequency at 2.49 GHz with $f_{CK} = 5$ GHz.

Fig. 20 shows the power breakdown of the complete DDFS chip estimated by a HSPICE simulation for $V_{DD} = 3.3$ V. The DAC, TSC, and output buffers in analog design consume 8%, 5%, and 7% of the power in the DDFS, respectively. The digital accumulator and 1's complementor circuits (including the clock buffers) consume a lot of power, 54%, because many DFFs are used.

TABLE I
PERFORMANCE COMPARISON OF ULTRA HIGH-SPEED DDFS RFICS

Ref	Process [um]	Architecture	VDD [V]	Max. f_{ck} [GHz]	Bit Size ACC/DAC [Bit/Bit]	SFDR [dBc]	Die area [mm^2]	Power P_{DC}[W]	FOM $\frac{f_{ck}[GHz]}{P_{DC}[W]}$	FOM $\frac{f_{ck}[GHz]\cdot 2^{SFDR/6}}{P_{DC}[W]}$
2002 [2] JSSC	InP	Nonlinear DAC	NA	9.2	8/7	<30	40	15	0.61	< 19.62
2006 [3] MWCL	InP	Nonlinear DAC	NA	13	8/7	26.67	3.915	5.42	2.4	52.24
2006 [4] JSSC	InP	Nonlinear DAC	NA	32	8/5	21.65	3.915	9.45	3.39	41.3
2008 [5] TMTT	0.18 SiGe BiCMOS	Nonlinear DAC	3.3/4	6.8	9/8	30	9	2.5	2.72	87.04
2008 [9] MWCL	0.25 SiGe BiCMOS	Linear DAC + TSC*	2.8	6	9/8	17	1	0.308	19.48	138.84
2008 [6] JSSC	0.18 SiGe BiCMOS	Nonlinear DAC	3.3/4	12.3	9/8	20	9	1.9	6.47	65.25
2010 [7] JSSC	0.13 SiGe BiCMOS	Nonlinear DAC	3.3	8.6	11/10	33	14	4.8	1.79	81.08
2010 [8] JSSC	0.13 SiGe BiCMOS	Nonlinear DAC	3.3	5	24/10	45	11.1	4.7	1.06	192.57
This Work	0.35 SiGe BiCMOS	Linear DAC + TSC	3.3	5	9/8	45.7	2.1	0.46	10.87	2133.3

* A bipolar differential pair.

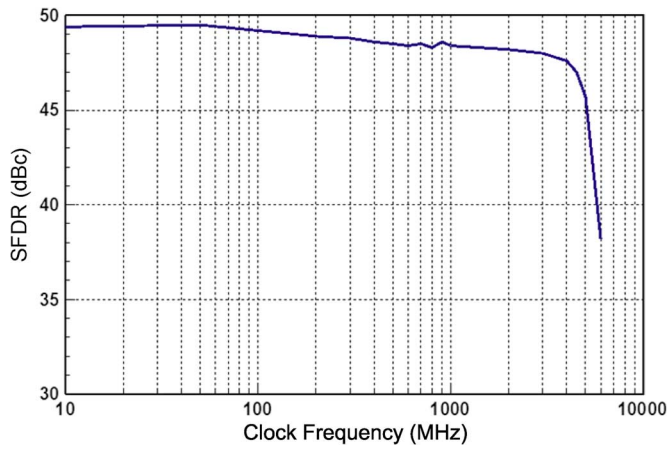

Fig. 17. Measured SFDR as a function of clock frequency, at Nyquist rate ($F_{CW} = 255$).

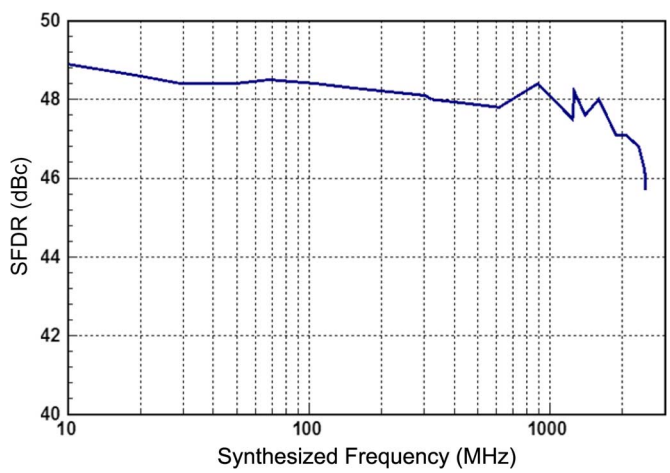

Fig. 18. Measured DDFS output SFDR versus synthesized frequency with $f_{CK} = 5$ GHz.

Table I lists several comparable DDFS's over the past years [2]–[9]. In order to normalize the power efficiency and SFDR

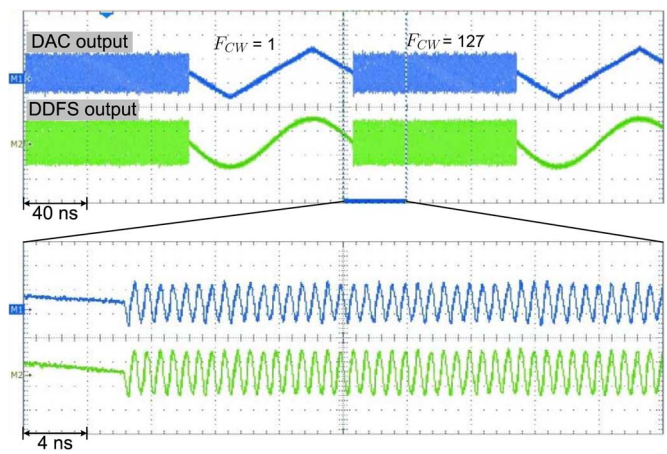

Fig. 19. Measured waveforms of DAC and DDFS for frequency switching when F_{CW} is changed between 1 and 127.

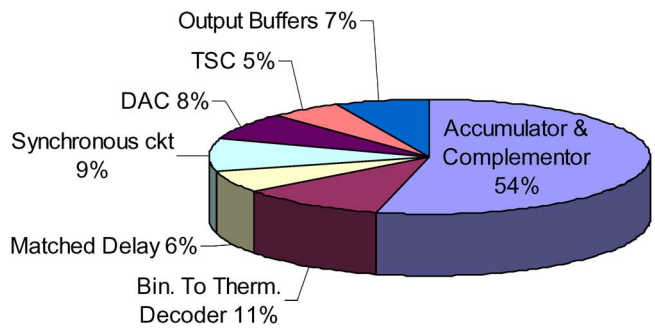

Fig. 20. DDFS power breakdown.

for a DDFS, the figure of merits (FOMs) defined in [7] are calculated, where SFDR(dB)/6 represents the ENOB obtained from the SFDR measurement. Compared to the prior DDFS MMICs, this DDFS employing the combination of a linear DAC and an analog sine converter significantly reduces power consumption and chip area, and achieves the better reported power efficiency FOM of 2133.3 GHz-$2^{\mathrm{SFDR}/6}$/W.

VI. Conclusion

In this paper, a new design technique for ROM-less DDFS using a linear DAC and an analog TSC is proposed. Compared to conventional ROM-based DDFSs, it requires significantly less power, just like the general ROM-less DDFSs using nonlinear DAC. The nonlinear DAC requires a sine interpolation algorithm for phase and amplitude transfer in hybrid digital and analog domain, leading to a complex and cumbersome design work. Instead of the nonlinear DAC, the combination of linear DAC and TSC can be designed without any truncation of digital control words for a given phase resolution and amplitude resolution requirement. Furthermore, the proposed technique will have significant advantages in terms of power dissipation and die area over conventional DDFSs for high-frequency operation.

To demonstrate the proposed technique, the DDFS was implemented with 0.35-μm BiCMOS technology. Using the inherent characteristics of BJTs, the TSC employs a translinear principle to fulfill sine function without complex compensated circuits. The DDFS covers a bandwidth from dc to 2.5 GHz in steps of 9.765625 MHz. The SFDR is measured to be over 48 dBc at low synthesized frequencies and to be 45.7 dBc at 2.5 GHz.

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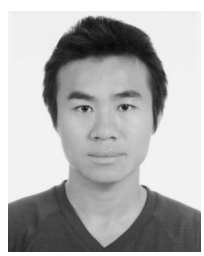
Ching-Yuan Yang (S'97–M'01) received the B.S. degree in electrical engineering from the Tatung Institute of Technology, Taipei, Taiwan, R.O.C., in 1990, and the M.S. and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1996 and 2000, respectively.

During 2000–2002, he was on the faculty of Huafan University, Taipei, Taiwan. Since 2002, he has been on the faculty of National Chung Hsing University, Taichung, Taiwan, where he is currently an Associate Professor with the Department of Electrical Engineering. His research interests are in the area of mixed-signal integrated circuits and systems for high-speed wireline and wireless communications.

Jun-Hong Weng (S'06) was born in Yunlin, Taiwan, R.O.C., in 1974. He received the B.S. and M.S. degrees in electrical engineering from Dayeh University, Changhua, Taiwan, in 1998 and 2005, respectively. He is currently working toward Ph.D. degree in electrical engineering at Nation Chung Hsing University, Taichung, Taiwan. His current research interests include in the area of integrated circuits and systems for high-speed interfaces, wireless communications and low-power ICs.



Hsuan-Yu Chang was born in Yunlin, Taiwan, R.O.C., in 1984. He received the B.S. and M.S. degrees in electrical engineering from National Chung Hsing University in 2006 and 2009, respectively. He is currently studying for the Ph.D. degree in the Department of Electronic Engineering, National Chung Hsing University, Taichung, Taiwan. His research interests include the analog-to-digital converter and the digital-to-analog converter.