A 0.5/0.8-V 9-GHz Frequency Synthesizer With Doubling Generation in 0.13-μm CMOS

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***Abstract*—To lower the supply voltage for high-frequency operation, a fully integrated frequency synthesizer, together with regenerative frequency-doubling and fractional phase-rotating techniques, is presented. The frequency-doubling circuit regenerates the tail signals at twice the frequency of the quadrature voltage-controlled oscillator (QVCO) to achieve larger output swing and higher operating frequency for the synthesizer. Additionally, a hybrid circuit utilizing a new folded regime for the first-stage divider and the phase-rotating circuit is developed in the prescaler. Under full-speed operation, the QVCO with the frequency doubler and the divider can work from a 0.5-V supply, whereas the synthesizer dissipates 12 mW. At 9.1-GHz carrier frequency, the measured phase noise is −104.5 dBc/Hz from 1-MHz offset.**

***Index Terms*—Frequency doubler, frequency synthesizer, low voltage, phase rotator, phase-locked loop (PLL), voltage-controlled oscillator (VCO).**

I. Introduction

DURING the last years, much effort has been put into the reduction of the supply voltage and the supply power of mixed analog–digital CMOS systems. This is primarily due to the increasing importance of battery-powered electronics and the continuing downscaling of device sizes. CMOS offers the big advantage of cheap processing and single-chip integration with digital building blocks. However, to obtain the low-voltage and high-frequency operation required in modern telecommunication systems at reasonable power consumption, new circuit techniques must be developed. Sometimes, single-battery or solar-battery operations will impose the additional constraint of operation at low voltage, i.e., as low as below 1 V, which will require entirely new ways of doing electronic circuit design [1]–[3].

In this paper, the voltage-controlled oscillator (VCO) with a frequency doubler and the high-frequency phase-rotating divider for fractional operation are proposed under a 0.5-V supply voltage [4]. Through the transformer's coupling, the frequency-doubling signal from the VCO can be regenerated to achieve higher operating frequency and larger output swing. In the phase-locked loop (PLL), the high-frequency fractional divider can be implemented by a high-speed phase rotating technique from the multiphase VCO. Moreover, a new folded topology consisting of the phase selector and the first-stage divider is developed to correctly divide the VCO's output in fraction at very low-voltage supply.

Manuscript received June 26, 2010; revised September 23, 2010; accepted November 8, 2010. Date of publication December 20, 2010; date of current version February 24, 2011. This work was supported by the National Science Council, Taiwan, under Contract NSC97-2221-E-005-090. This paper was recommended by Associate Editor A. Liscidini.

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Digital Object Identifier 10.1109/TCSII.2010.2092830

II. Frequency Synthesis Circuit Implementation

A. Architecture

Fig. 1 shows the proposed frequency synthesizer, which contains a phase-frequency detector, a charge pump, a low-pass loop filter, an LC-type quadrature VCO (QVCO), a frequency doubler, a divider, and a phase selector with an accumulator for dual-modulus division control. The block schematic of the QVCO consists of two identical differential LC-type VCOs. The combination of the direct and inverted connection forces the two VCOs to oscillate in quadrature. Following the QVCO, the frequency doubler provides twice the oscillation frequency through a transformer coupling. Referred as an injection-coupled structure with a resonator circuit, the frequency doubler regenerates the incident signal. Since the QVCO is based on narrow-band regimes, the narrow-band analog frequency doubler may be more suitable for this application to reduce power consumption and increase maximum operation frequency. Additionally, introducing the frequency-doubling regime in the synthesizer can mitigate the speed limitation of the QVCO and the prescaler. With a half-rate feature, the QVCO may provide a more reasonable tuning range and lower power consumption.

By utilizing the QVCO's output phases in sequence, the feedback divider can perform a fractional division ratio [5]. The divider using phase rotation can be proposed to realize the fine phase resolution and, thereby, low division ratios. In general integer-N PLLs, a fine resolution (or low $f_{\rm ref}$) leads to high division ratio N and narrow loop bandwidths to maintain stability $(< 0.1 f_{\rm ref})$ [8], resulting in longer settling times. Conversely, the fraction topology has the benefit of higher $f_{\rm ref}$ and more reasonable loop bandwidth, resulting in lower division ratios and shorter settling times. Depending on the logic value at the mode control, the division ratio is 64 $(MC = 0)$ and 64.25 $(MC = 1)$. In addition, the PLL is a third-order system with a second-order passive loop filter.

B. QVCO and Frequency-Doubling Regenerator

The original idea comes from a simple LC oscillator, which includes an LC tank, a pair of negative transconductance cells as a frequency doubler, and an output bandpass network (Z_L), as shown in Fig. 2 [7]. With the differential output phases provided at the fundamental frequency in the tank, in Fig. 2, the

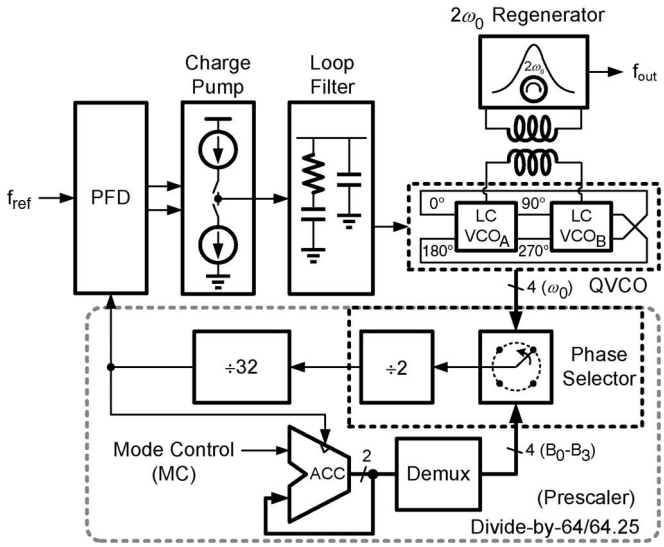

Fig. 1. Block diagram of the PLL-based frequency synthesizer with a dual-modulus divider.

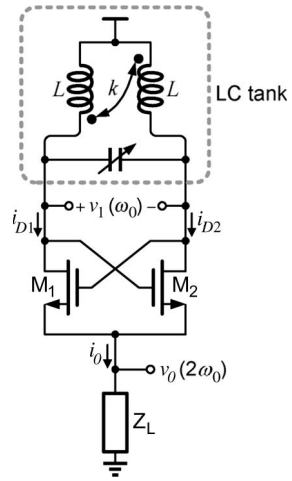

Fig. 2. LC-tank oscillator with a pair of negative transconductance cells to generate twice the oscillation frequency.

frequency doubler can be realized by the source-coupled stage. The circuit operation shows a strong nonlinear effect due to the large output in the VCO. Thus, the nonlinearity is modeled with polynomials empirically. Let us suppose that the VCO outputs are expressed as $v_{1+} = V_{DC} + x$ and $v_{1-} = V_{DC} - x$. The drain currents of the MOSFETs are modeled as

$$i_{D1} = g_0 + g_1 x + g_2 x^2 + \cdots \tag{1}$$

$$i_{D2} = g_0 - g_1 x + g_2 x^2 - \cdots. \tag{2}$$

It follows that

$$i_o = i_{D1} + i_{D2} = 2(g_0 + g_2 x^2 + \cdots). \tag{3}$$

If $x = A\cos\omega_0 t$, considering terms only up to second order, then we have

$$i_o \approx (2g_0 + g_2 A^2) + g_2 A^2 \cos 2\omega_0 t. \tag{4}$$

Thus, the output ac current is $g_2 A^2 \cos 2\omega_0 t$, which operates at twice the fundamental frequency. As a result, the LC oscillator generates an oscillation frequency of ω_0, whereas the source-couple pair cells generate the output at $2\omega_0$ at the source nodes. The second harmonic is generated by the nonlinearity of the source currents and the gate voltages in the source-coupled transistors.

The concept for quadrature coupling of LC oscillators can be found in [7], which uses the second harmonic of the outputs to couple the oscillators and to provide quadrature over a wide tuning range. Based on this concept, the proposed schematic of the QVCO, together with the frequency-doubling regenerator, is exploited in Fig. 3. The circuit implementation of the QVCO is constructed on two identical differential cross-coupled pMOS LC VCOs with the oscillation frequency of ω_0. Unlike the traditional ones, the tail devices are replaced by coupling inductors that are dimensioned such that they resonate with parasitic capacitance at a frequency of $2\omega_0$. The cross connection of pMOS $(M_5 - M_8)$ differential pairs in positive feedback generates a negative resistance to compensate the parasitic parallel resistance of the LC tank. Since the sources of transistors

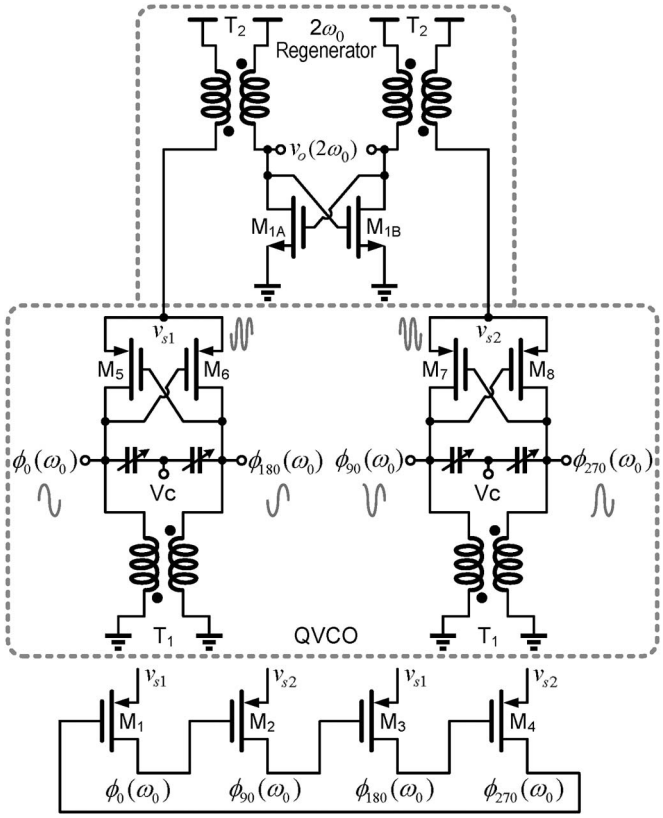

Fig. 3. QVCO and frequency-doubling regenerator.

vary at twice the oscillation frequency, two transformers (T_2's) with mutual inductors can be introduced between the VCOs and the regenerator to couple the high-frequency signals. The regenerator also has a resonator at $2\omega_0$.

In Fig. 3, the output stage regenerates the $2\omega_0$ signals by means of differential signals through transformers' coupling. Like a simple LC-VCO structure but not to oscillate, the regenerator provides twice the resonant frequency of the QVCO and negative resistance using cross connection of an nMOS differential pair $(M_{1A} - M_{1B})$ in positive feedback. Without the tail current source to release the voltage headroom requirement, both circuits can operate at a very low supply voltage.

In general quadrature LC oscillators based on a ring structure, the oscillation frequency can differ from the resonance frequency of the individual tanks. Like that shown in Fig. 3, the cross-coupling (M_1-M_4) circuits connected at the LC VCOs output are used to ensure sequence quadrature phase operation (ϕ_0, ϕ_{90}, ϕ_{180}, and ϕ_{270}) in QVCO. Since the tank is no longer operating at the frequency where the impedance is the highest and the phase characteristic is the steepest, the oscillation amplitude and phase stability are reduced, and the phase noise increases [6]. In the presented QVCO of Fig. 3, due to the superharmonic-coupled operation provided by the frequency doubler, the second-order harmonic is in antiphase, and then, the output waveforms of the two oscillators must be in quadrature [7]. The quadrature coupling does not require the oscillation frequency to deviate from the tank resonance. With the superharmonic coupled, small sizes of coupling transistors (M_1-M_4) can be required to output the phases in sequence. Consequently, the QVCO has more phase stability of each individual oscillator and less phase noise increased, as a result of the superharmonic-coupled characteristic.

The inputs of the regenerator, which are coupled by the transformers (T_2's), are the second-order harmonics of two separate differential oscillators. The transformers are dimensioned such that they resonate with the parasitic capacitance at $2\omega_0$. The QVCO produces an oscillation frequency of ω_0 at the quadrature nodes and harmonic of $2\omega_0$ with differential formats at the tail nodes. However, the phase and amplitude errors due to device mismatch and layout asymmetry are inevitable in practical circuit implementation. Due to the phase and amplitude errors in QVCO, the output current in (4) will consist of components at the fundamental (ω_0) and twice the fundamental $(2\omega_0)$ frequencies. With the bandpass filtering characteristic of the resonator at $2\omega_0$, the frequency doubler can effectively suppress the fundamental component.

Fig. 4(a) shows the simulated quadrature waveforms existing in the QVCO, along with the source voltages. It shows the gate–source and drain–source voltages of the switching transistors (M_5-M_8 in Fig. 3) periodically reach a small value. Transistors M_1-M_4 are small-size devices ($W/L = 0.26\ \mu$m$/0.13\ \mu$m) that are added to give directive to the quadrature phases. Without them, the oscillator would have no distinct preference for oscillation at either $+90^\circ$ or -90° phase difference. The currents flowing through transistors M_1-M_4 are negligible, compared with those in the transistors M_5-M_8 ($W/L = 48\ \mu$m$/0.13\ \mu$m). Replacing the traditional biased transistors with the transformers, the drain voltages of QVCO vary at twice the oscillation frequency across the supply voltage. As a result, without the required voltage drop on the current sources, the allowable oscillation swings can be enlarged under a very low supply voltage, even around the threshold voltage. Fig. 4(b) shows the tuned frequency of QVCO as the control voltage from 0 to 0.8 V at $V_{DD} = 0.5$ V.

C. Dual-Modulus Prescaler With a Phase-Rotating Topology

The dual-modulus prescaler is the other high-frequency building block of the PLL in Fig. 1. It consists of a phase selector, an integral divider, and a logic controller using an accumulator to determine the selected phase. If the input MC is high, the phase control block is now working, and the divide fractional ratio can be represented by $(64 + 1/4)$. Since

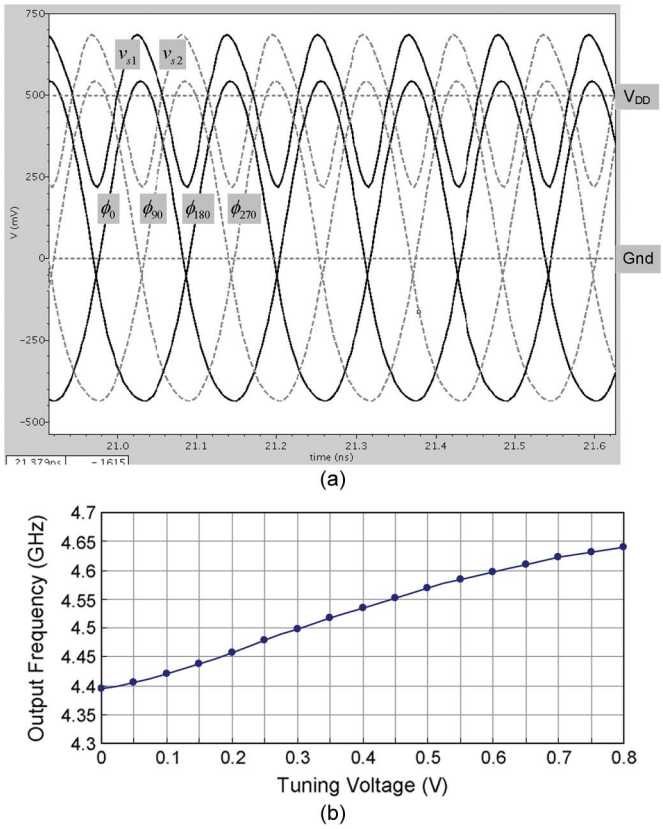

Fig. 4. (a) Waveforms and (b) tuning characteristic of the proposed QVCO.

a set of phase-shift waveforms (ϕ_0, ϕ_{90}, ϕ_{180}, and ϕ_{270}) is obtained by the QVCO, the amount of the phase shift is one fourth of the QVCO period. By manipulating the waveform set, an output waveform whose period is a fractional multiple of the QVCO period is generated. The phase rotator multiplexes the phase-shift waveforms with the following cyclic sequence: $\phi_0 \rightarrow \phi_{90} \rightarrow \phi_{180} \rightarrow \phi_{270} \rightarrow \phi_0 \cdots$, and thereby, the output period of the fractional divider becomes $(64 + 1/4)T_{QVCO}$. Moreover, the quantization noise coming from the dithered phase-rotating divider should be well filtered out by the low-pass transfer function of the PLL. However, only a first-order DS modulator can be employed in this architecture; in this case, the large in-band fractional spurs cannot be attenuated by the low-pass loop filter.

The frequency-limiting building in the prescaler architecture is, of course, the phase-select block and the first-stage divide-by-2 block, as shown in the dotted box of the prescaler in Fig. 1. In addition, it is necessary to facilitate the design for low-voltage operations through some circuit modification. As shown in Fig. 5(a), a folded topology using a pMOS-nMOS combination performs the D flip-flop function with two-D-latch configuration. The employed folded differential configuration can achieve stable operations and wide output swings, even at low supply voltages. The folded scheme enables to exploit the full-speed performance of the divide-by-2 circuit, together with the phase-select circuit, where the control bits B_0-B_3 is used to determine the phase-select path. The input stage is the phase-select block, whereas the output stage performs divide-by-2 operation. Their folded nodes are connected by the mutual inductor pair (L_3's), which are dimensioned such that they resonate with the parasitic capacitance at ω_0. The

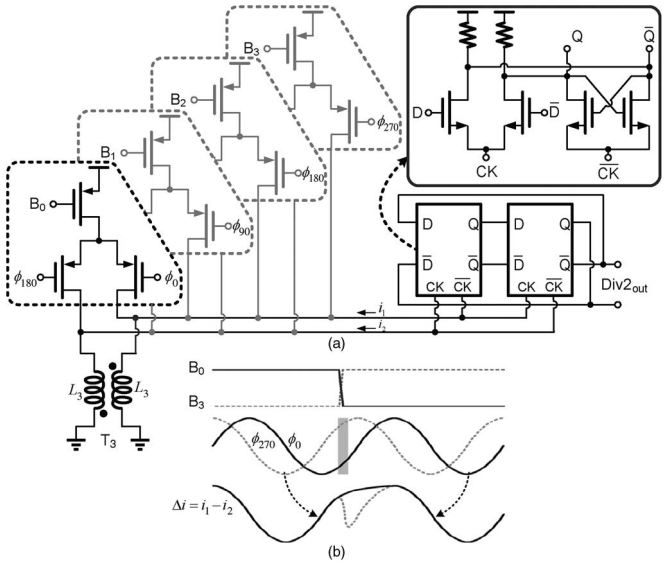

Fig. 5. (a) Folded scheme for the divide-by-2 circuit, together with phase switching. (b) Timing diagram for a critical control path.

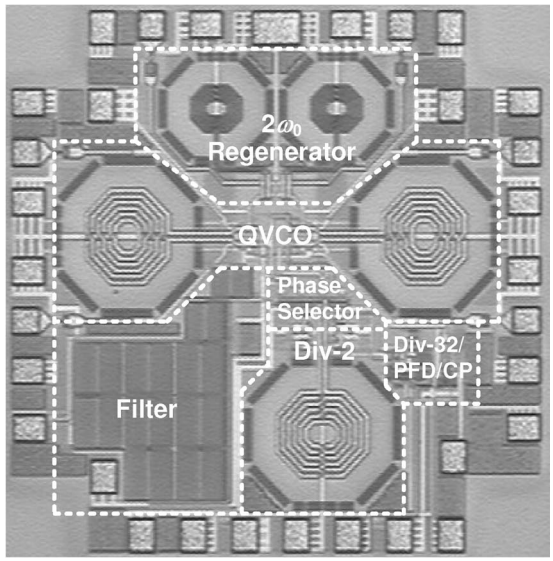

Fig. 6. Die photo of the fabricated chip.

equivalent circuit in the folded node can act as an LC-resonant buffer. Note that a possible drawback of the conventional phase-switching architecture in [9] is the spike that is situated in transition from phase to another. To understand the occurrence of the spike, the phase-select signals and the corresponding controls are shown in Fig. 5(b). The transition must occur smoothly under all circumstances since a spike in the transition would trigger the divide-by-2 circuit, leading to an erroneous division. With phase switching, therefore, smooth conversion must be guaranteed for all possible variations in processing or temperature and for all input frequencies. In the proposed circuit, the spike can be removed through the bandpass filtering in the folded node. With the narrow tuning in the QVCO, consequentially, it is suited for the first-stage divider and the phase-switching circuit to employ a transformer as the folded device for low-voltage and high-frequency operations.

III. Circuit Implementation and Measurement

To verify the performance of the frequency synthesizer as previously described, the proposed circuit was fabricated in standard 0.13-μm CMOS technology with a nominal voltage of 1.2 V. Fig. 6 shows the microphotograph of the test chip with an area of 1.1×1.1 mm^2, including the output buffers and I/O pads. Employing the symmetrical layout, the center-tapped spiral transformers with widths of 9- and 3-μm metal layers are employed for the required inductances in the QVCO and the frequency-doubling regenerator, respectively. Their coupled element sets $\{L, k\}$ of the symmetrical transformers are given to {1.41 nH, 0.633} and {0.56 nH, 0.556}, where k is the inductive coupling coefficient between the two coils. In addition, the accumulation-type devices are used as the varactors. The designed loop bandwidth of the PLL is about 500 kHz, which results in a total capacitance of 158 pF for the loop filter to be fully integrated on a chip. The power supplies are separated by the high- and middle-frequency circuits, respectively. The minimum operating supply voltage for QVCO, together with the frequency-doubling regenerator (Fig. 3) and the first-stage divider with phase selection [Fig. 5(a)], is 0.5 V, and the consumption current is 16 mA. However, the other circuits are supplied by 0.8 V due to the speed limitation of the divider and consume 5 mA. The divide-by-32 circuit consists of a chain of five toggle flip-flops (TFFs), and their critical operation voltage is limited by the first-stage TFF. Since its maximum operating frequency is the half of the oscillation frequency in the QVCO, the first-stage TFF must operate at around 2.25 GHz. If this TFF is improved, the minimum supply voltage for the divide-by-32 circuit will be decreased somewhat.

To evaluate the circuit performance, the frequency synthesizer was tested on an FR-4 personal computer board using the spectrum analyzer for measurement. For test purposes, each output signal was connected to an open-drain circuit with an externally match resistance of 50 Ω. A signal generator was used as the reference for all closed-loop measurements. The measured output range of the synthesizer was from 8.8 to 9.2 GHz if varying the input reference frequencies. For a given reference clock of 71 MHz, Fig. 7 shows the measured output spectrum of the frequency synthesizer when the divider provides divisions of 64 $(MC = 0)$ and 64.25 $(MC = 1)$, respectively. The buffered output in whole spectrum and its close-in spectrum are shown in Fig. 7(a) and (b), respectively, with the output power of -15 dBm. It can be seen that the second harmonic effect is -32 dBc and the fundamental rejection at the output of the frequency-doubling regenerator is 44 dB. The measured spurs are approximately 58 dB below the carrier. For the 9.12-GHz carrier, a logarithmic plot of the measured output phase noise with -104.54 dBc/Hz at 1-MHz offset is shown in Fig. 8. To determine the switching time of the frequency synthesizer, the dual-modulus frequency-division ratio is switched through the change of MC, and the control voltage of the QVCO is measured by an active probe. As shown in Fig. 9, the measurable switching times of the proposed synthesizer are 4.5 μs from $MC = 1$ to $MC = 0$ and 4.7 μs from $MC = 0$ to $MC = 1$. Table I shows the several comparable over the past years [1]–[3], which employ CMOS techniques to operate at below 1-V supply. Compared to the other prior works, the presented synthesizer with the doubling feature can operate at much more higher frequencies.

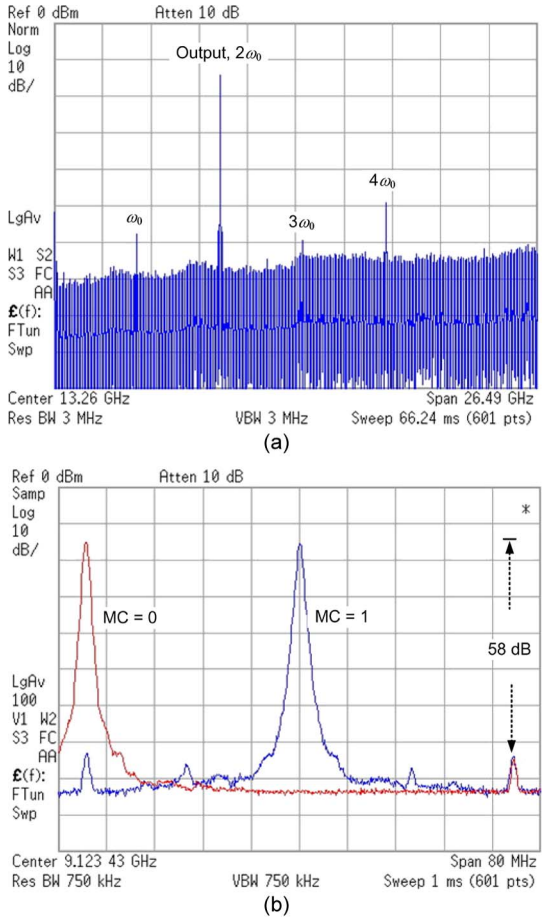

Fig. 7. Measured output spectrum of the frequency synthesizer. (a) Whole spectrum. (b) Close-in spectrum.

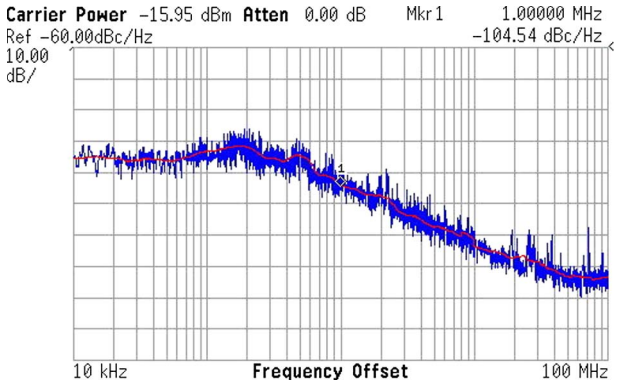

Fig. 8. Measured phase-noise plot at 9.12 GHz.

IV. Conclusion

A low-voltage, high-frequency and fully-integrated frequency synthesizer employing a frequency-doubling topology has been presented. The proposed topology can mitigate the speed limitation of the QVCO and the prescaler, leading into more design spaces for very low-voltage and high-frequency operation. The frequency doubler regenerates the frequency-doubling signals embedded in the tail device of the QVCO through the coupling transformers that can also work as a tail resonator of the QVCO to give the beneficial impact on noise filtering. Design of the dual-modulus prescaler is another critical implementation of the synthesizer resulting from its speed limitation. In the prescaler, a new folded topology for the phase selector and the divide-by-2 circuit is developed to operate at full speed from a very low supply voltage. With the bandpass filtering in the folded node, the phase transition can work smoothly under all circumstances as the phase switching occurs. Implemented in a standard 0.13-μm CMOS process, the fully integrated prototypeis presented. Employing the proposed techniques in the frequency doubler, the QVCO and the first-stage divider with phase switching enables to operate at 0.5-V supply voltage. The synthesizer provides the tuning range of 8.8–9.2 GHz and dissipates 12 mW. At 9.1-GHz carrier frequency, the measured phase noise is -104.5 dBc/Hz from 1-MHz offset.

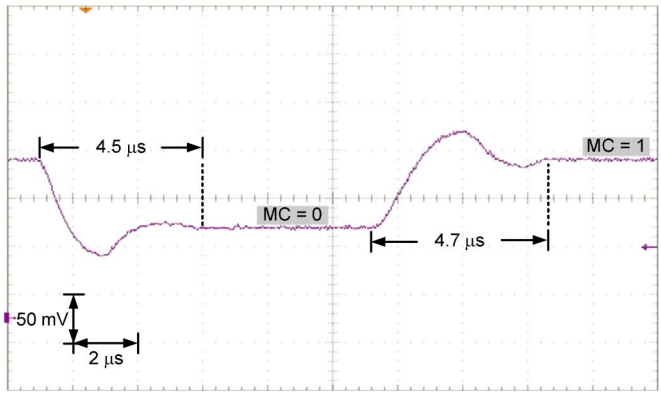

Fig. 9. Switching time measurement of the proposed synthesizer.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE PRIOR WORKS

Ref.	Tech. (μm)	Topology	Freq. (GHz)	V_{DD} (V)	P_{DC} (mW)	PN@1MHz (dBc/Hz)	Area (mm^2)
[1]	0.18	PLL	1.06–1.4	0.8	4.92	–121	1.65
[2]	0.18	PLL	1.9–2.1	0.5	4.5	–120	1.32*
[3]	0.09	PLL	2.4–2.6	0.5/0.65	5.5	–113	N/A
This	0.13	PLL&x2	8.8–9.2	0.5/0.8	12	–104.5	1.21

*off-chip loop filter

References

[1] W. Wang and H. C. Luong, "A 0.8-V 4.9-mW 1.2-GHz CMOS fractional-N frequency synthesizer for UHF RFID readers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 9, pp. 2505–2513, Oct. 2008.

[2] H.-H. Hsieh, C.-T. Lu, and L.-H. Lu, "A 0.5-V 1.9-GHz low-power phase-locked loop in 0.18- μm CMOS," in *Porc. Symp. VLSI Circuits*, Jun. 2007, pp. 164–165.

[3] S. Yu and P. Kinget, "A 0.65 V 2.5 GHz fractional-N frequency synthesizer in 90 nm CMOS," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 304–305.

[4] C.-H. Chang and C.-Y. Yang, "A low voltage, 9-GHz 0.13- μm CMOS frequency synthesizer with a fractional phase-rotating and frequency-doubling topology," in *Proc. Symp. VLSI Circuits*, Jun. 2009, pp. 192–193.

[5] B. A. Floyd, "Sub-integer frequency synthesis using phase-rotating frequency dividers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 7, pp. 1823–1833, Aug. 2008.

[6] P. Andreani, A. Bonfanti, L. Romano, and C. Samori, "Analysis and design of a 1.8-GHz CMOS *LC* quadrature VCO," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, Dec. 2002.

[7] S. L. J. Gierkink, S. Levantino, R. C. Frye, C. Samori, and V. Boccuzzi, "A low-phase-noise 5-GHz CMOS quadrature VCO using superharmonic coupling," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1148–1154, Jul. 2003.

[8] F. M. Gardner, "Charge-pump phase-lock loops," *IEEE Trans. Commun.*, vol. COM-28, no. 11, pp. 1849–1858, Nov. 1980.

[9] J. Craninckx and M. Steyaert, "A 1.75-GHz/3-V dual-modulus divide-by-128/129 prescaler in 0.7- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 890–897, Jul. 1996.