A Quadrature CMOS VCO Using a Distributed MIM Poly-Phase Network

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***Abstract*—In this letter, a 0.18 μm CMOS quadrature voltage-controlled oscillator (QVCO) using a simple distributed metal-insulator-metal (MIM) poly-phase network is presented. The MIM network is used to replace the conventional coupling transistors and to lower the power consumption and phase noise. The QVCO has a tuning range from 5.29 to 5.67 GHz and the power consumption is about 5.2 mW at a 0.6 V supply. At 1-MHz offset from a 5.48-GHz carrier, the measured phase noise is −118.58 dBc/Hz.**

***Index Terms*—Distributed poly-phase, low voltage, metal-insulator-metal (MIM), phase noise, quadrature voltage-controlled oscillation (VCO).**

I. Introduction

MANY modern wired/wireless transceiver architectures employ quadrature voltage-controlled oscillators (QVCOs) to generate in-phase and quadrature (I/Q) signals for modulation and demodulation. A popular QVCO combines two identical differential LC VCOs, with the coupling transistors placed in parallel with the switching transistors, and was known to have a poor phase-noise behavior. Without coupling transistors, recently, one method using transformer coupling between the two constituent VCOs in the QVCO was proposed in [1] and [2], but using the passive-transformer coupling may significantly suffer from a large chip area because of the integrated coupled devices. Besides, based on the same distributed principle, other VCOs using integrated strip-lines to generate I/Q output have been published in [3] and [4]. However, quadrature realization of distributed oscillators requires the use of four transmission lines, leading to a complex and cumbersome layout.

In this letter, a QVCO based on a distributed metal-insulator-metal (MIM) poly-phase network is proposed. In the circuit, several features exist to improve the prior QVCOs. First, compared to the transformers or distributed strip line used, the distributed MIM network can save more chip area. Next, replacing the coupling transistors with the distributed MIM network, it has the advantages of low phase noise and low power performance because the coupling transistors tend to generate additional device noise and consume more power. In addition, the QVCO can achieve 0.6 V operation because of only one transistor's voltage headroom.

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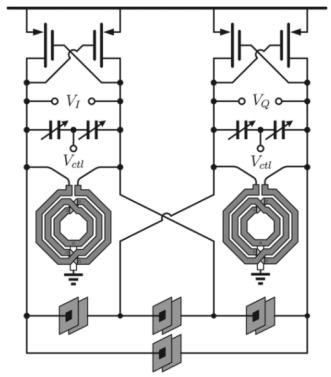


Fig. 1. Proposed QVCO with a distributed MIM network.

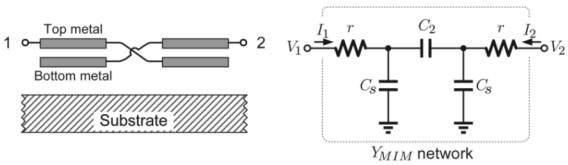


Fig. 2. Structure and equivalent circuit of a MIM device.

II. Circuit Design

Fig. 1 depicts the proposed QVCO topology, including two identical LC VCOs with a distributed MIM array in a closed loop. Each MIM device is depicted in Fig. 2, which is symmetrically constructed by top and bottom metals. Thus, the MIM device can be modeled by a two-port network with the matrix

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{1}$$

where

$$y_{11} = y_{22} = \frac{s^2(2C_2 + C_s)C_s r + s(C_2 + C_s)}{s^2(2C_2 + C_s)C_s r^2 + 2s(C_2 + C_s)r + 1}$$

and

$$y_{12} = y_{21} = -\frac{sC_2}{s^2(2C_2 + C_s)C_s r^2 + 2s(C_2 + C_s)r + 1}.$$

The MIM model includes the effective capacitance C_2 between top and bottom metals, the parasitic capacitance C_s between bottom metal and substrate, and the resistance r due to the MIM intrinsic loss.

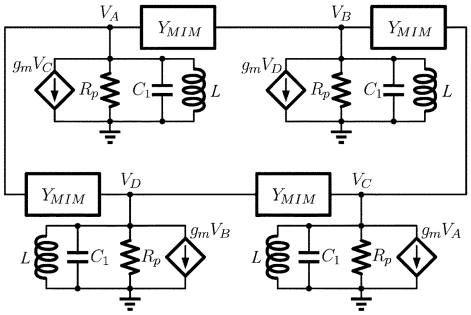


Fig. 3. Equivalent circuit of the QVCO.

The MIM array plays a role of phase-shift network, and forces the generated output phases to be in quadrature if oscillation occurs. The resonator is composed of a ring structure with the distributed MIM capacitors and the constituent LC tanks at IQ nodes, and the cross-connection MOS pairs in positive feedback generate negative resistances to compensate the loss of the LC tank. Such an oscillator combines the advantages of both, the LC tank and the ring topology. With the distributed MIM devices, therefore, the resonator has the LC characteristics from capacitive coupling, like in conventional LC tank to store energy, but it is also a distributed medium to generate four quadrature phases. Fig. 3 shows the equivalent circuit, where g_m is transconductance of the transistor, and L, R_p and C_1 are the inductance, the equivalent parallel resistance for loss and the total capacitances, including the varactor's capacitance and the parasitic capacitances of the transistors and the inductor, respectively. By node theory, we can obtain the following matrix:

$$\begin{bmatrix} \Gamma & y_{12} & g_m & y_{12} \\ y_{12} & \Gamma & y_{12} & g_m \\ g_m & y_{12} & \Gamma & y_{12} \\ y_{12} & g_m & y_{12} & \Gamma \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \\ V_D \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{2}$$

where $\Gamma = 2y_{11} + sC_1 + 1/sL + 1/R_p$. Since the desired QVCO outputs are nonzero, from above equation, we have: $V_A = -V_C$, $V_B = -V_D$, and $\Gamma - g_m = 0$. Substituting $s = j\omega_0$ and $rC_s \approx 0$ for simplicity in typical design cases, the oscillation frequency can be calculated by

$$\omega_0^2 \approx \frac{-\alpha + \sqrt{\alpha^2 + 16LC_1C_2^2r^2}}{8LC_1C_2^2r^2} \tag{3}$$

where $\alpha = L(C_1 + 2C_2 + 2C_s) - 4C_2^2r^2$. In addition, the required condition for a sustain oscillation is obtained by

$$g_m > \frac{1}{R_p} + \frac{4\omega_0^2C_2^2r}{1 + 4\omega_0^2C_2^2r^2}. \tag{4}$$

If r is small, (3) can be approximated as

$$\omega_0^2 \approx \frac{1}{L(C_1+2C_2+2C_s)}\left(1 + \frac{4C_2^2r^2}{L(C_1+2C_2+2C_s)}\right). \tag{5}$$

Thus, the distributed network with the parasitic components can contribute to determine the oscillation frequency.

Symmetric layout design in the distributed network is necessary to ensure the phase error between I and Q signals. Each distributed device was constructed by four MIM cells with the dimensions of 5 μm $\times$ 5 μm as the unit cell. Layout for the MIM device is common-centroid to keep matched characteristic as possible, as depicted in the right of Fig. 4. However, the

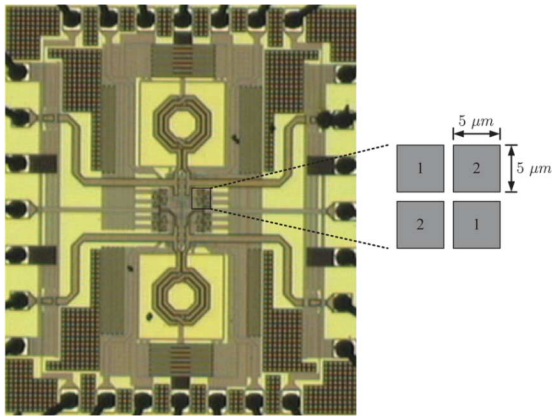
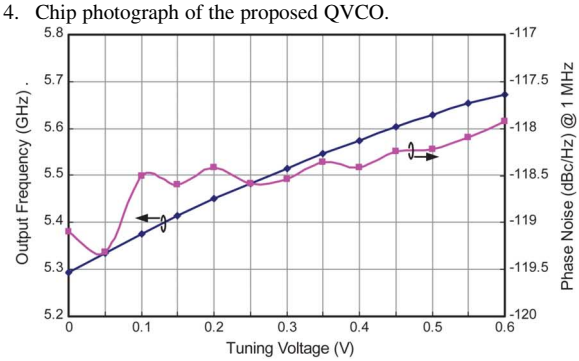
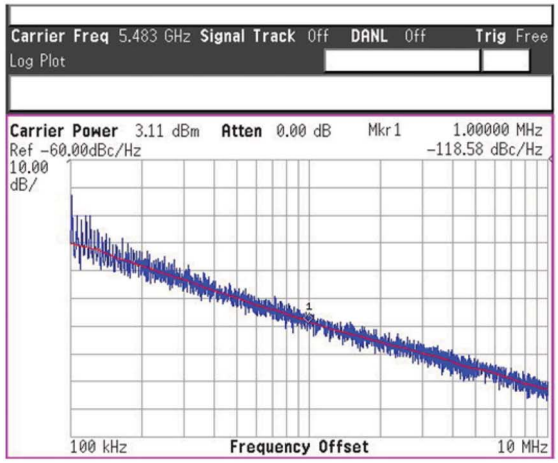


Fig. 4. Chip photograph of the proposed QVCO.



(a)



(b)

Fig. 5. (a) Measured tuning characteristic and phase noise @ 1 MHz, as a function of control voltage, and (b) phase noise plot at 5.48-GHz mid-band.

phase errors due to device mismatch and layout asymmetry are inevitable in practical circuit implementation. Thus, symmetric layout design is necessary to ensure sufficient suppression of the phase error for the QVCO.

Considering the wired effect, the parameters for each distributed device can be extracted as: $C_2 = 122$ fF, $C_s = 7.8$ fF and $r = 472.75\ \Omega$. The physical layout parameters of the transformer are: the number of turns $N = 3$, the line width $W = 15\ \mu$m, and the inner radius $R = 45\ \mu$m, and thereby $L = 1.4$ nH. An accumulation-mode MOS varactor is used for frequency tuning. Using the simulator to extract the value of C_1 which includes the varactor and parasitic capacitances for the inductor and transistors can be approximately from 290 fF to 390 fF. As a result, the last term shown in (5) is very smaller than 1, and thereby we have: $\omega_0 \approx 1/\sqrt{L(C_1 + 2C_2 + 2C_s)}$.

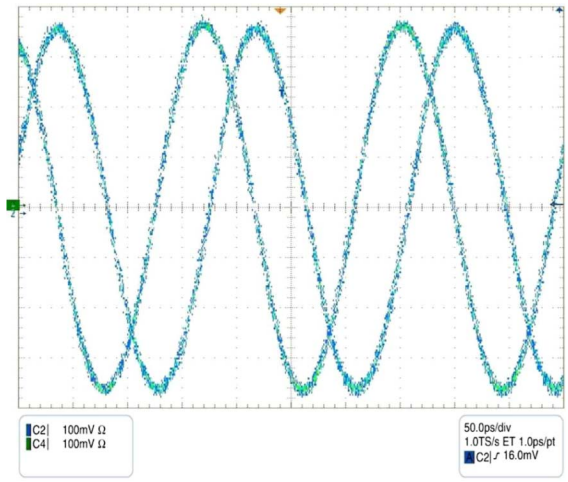


Fig. 6. Measure output waveforms of the I and Q channels. (Horizontal scale: 50 ps/div, vertical scale: 100 mV/div.)

However, the values of C_2 and C_s in MIM device will affect the QVCO tuning range because they are fixed.

In this work, PMOS transistors are employed because they have lower low-frequency flicker noise than NMOS transistors. This implies a lower VCO phase noise can be obtained using PMOS only circuits. Moreover, the proposed QVCO has no coupling transistor as the conventional topologies. It has the advantages of low phase noise and low power performance because the coupling transistors tend to generate additional device noise and consume more power. In addition, the QVCO can achieve low-voltage operation because the circuit consumes only one transistor's voltage headroom.

III. Experimental Results

The proposed distributed oscillator chip was designed and fabricated using standard 0.18 μm CMOS process. The microphotograph of the chip is shown in Fig. 4. The chip size is 1330×1155 $\mu\mathrm{m}^2$ including IO pads while the QVCO core occurs 857×290 $\mu\mathrm{m}^2$. An off-chip regulator circuit is used for power supply and open-drain buffers with external bias tees are used for output measurement. Its frequency characteristic was measured with the spectrum analyzer. The minimum operating supply voltage for the QVCO was 0.6 V. At 0.6 V supply voltage, the amplitude of simulated waveforms in the proposed QVCO was about 1 V. In order to maintain sufficient swing for the measurement, the external bias tees connected to the internal open-drain were supplied by 1.8 V (the standard voltage for 0.18-μm CMOS process).

Fig. 5(a) shows the tuned frequency (from 5.29 to 5.67 GHz) and the phase noise (at 1 MHz offset) variation as the control voltage from 0 to $\mathrm{V_{DD}}$ while power consumption is about 5.2 mW at $\mathrm{V_{DD}} = 0.6$ V. The measured output phase-noise plot from the 5.48-GHz middleband carrier is shown in Fig. 5(b), which shows the output power of 3.1 dBm and the phase noise performance of -118.58 dBc/Hz at 1-MHz offset. By calculation, the figure of merit (FoM) of the proposed QVCO is about -186.2 dB. Using the digital oscilloscope, the measured output quadrature waveforms are shown in Fig. 6. However, the phase errors due to device mismatch and layout asymmetry are inevitable in practical circuit implementation, resulting in 0.8° phase error. Table I lists the overall specifications of the QVCO with several previously published reports [5]–[10]. To achieve quadrature operation, there are five inductor devices used in [7], four inductors used in [9] and three inductors used in [10]. Our core using MIM devices may have less area than them. The phase noise of this work is better than [5], [6] and [9], and the FoM is better than [5]–[8]. In addition, our QVCO can achieve low-voltage operation because the circuit consumes only one transistor's voltage headroom.

TABLE I
Comparison of VCO Performance

Ref.	Tech. (μm)	Freq. (GHz)	V_{DD}/P_{DC} (mW)	FoM (dB)	Phase Error	f_{tuned} (GHz)	Area (mm^2)
[5]	0.18	6.0	1.8/5.8	−182.2	0.5°	1.2	0.84
[6]	0.13	5.5	1.2/5.28	−184.6	1.0°	1.0	N/A
[7]	0.25	5.2	2.5/22	−185	2.6°	0.6	N/A
[8]	0.18	5.31	1/8.0	−185.5	0.33°	0.44	0.57
[9]	0.13	5.5	1/3.56	−187.3	0.34°	0.49	0.94
[10]	0.25	5.44	1.1/9.9	−189.1	0.73°	0.19	0.61
This	0.18	5.48	0.6/5.2	−186.2	0.8°	0.38	0.25*/1.43

* The area of the active core, excluding I/O pads.

IV. Conclusion

A low-voltage QVCO using distributed MIM phase-shift network for four phase generation is proposed. The proposed architecture improves not only the noise performance of the conventional QVCOs, but also saves the area and power consumption of the chip. The QVCO is demonstrated in a standard 0.18 μm CMOS process at a 0.6 V supply voltage with figure of merit comparable to that of other state-of-art QVCO designs.

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