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ANALYSIS OF POWER EFFICIENCY FOR FOUR-PHASE POSITIVE CHARGE PUMPS

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ABSTRACT
In this paper, the compact model of power efficiency for four-phase positive charge pump is derived. The model was verified by using post-layout simulation with 0.25μm triple-well flash memory technology. By including parasitic effects in the pump, the discrepancies between the model and the post-layout simulation results are within 4%**.**

KEY WORDS
Modelling, power efficiency, body effect, threshold voltage, and charge pump

1. Introduction

The charge pump is a DC-DC voltage converter to generate the required voltage higher or lower than the supply voltage. Charge pump circuits are usually applied to flash memory, EEPROM and LCD displays. The most popular schemes are based on the circuit proposed by Dickson [1].

Due to low power requirement in many applications, the power efficiency of the charge pump has become one of the important issues in recent years. Palumbo *et al*. proposed an optimized strategy to design minimum power consumption for the two-phase charge pump [2]. The power efficiency comparison between four-phase charge pump and voltage doublers [3] was presented. Even though the power efficiency of voltage doublers is slightly better, they require both NMOS and PMOS transistors at the same time, unlike four-phase charge pumps only requiring NMOS or PMOS transistors. The SOI CMOS process used to increase efficiency was discussed in [4]-[6]. Although many works have been done for power efficiencies of the two-phase charge pumps and voltage doublers, there have been few reports focused on four-phase charge pumps. In this paper, a complete charge transfer method to analyze the power efficiency is presented for the four-phase charge pump. The resulting model was verified by using a 0.25μm triple-well flash memory process.

This paper is organized as follows. In Section 2, the modified four-phase four-stage positive charge is described. The formulation of power efficiency for the charge pump is derived in the next section. Section 4 shows the agreement of the proposed model and the post-layout simulations. The final conclusions are given in Section 5.

2. The Four-Phase Positive Charge Pump

The performance of the Dickson charge pump is degraded due to threshold voltage and body effect. The modified four-stage positive charge pump with the four-phase clocks is shown in Fig. 1 [7]. The reason to add the transistor M_{si} (i = 1~4) will be given below.

One stage of the charge pump consists of a storage capacitor (C_i = C_L= C, i = 1~4), an NMOS switch (M_i), a gate boosting circuitry (M_i' and C_{gi}), and a body control transistors M_{si}. During the charge transferring period, the charge stored in C_i is transferred to C_{i+1} of the next stage through the switch transistor, M_i. In order to eliminate the threshold voltage degradation in M_i, the gate boosting circuitry is used to raise much higher gate voltage of M_i. The conventional method to avoid body effect of M_i is achieved by tie the well to its drain. However, the high instantaneous PN junction between the well and the source may cause higher noise in the chip, thus the reliability may become an issue. To minimize the noise issue, the transfer switch M_{si} is used to track the well to the lowest potential in each stage to avoid body effects [8].

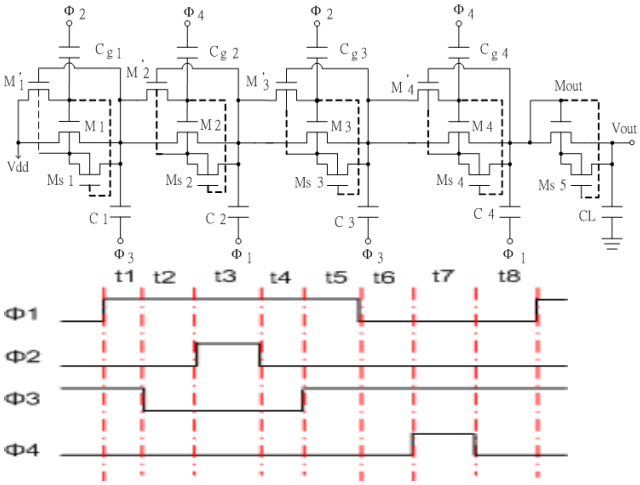


Fig. 1. The modified four-stage positive charge pump and the four-phase clocks

The output of an N-stage four-phase positive charge pump can be given as

$$V_{out} = (N+1)\left(\frac{C}{C+C_{top}}\right)V_{DD} - V_{tn} - \frac{NI_{load}}{f(C+C_{top})} \quad (1)$$

where V_{tn} is the threshold voltage of switch M_{out}, C_{top} is the switch-node parasitic capacitance, I_{load} is the load current, and f is clock frequency whose amplitude is V_{DD}.

3. Compact Model of Power Efficiency

To calculate the power efficiency of the four-phase positive charge pump, the power consumption must be evaluated. The power consumption in the charge pump includes the storage capacitor C_i, the boosting capacitor C_{gi}, the bottom-plate (C_{bot}) and the top-plate (C_{top}) parasitic capacitances of C_i, as well as the bottom-plate (C_{bg}) and the top-plate (C_{tg}) parasitic capacitances of C_{gi}. Actually, the total switch-node parasitic capacitors include the gate capacitance of M_i', C_{db} of M_i', C_{db} and C_{sb} of M_i, and C_{db} of M_{si} [6]. For simplicity, those parasitic capacitances are assumed to be included in C_{top} and C_{tg} in the following analysis. Moreover, the ideal clock signals without buffers are directly connected to the bottom plates of C_i and C_{gi} for power efficiency analyses [1], since the sizes of buffers influence the power consumption and the waveforms of clocks.

The clock cycles are divided into eight different intervals in time. Figs. 2 to 5 illustrate the charge distribution of the four-phase positive charge pump in time intervals $t1$, $t3$, $t5$ and $t7$, respectively. During $t1$, M_1', M_3' and M_{out} are turned on and the charges of V_{DD} and ϕ_1 are transferred to C_{g1}, C_{g3} and C_L, respectively. At time interval $t3$, the charges of V_{DD} and C_2 are transferred to C_1 and C_3 through M_1 and M_3, respectively. During $t5$, similar to $t1$, M_2' and M_4' turn on and the charges of ϕ_3 are delivered to C_{g2} and C_{g4}. Similarly, at time $t7$, those charges stored in C_1 and C_3 are transferred to C_2 and C_4 through M_2 and M_4, respectively. Nevertheless, there is no charge consumed in the others time interval.

The clock cycles are divided into eight different intervals in time. Figs. 2 to 5 illustrate the charge distribution of the four-phase positive charge pump in time intervals $t1$, $t3$, $t5$ and $t7$, respectively. During $t1$, M_1', M_3' and M_{out} are turned on and the charges of V_{DD} and ϕ_1 are transferred to C_{g1}, C_{g3} and C_L, respectively. At time interval $t3$, the charges of V_{DD} and C_2 are transferred to C_1 and C_3 through M_1 and M_3, respectively. During $t5$, it is similar to $t1$ that M_2' and M_4' are turned on and the charges of ϕ_3 are delivered to C_{g2} and C_{g4}. Similarly, at time $t7$, those charges stored in C_1 and C_3 are transferred to C_2 and C_4 through M_2 and M_4, respectively. Nevertheless, there is no charge consumed in the other time intervals.

From $t1$ to $t8$, the charges provided by V_{DD} are

$$\Delta Q_{t1} = \Delta Q + 2\Delta Q_{bot} + 3\Delta Q_{top} + 2\Delta Q_g + 2\Delta Q_{tg} \quad (2)$$

$$\Delta Q_{t3} = 2\Delta Q + 2\Delta Q_{top} + 2\Delta Q_{bg} + 2\Delta Q_{tg} \quad (3)$$

$$\Delta Q_{t5} = 2\Delta Q_{bot} + 2\Delta Q_{top} + 2\Delta Q_g + 2\Delta Q_{tg} \quad (4)$$

$$\Delta Q_{t7} = 2\Delta Q + 2\Delta Q_{top} + 2\Delta Q_{tg} + 2\Delta Q_{bg} \quad (5)$$

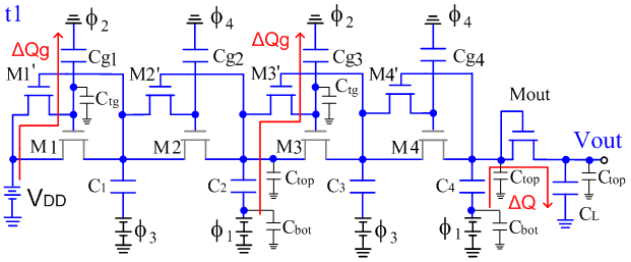


Fig. 2. Charge transfer during $t1$ (ϕ_1 = ϕ_3 = high, ϕ_2 = ϕ_4 = low)

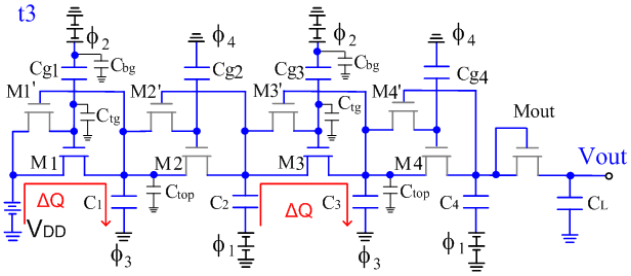


Fig. 3. Charge transfer during $t3$ (ϕ_1 = ϕ_2 = high, ϕ_3 = ϕ_4 = low)

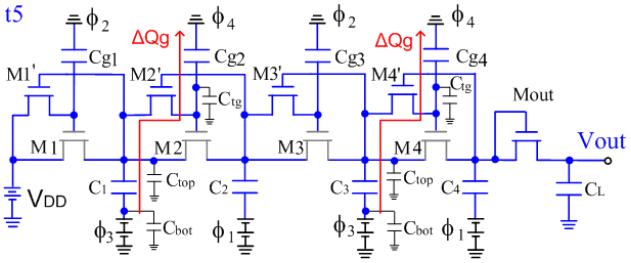


Fig. 4. Charge transfer during $t5$ (ϕ_1 = ϕ_3 = high, ϕ_2 = ϕ_4 = low)

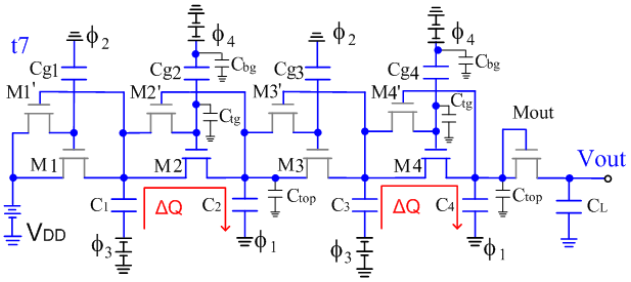


Fig. 5. Charge transfer during $t7$ (ϕ_1 = ϕ_2 = low, ϕ_3 = ϕ_4 = high)

The total charge provided by the power supply in one clock cycle is the sum of Eqns. (2) to (5).

$$\Delta Q_{1T} = 5\Delta Q + 4\Delta Q_{bot} + 9\Delta Q_{top} + 4\Delta Q_g + 8\Delta Q_{tg} + 4\Delta Q_{bg} \quad (6)$$

Therefore, the total current consumption of the four-phase charge pump is

$$I_{total} = 5I_{load} + 4I_{bot} + 9I_{top} + 4I_g + 8I_{tg} + 4I_{bg} \quad (7)$$

This analysis can be extended to any number of stages. For an N-stage charge pump, the total current consumption can be expressed as

$$I_{total} = (N+1)I_{load} + NI_{bot} + (2N+1)I_{top} + NI_g + 2NI_{tg} + NI_{bg} \quad (8)$$

The current that charges and discharges the bottom plate and the top plate of the storage capacitor is given as [6]

$$I_{bot} = C_{bot} \cdot V_{DD} \cdot f \quad (9)$$

$$I_{top} = \frac{C_{top}}{C + C_{top}} \cdot I_{load} \quad (10)$$

where V_{DD} is the supply voltage and I_{load} is the output loading current.

Similarly, $I_{bg} = C_{bg} \cdot V_{DD} \cdot f$ and $I_{tg} = \frac{C_{tg}}{C_{gi} + C_{tg}} \cdot I_g$ can be obtained for the bottom plate and the top plate of the boosting capacitor, where I_g is the current that charges the boosting capacitor.

By definition, the power efficiency of the charge pump may be written as follows.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} I_{load}}{V_{DD} I_{total}} \quad (11)$$

By substituting the above expressions of currents and V_{out} into Eqn. (11), the efficiency η can be written in Eqn. (12).

$$\eta = \frac{(N+1)(\frac{C}{C+C_{top}})V_{DD} - V_{tn} - \frac{NI_{load}}{f \cdot (C+C_{top})}}{V_{DD}\left[(N+1) + \frac{NC_{bot}V_{DD}f}{I_{load}} + \frac{(2N+1)C_{top}}{C+C_{top}} + \frac{NI_g}{I_{load}} + 2N\frac{I_g \cdot C_{tg}}{I_{load}(C_{gi}+C_{tg})} + N\frac{C_{bg}V_{DD}f}{I_{load}}\right]} \quad (12)$$

Since the bottom-plate and the top-plate parasitic capacitance C_{bot} and C_{top} are nearly proportional to the storage capacitor C, we may assume $C_{bot} = \alpha C$ and $C_{top} = \beta C$. Hence, Eqns. (9) and (10) become

$$I_{bot} = \alpha \cdot C \cdot V_{DD} \cdot f \quad (13)$$

$$I_{top} = \frac{\beta \cdot C}{C + \beta \cdot C} \cdot I_{load} = \frac{\beta}{1+\beta} \cdot I_{load} \quad (14)$$

Similarly, C_{bg} and C_{tg} are also fractions of the boosting capacitor C_{gi} so that $C_{bg} = \alpha_g C_{gi}$ and $C_{tg} = \beta_g C_{gi}$. I_{bg} and I_{tg} can be expressed as

$$I_{bg} = \alpha_g \cdot C_{gi} \cdot V_{DD} \cdot f \quad (15)$$

$$I_{tg} = \frac{\beta_g \cdot C_{gi}}{C_{gi} + \beta_g \cdot C_{gi}} \cdot I_g = \frac{\beta_g}{1+\beta_g} \cdot I_g \quad (16)$$

Since the storage capacitance is more than an order of magnitude larger than boosting capacitor. Therefore, it can be assumed that C_{gi} is a fraction of C to have $C_{gi} = \gamma C$. Thus, Eqn. (12) can be rewritten as

$$\eta = \frac{(N+1)(\frac{1}{1+\beta})V_{DD} - V_{tn} - \frac{NI_{load}}{f \cdot (1+\beta) \cdot C}}{V_{DD}\left[(N+1) + \frac{N\alpha C V_{DD} f}{I_{load}} + \frac{(2N+1)\beta}{1+\beta} + N\gamma + 2N\frac{\gamma \cdot \beta_g}{1+\beta_g} + N\frac{\alpha_g \cdot C\gamma V_{DD} f}{I_{load}}\right]} \quad (17)$$

4. Model Verification

To verify the compact model obtained in the previous section, the post-layout SPICE simulations were carried out with 0.25 μm triple-well flash memory technology. The threshold voltage of the NMOS is about 0.65 V. The storage capacitance and the boosting capacitance for the charge pump are 35 pF and 1 pF, respectively. The parameters α and β based on the post-layout parasitic parameter extraction for the charge pump are α = 0.171 and β = 0.022. Similarly, the parameters related to the boosting capacitors α_g and β_g are 0.185 and 0.019, respectively.

A set of simulation results was performed by varying the supply voltage from 1.2 V to 2 V with the output current from 20 μA to 240 μA at the frequency of 6MHz or 10MHz. Power efficiency and V_{out} are compared between the compact model and post-layout simulations in Figs. 6 to 9. The simulations agree well with the model with the maximum errors lower than 4%.

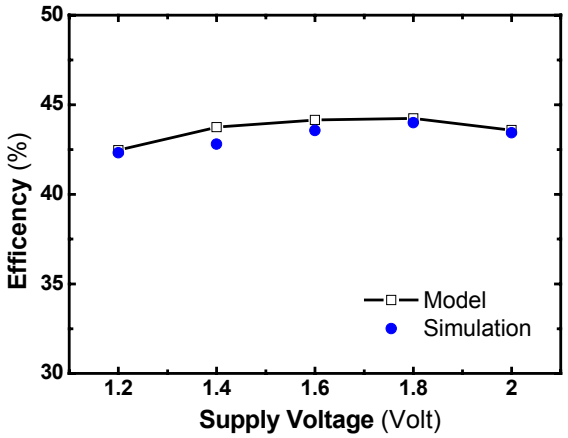


Fig.6. Power efficiencies versus supply voltages for the four-stage pump with f = 10 MHz and output current = 140 μA

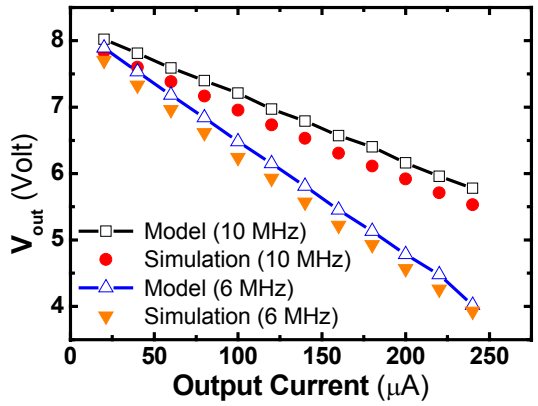
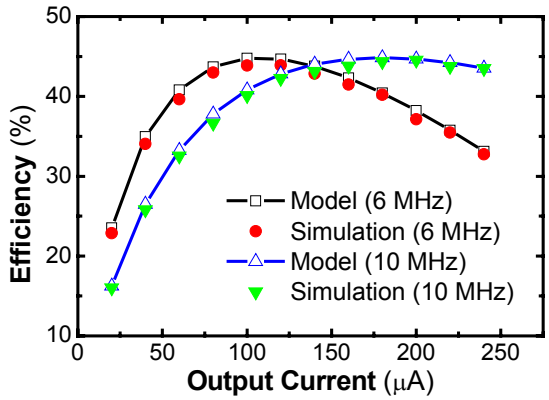


Fig. 7. Output voltages vs. loading currents for the four-stage positive charge pump with V_{DD} = 1.8 V



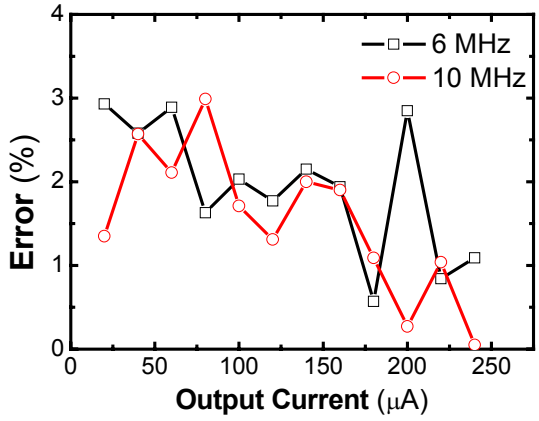


Fig. 8. Power efficiencies and error percentage between the model and simulations are plotted as functions of loading current for the four-stage charge pump with V_{DD} = 1.8 V.

5. Conclusion

In this work, a theoretical analysis of power efficiency is presented for the four-phase positive charge pump with body potential control to avoid body effects and minimize noise due to PN junction conduction. The compact model well agrees with the post-layout simulation results. The maximum errors are always less than 4% for various loading currents and supply voltages. This model should be very helpful for design of stage number, capacitors and operation frequency of positive four-phase charge pumps.

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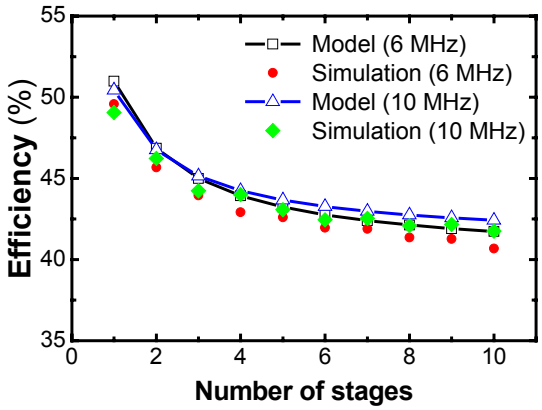

Fig. 9. Power efficiencies versus stage numbers for the four-stage charge pump with output current of 140 μA and V_{DD} = 1.8 V.

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