Enhanced p-Channel Metal–Oxide–Semiconductor Field-Effect Transistor Charge Pump for Low-Voltage Applications

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In this paper, a power-efficient two-phase p-channel metal–oxide–semiconductor field-effect transistor (PMOSFET) charge pump with two auxiliary clocks to boost the gate biases of the switching transistors is proposed for low-voltage applications. It can increase overdrive voltages of the switching transistors, preserve low voltage drops within the transistors, and work well at a reduced supply voltage. Simulation results show that the proposed two-stage charge pump improves the voltage gain by more than 30% for 0.35 µm complementary metal–oxide–semiconductor (CMOS) field-effect transistor (FET) technology and improves the maximum power efficiency by 40% for 0.18 µm CMOS technology in comparison with Racape and Daga's charge pump. Measurement results show that the voltage gains of the proposed two-stage charge pump are more than 95.7 and 92% at supply voltages higher than 1.4 and 0.7 V for 0.35 and 0.18 µm CMOS technologies, respectively. A compact model of power efficiency for the proposed charge pump is derived and verified by simulations and measurements. Results show that the power efficiency can be approximately 60% at low supply voltages.

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1. Introduction

Charge pump circuits are DC–DC voltage converters used to generate positive voltages that increase the supply voltage or negative voltages. They are extensively applied to flash memories, electrically erasable programmable read-only memories (EEPROMs), liquid crystal displays (LCDs) and so on. The most conventionally adopted schemes are based on the Dickson structure using n-channel metal–oxide–semiconductor (NMOS) field-effect transistors.[1)] In recent years, many charge pumps[2–7)] have been proposed to reduce the effects of the body effect and threshold voltage as the number of stages increases. Therefore, the voltage gain of these charge pumps can be improved and the output voltages of the charge pump circuits can be nearly proportional to the number of stages.

Racape and Daga[3)] proposed a simple p-channel metal–oxide–semiconductor field-effect transistors (PMOSFET) charge pump that can reduce the effect of threshold voltage, keep a low voltage difference between any two electrodes in a transistor, and be implemented using low-cost twin-well complementary metal–oxide–semiconductor field-effect transistor (CMOSFET) technology. Note that if an NMOS is used in triple-well technology, since a deep N-well is required, a larger chip area overhead is required. However, the boosted gate voltages degrade significantly at low supply voltages or high output currents. Thus, the output voltage of Racape and Daga's charge pump is reduced. In this paper, a simple two-phase clock scheme is proposed to increase the overdrive voltage of transfer devices without degrading the other good characteristics for low-voltage applications. Simulations and measurements using 0.18 and 0.35 µm CMOS technologies were performed to demonstrate the performance of the proposed charge pump.

In addition, power efficiency is important owing to the recent trend of green energy. To show how high the power efficiency is, a compact power efficiency model was derived for the proposed charge pump on the basis of the charge balance method[8,9)] with parasitic capacitance effects. The model was then verified by simulations and measurements.

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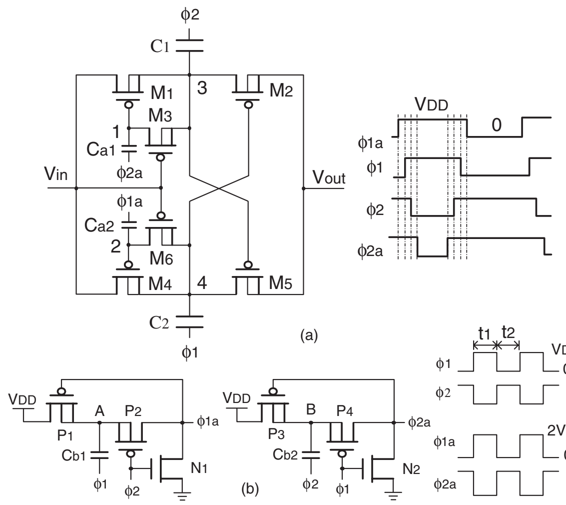


Fig. 1. (a) One stage of Racape/Daga's charge pump as described in ref. 3. (b) Proposed clock scheme.

This paper is organized as follows. In §2, the driving capability of Racape and Daga's charge pump is analyzed. In §3, the proposed PMOSFET (PMOS) charge pump circuit is presented. In §4, the power efficiency model is derived. In §5, the agreement between the model, simulation, and measurement of the proposed scheme is demonstrated. Conclusions are drawn in §6.

2. Analysis of Driving Capability

Figure 1(a) shows one stage of Racape and Daga's charge pump[3)] consisting of four-phase clock waveforms with the amplitude V_{DD}. Each stage consists of six transistors including two major switching transistors, M_1 and M_4, a pair of pumping capacitors, C_1 and C_2, and a pair of auxiliary capacitors, C_{a1} and C_{a2}. During pumping, the voltages at nodes 1 and 2 of the first stage are varied from V_{low} to $2V_{DD}$. V_{low} is given as[3)]

$$V_{low} = V_{in} + V_t - V_{DD}\left(\frac{C_{ai}}{C_{par} + C_{ai}}\right), \qquad (1)$$

where C_{ai} ($i = 1$ to 2) indicates the auxiliary capacitance, C_{par} is the total parasitic capacitance at node 1 or 2, and V_t is

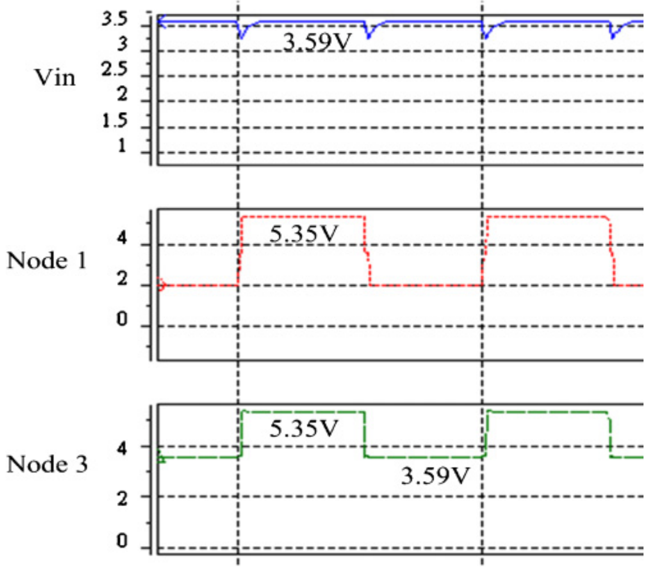


Fig. 2. (Color online) Simulated waveforms of the second stage of the proposed charge pump using 0.35 μm CMOS technology at $V_{DD} = 1.8$ V and $f = 10$ MHz.

the absolute value of the threshold voltage of the PMOSFET. If the parasitic capacitance compared with the auxiliary capacitance C_{ai} is very small and $V_{in} = V_{DD}$, V_{low} is equal to V_t. The minimum supply voltage should exceed $2V_t$.[3)]

If the on-resistance of the switching transistor is neglected, the output voltage of an N-stage charge pump can be expressed as

$$V_{out} = V_{DD} + \left(\frac{N}{1+\beta}\right)V_{DD} - I_{out}R_{out}, \tag{2}$$

where I_{out} is the output current, R_{out} is the output resistance, β is the ratio of the top-plate parasitic capacitance to the pumping capacitance, and R_{out} is equal to $N/2fC_i$, C_i ($i = 1$ to 2) being the pumping capacitance and f being the clock frequency. When the resistance of the switching transistor is considered, R_{out} can be approximated as[10)]

$$R_{out} = \frac{N}{2fC_i}\coth\left(\frac{T_{on}}{r_{on}C_i}\right), \tag{3}$$

where T_{on} is the time when the switching transistor is on in one clock cycle and $r_{on} \cong L/\mu C_{ox}WV_{ov}$. V_{ov} is the overdrive voltage of the switching transistor. The overdrive voltage of Racape/Daga's charge pump is expressed as

$$V_{ov} = V_{DD} - V_{low} - V_t - I_{out}R_{out}. \tag{4}$$

This implies lower supply voltages or larger output currents resulting in lower V_{ov}, thus, higher r_{on} and R_{out}. In this situation, the driving capacity of the charge pump is degraded.

3. Enhanced PMOS Charge Pump

A two-phase clock scheme used to increase the overdrive voltage of the transfer devices is presented in Fig. 1(b). Notably, four-phase clocks are not required. According to Fig. 1(b), two auxiliary clocks, ϕ_{1a} and ϕ_{2a}, are generated from two out-of-phase clocks, ϕ_1 and ϕ_2, by a pair of level shifters. Note that many different level shifters can be used. Some of them can preserve low voltage drops within the transistors with more complex circuits.[11,12)] Here, a simple version requiring high-voltage NMOSFETs (N_1 and N_2) is used. One level shifter has three transistors. When ϕ_1 switches to low and ϕ_2 switches to high, transistors N_1 and P_1 are turned on. At this moment (t_1), ϕ_{1a} switches to low and charge is transferred from V_{DD} to node A. Then, ϕ_1 switches to high and ϕ_2 switches to low, transistors N_1 and P_1 are turned off, and transistor P_2 is turned on to transform ϕ_{1a} to $2V_{DD}$. The operation of the auxiliary clock ϕ_{2a} is similar to that of the clock ϕ_{1a} but with a 180° phase difference.

In the proposed charge pump, since the voltages at nodes 1 and 2 are varied from 0 to $2V_{DD}$, according to eq. (4), the overdrive voltages of M_1 and M_4 are increased to $V_{DD} - V_t - I_{out}R_{out}$. Figure 2 shows the simulated waveforms at the second stage of the proposed charge pump with $V_{DD} = 1.8$ V, $f = 10$ MHz, and $I_{out} = 0$. In Fig. 2, the voltage waveform of node 1 varies between V_{DD} and $3V_{DD}$. This indicates that the overdrive voltage of the second stage of the proposed charge pump is approximately equal to $V_{DD}-V_t$ as node 1 switches to V_{DD} and node 3 switches to $2V_{DD}$. It is worth noting that the voltage differences within transistors M_1 and M_3 are always less than V_{DD}. Theoretically, the supply voltage of the proposed method without output current can be reduced to V_t.

4. Compact Model of Power Efficiency

The power efficiency (η) of a charge pump is defined as the output power P_o divided by the input power P_i,

$$\eta = \frac{P_o}{P_i} = \frac{V_{out}I_{out}}{V_{DD}I_{power}}, \tag{5}$$

where I_{out} is the output current, I_{power} is the current drawn from the power supply, and V_{out} is the output voltage.

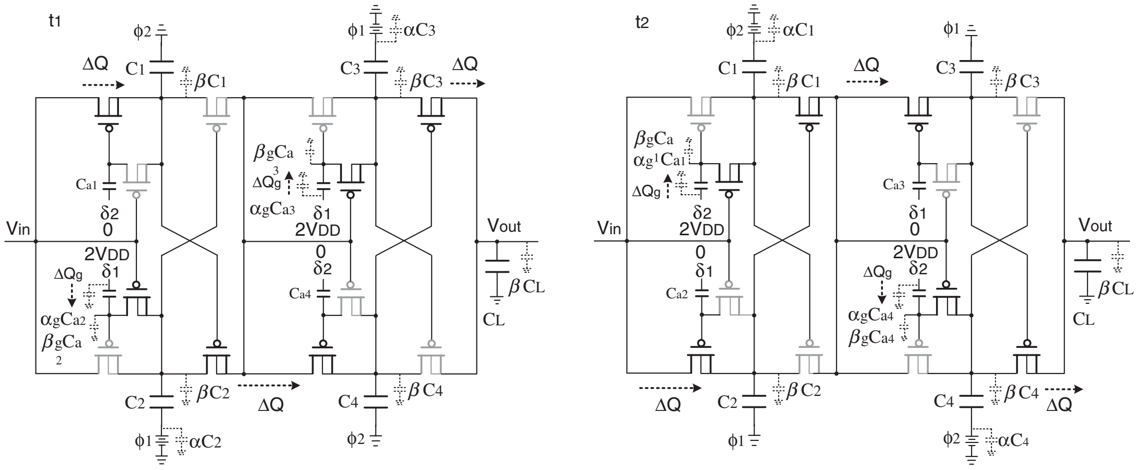
Figures 3(a) and 3(b) show the charge transfer of the proposed two-stage PMOS charge pump at the time intervals t_1 and t_2, respectively. Transistor symbols with gray lines indicate that the transistors are off, while those with black lines indicate that the transistors are on. Charge can be transferred only if the transistors are on. From Fig. 3(a), ΔQ indicates the charge transferred to the pumping capacitor by the power supply or clocks at t_1. ΔQ_{top} is the charge loss due to the top-plate parasitic capacitance and ΔQ_{bot} is the charge loss due to the bottom-plate parasitic capacitance of the pumping capacitor. Here, C_L is assumed to be equal to C_i, where $i = [1, 4]$. Similarly, the charge transferred to the auxiliary capacitor is ΔQ_g, and the charge loss due to the top-plate and bottom-plate parasitic capacitances of the auxiliary capacitor are given as ΔQ_{gt} and ΔQ_{gb}, respectively. Hence, the charges provided by the power supply and clocks at t_1 or t_2 can be analyzed and written as

$$Q_{t1} = Q_{t2} = 3\Delta Q + 2\Delta Q_{bot} + 5\Delta Q_{top} + 4\Delta Q_g + 4\Delta Q_{gb} + 4\Delta Q_{gt}. \tag{6}$$

The total charge provided by the power supply and clocks in one clock cycle is $\sum \Delta Q_{ti}$, where $i = [1, 2]$.

$$Q_T = 6\Delta Q + 4\Delta Q_{bot} + 10\Delta Q_{top} + 8\Delta Q_g + 8\Delta Q_{gb} + 8\Delta Q_{gt}. \tag{7}$$

Since the charge pump has two branches, the charge transfer to the output occurs twice in one clock cycle (T). The total current consumption can be obtained using eq. (7) by converting charge into current with a division factor of 2.



(a) (b)

Fig. 3. Charge transfer of the proposed two-stage charge pump at (a) time t_1 and (b) time t_2.

$$I_{\rm power} = 3I_{\rm out} + 2I_{\rm bot} + 5I_{\rm top} + 4I_{\rm g} + 4I_{\rm gb} + 4I_{\rm gt}. \quad (8)$$

The above expression can be extended to N stages as

$$I_{\rm power} = (N+1)I_{\rm out} + NI_{\rm bot} + (2N+1)I_{\rm top} + 2NI_{\rm g} + 2NI_{\rm gb} + 2NI_{\rm gt}. \quad (9)$$

The currents that charge or discharge the bottom- and top-plate parasitic capacitances of the pumping and auxiliary capacitors exhibit the following relationships:[5)]

$$I_{\rm bot} = \alpha C \cdot V_{\rm DD} \cdot f, \quad (10)$$

$$I_{\rm top} = \frac{\beta}{1+\beta} \cdot I_{\rm out}, \quad (11)$$

$$I_{\rm gb} = \alpha_{\rm g} C_{\rm a} \cdot V_{\rm DD} \cdot f, \quad (12)$$

$$I_{\rm gt} = \frac{\beta_{\rm g}}{1+\beta_{\rm g}} \cdot I_{\rm g}. \quad (13)$$

As shown in Figs. 3(a) and 3(b), α and β are the ratios of the bottom- and top-plate parasitic capacitances to the pumping capacitance C ($C_i + C_{i+1}$), respectively. $\alpha_{\rm g}$ and $\beta_{\rm g}$ are the ratios of the bottom- and top-plate parasitic capacitances to the auxiliary capacitance $C_{\rm a}$ ($C_{{\rm a}i} + C_{{\rm a}i+1}$), respectively. $I_{\rm g}$ is the current from the pumping capacitor.

Substituting eqs. (10)–(13) into eq. (9), the power efficiency η can be formulated as

$$\eta = \frac{V_{\rm DD} + \left(\dfrac{N}{1+\beta}\right)V_{\rm DD} - \dfrac{NI_{\rm out}}{fC(1+\beta)}}{V_{\rm DD}\left[(N+1) + \dfrac{N\alpha CV_{\rm DD}f}{I_{\rm out}} + \dfrac{(2N+1)\beta}{1+\beta} + 2N\dfrac{I_{\rm g}}{I_{\rm out}} + 2N\dfrac{\alpha_{\rm g}C_{\rm a}V_{\rm DD}f}{I_{\rm out}} + 2N\dfrac{I_{\rm g}\beta_{\rm g}}{(1+\beta_{\rm g})I_{\rm out}}\right]}. \quad (14)$$

5. Simulation and Measurement Results

The Racape/Daga's and proposed charge pumps were simulated using 0.35 and 0.18 μm CMOS technologies. Both charge pumps were designed using the same capacitors, clock frequency, and transistor sizes. Pumping and auxiliary capacitances of 30 and 0.5 pF were respectively selected for both pumps. The parameters α, β, $\alpha_{\rm g}$, and $\beta_{\rm g}$ of the proposed charge pump based on the post layout parasitic parameter extraction for 0.35 and 0.18 μm CMOS technologies are 0.128, 0.03, 0.128 and 0.02, and 0.087, 0.04, 0.087 and 0.02, respectively.

For 0.35 μm CMOS technology, the post layout simulated output voltages of the two-stage Racape/Daga's and proposed charge pumps versus supply voltages without output current at frequencies of 10 and 12 MHz are shown in Fig. 4. The output voltages increase linearly when the supply voltage is increased. The proposed charge pump improves the voltage gain by more than 30% in comparison with Racape and Daga's charge pump.

Figure 5 shows the performance characteristics of the two-stage Racape and Daga's and proposed charge pumps as functions of output current at frequencies of 10 and 12 MHz with $V_{\rm DD} = 1.8$ V. In general, the proposed charge pump has higher boosted output voltages than Racape and Daga's charge pump, because it has higher overdrive voltages. This indicates that the proposed charge pump is more suitable for lower voltage applications. The simulated output voltages and power efficiencies of both two-stage charge pumps at a supply voltage of 1.8 V and a frequency of 12 MHz are shown in Fig. 6. The maximum simulated power efficiencies of the Racape and Daga's and proposed charge pumps are 45.42% at an output current of 100 μA and 64.3% at an output current of 120 μA, respectively. The proposed charge pump improves the maximum output voltage and power efficiency by approximately 34 and 40%, respectively, as compared with Racape and Daga's charge pump.

Figure 7 shows the chip microphotograph of the proposed two-stage charge pump with areas of about 0.879 and 0.604 mm^2 for 0.35 and 0.18 μm CMOS technologies, respectively.

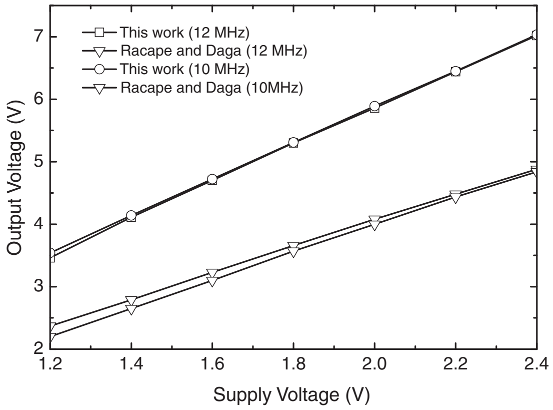


Fig. 4. Comparison of simulated output voltages of the two two-stage charge pumps as functions of supply voltage with $I_{out} = 0$ and frequencies of 10 and 12 MHz using 0.35 μm CMOS technology.

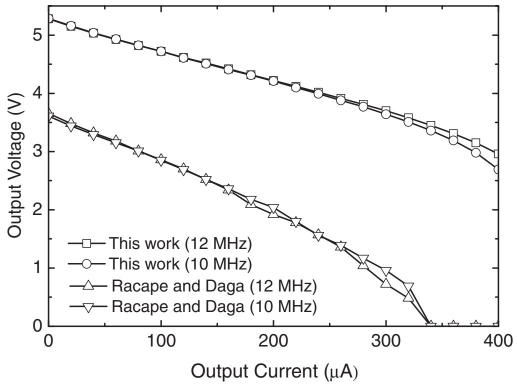


Fig. 5. Comparison of simulated output voltages of the two-stage charge pumps as functions of output current with $V_{DD} = 1.8$ V and frequencies of 10 and 12 MHz using 0.35 μm CMOS technology.

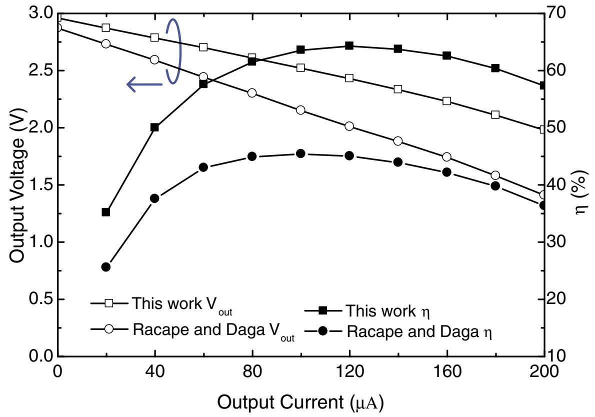


Fig. 6. (Color online) Comparison of simulated output voltages and power efficiencies of the two-stage charge pumps as functions of output current with $f = 12$ MHz and $V_{DD} = 1$ V using 0.18 μm CMOS technology.

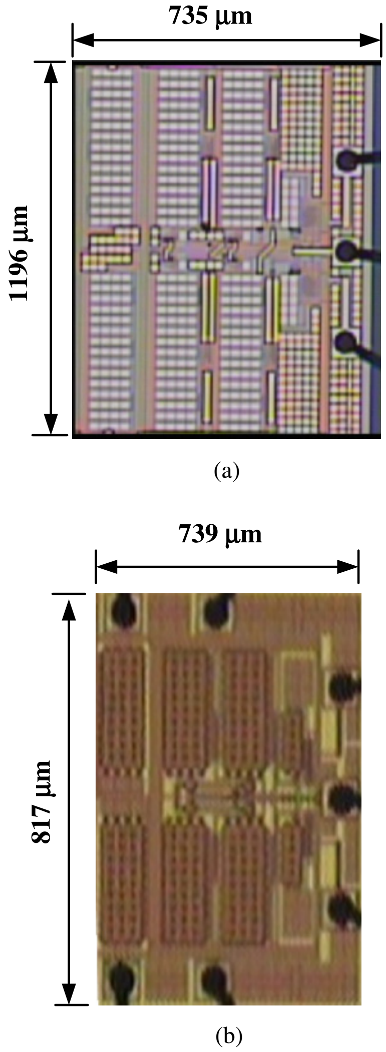


Fig. 7. (Color online) Microphotographs of the proposed two-stage PMOS charge pumping circuit using (a) 0.35 (b) 0.18 μm CMOS technologies.

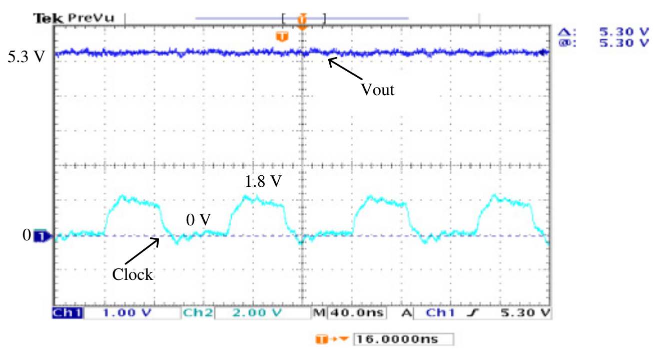


Fig. 8. (Color online) Measured output voltage and clock waveforms of the proposed PMOS charge pump with $I_{out} = 0$ at $f = 10$ MHz and $V_{DD} = 1.8$ V using 0.35 μm CMOS technology.

For 0.35 μm CMOS technology, Fig. 8 shows the measured output and clock waveforms of the proposed two-stage charge pump at a frequency of 10 MHz and $V_{DD} = 1.8$ V. The measured output voltages of the proposed charge pump for different supply voltages without output current are shown in Fig. 9. The measured maximum voltage gains of the proposed charge pump are 97.5% at a supply voltage of 1.6 V and 99.05% at a supply voltage of 1.4 V for frequencies of 10 and 12 MHz, respectively. A voltage gain of more than 95.7% is achieved when the supply voltage is higher than 1.4 V. Figure 10 also demonstrates the agreement between the simulated and measured boosted output voltages versus output current for different supply voltages at 10 MHz.

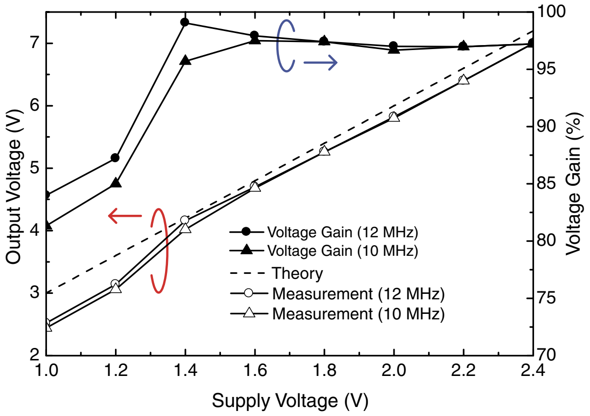


Fig. 9. (Color online) The measured output voltages vs supply voltage for the proposed two-stage charge pump are very close to the theoretical values for $I_{out} = 0$ and $V_{DD} = 1.8$ V at frequencies of 10 and 12 MHz using 0.35 μm CMOS technology.

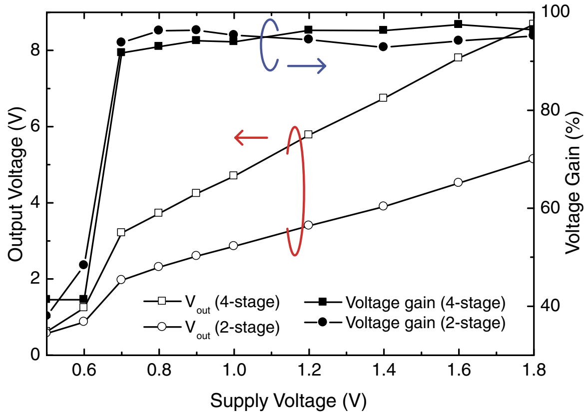


Fig. 11. (Color online) Measured output voltages vs supply voltage of the proposed two-stage and four-stage charge pumps without output current at $f = 10$ MHz and $V_{DD} = 1.8$ V using 0.18 μm CMOS technology.

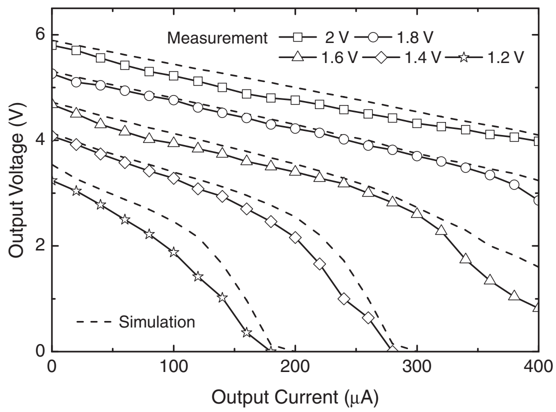


Fig. 10. Comparison of output voltages vs output current between measurement and simulation for various supply voltages at $f = 10$ MHz and $V_{DD} = 1.8$ V using 0.35 μm CMOS technology.

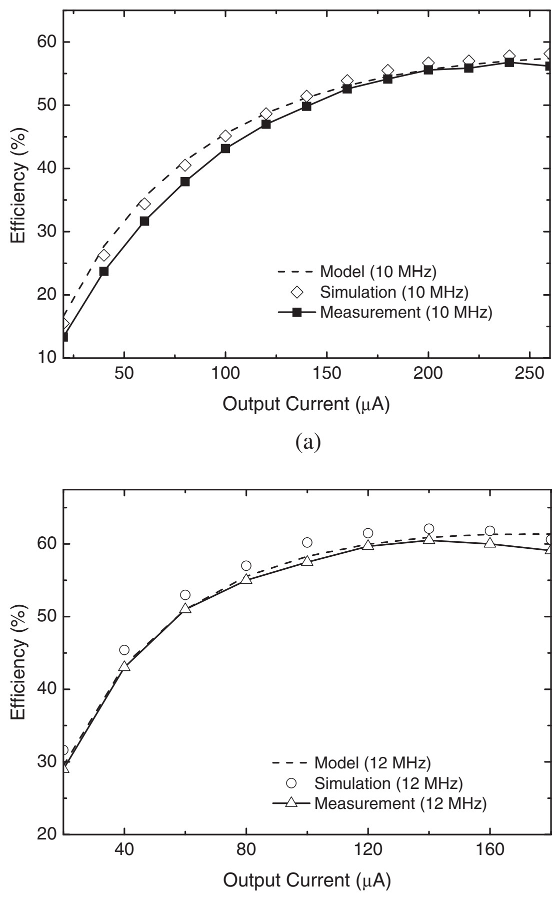


Fig. 12. Comparison of power efficiencies between model, measurement, and simulation as functions of I_{out} (a) at $f = 10$ MHz and $V_{DD} = 1.8$ V using 0.35 μm CMOS technology and (b) at $f = 12$ MHz and $V_{DD} = 1$ V using 0.18 μm CMOS technology.

For 0.18 μm CMOS technology, the measured output voltages of the proposed two- and four-stage charge pumps without output current at $V_{DD} = 1.8$ V and $f = 10$ MHz are plotted in Fig. 11. The measured maximum voltage gains of the proposed two- and four-stage charge pumps are 96.3% at a supply voltage of 0.9 V and 97.5% at a supply voltage of 1.6 V, respectively. The voltage gain is more than 92% even at a supply voltage of 0.7 V.

Figure 12 shows that the proposed power efficiency model of the proposed two-stage charge pump as a function of output current agrees well with the simulated and measured data. Figure 12(a) shows that the measured maximum efficiency is about 57% at an output current of 240 μA, $V_{DD} = 1.8$ V, and $f = 10$ MHz with 0.35 μm CMOS technology. Figure 12(b) also shows that the measured maximum efficiency is 61% at an output current of 140 μA, $V_{DD} = 1$ V, and $f = 12$ MHz with 0.18 μm CMOS technology.

6. Conclusions

The proposed two-phase PMOS charge pumps fabricated using 0.35 μm twin-well and 0.18 μm triple-well CMOS technologies with areas of about 0.879 and 0.604 mm^2, respectively, achieve high voltage gains and high power efficiencies as compared with Racape and Daga's charge pump. With the proposed clock scheme, the overdrive voltage of the switching transistors is increased to $V_{DD} - V_t$ instead of $V_{DD} - 2V_t$ at zero load, the supply voltage can be reduced, and the voltage drops within the transistors are always less than V_{DD} for good device reliability. Thus, the proposed charge pump is suitable for low-voltage applications. The measured voltage gains of the proposed two-stage charge pump are more than 95.7 and 92% with V_{DD} values higher than 1.4 and 0.7 V for 0.35 and 0.18 μm CMOS technologies, respectively. A compact power efficiency model was derived on the basis of the charge balance method with good agreement with the measured data obtained from test chips. The results show that the proposed PMOS charge pump improves the voltage gain by more than 30% and the maximum power efficiency by more than 40% using 0.18 μm CMOS technology in comparison with Racape and Daga's charge pump.

Acknowledgments

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