Analytical Models of Output Voltages and Power Efficiencies for Multistage Charge Pumps

Chien-Pin Hsu and Hongchin Lin

Abstract—Accurate analytical models of the output voltage and the power efficiency of voltage doublers and PMOS charge pumps are derived using dynamic charge transfer waveforms and charge balance methods, respectively. Since the on-resistance of switching devices and the parasitic capacitance can be estimated precisely, the proposed models are more accurate than the other existing models. The model-generated values agree well with simulations and measurements for these two charge pumps using 0.18 µm CMOS technology. The expressions for the output voltages prove that the PMOS charge pump can provide more output current without a significant increase in the sizes of transistors. Finally, the design methodology that is based on these models is developed to determine the transistor sizes, capacitance, and number of stages for the maximum power efficiency.

Index Terms—Analytical model, charge pump, design methodology, output voltage, power efficiency.

I. INTRODUCTION

C HARGE pump circuits are widely applied to flash memories and electrically erasable programmable read-only memory (EEPROM) to provide voltages higher than the supply voltage so as to program or erase memory cells. Most of the charge pumps are based on the Dickson structure using MOS transistors as switches [1]. However, the threshold voltage and body effect degrades the performance of the charge pump when the number of stages is raised. Various charge pump topologies [2]–[11] have been proposed to minimize the influence of body effect and threshold voltage. Thus, the voltage gain of these charge pumps can be increased and the output voltages of these circuits are nearly proportional to the number of stages. Four-stage charge pumps, such as the voltage doubler [8] and the PMOS charge pump [11] as illustrated in Figs. 1 and 2, respectively, are two simple high-performance charge pumps that benefit from the bodies of the charge transfer transistors that are connected to their source/drain electrodes.

The output voltage of an N-stage voltage doubler and PMOS charge pumps based on the assumption of zero turn-on resistance of the switching transistors can be expressed as [1]

\[ V_{out} = V_{DD} + N \left( \frac{C}{C + C_{top}} \right) V_{DD} - \frac{NI_o}{2f(C + C_{top})} \]  

Fig. 1. Four-stage voltage doubler circuit.

Fig. 2. Four-stage PMOS charge pump. (a) Circuit diagram. (b) Clock patterns and waveform generators.

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The authors are with the Department of Electrical Engineering, National Chung Hsing University, Taichung 402, Taiwan (e-mail: hclin@dragon.nchu.edu.tw).

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where \( C \) is the pumping capacitance, \( C_{\text{top}} \) is the switch-node parasitic capacitance, \( V_{\text{DD}} \) is the supply voltage, \( I_o \) is the output current, and \( f \) is the clock frequency. However, in low voltage or high output current applications, the on-resistance of switching transistors is increased and may not be neglected due to the low \( V_{gs} \) of switching transistors. By including the on-resistance in (1), the output voltage has been reported as [3]

\[
V_{\text{out}} = V_{\text{DD}} + N \left( \frac{C}{C + C_{\text{top}}} \right) V_{\text{DD}} - \frac{N I_o}{2f(C + C_{\text{top}})} \coth \left( \frac{1}{2f R_{\text{ON}} C} \right)
\]  

(2)

where \( R_{\text{ON}} = L/\mu C_{\text{ox}} W V_{\text{ov}} \) and \( V_{\text{ov}} \) is the overdrive voltage of the switching transistors that varies dynamically. It may be approximated as \( V_{gs} - |V_t| - I_o/2fC \), where \( V_{gs} \) is assumed to be the initial \( V_{gs} \) when the switch is just turned on. Obviously, accurately determining \( V_{ov} \), and thus \( R_{\text{ON}} \), is difficult. The simulated output voltages of a four-stage voltage doubler versus the output current are plotted in Fig. 3. The output voltages are decreased nonlinearly as the output current is high. In this situation, \( R_{\text{ON}} \) is nonlinear [12] and may be over- or underestimated, since the switching transistor tends to work in the triode region, but close to the saturation region. Hence, \( V_{\text{out}} \) cannot be precisely predicted by (1) and (2).

Recently, Hu and Chang [13] proposed an output voltage model by the charge transfer waveforms for charge-pump gain-increase circuits. The authors assumed zero on-resistance of the charge transfer transistors. However, as supply voltages tend lower or loading current trends higher, the development of output voltage models that consider the more accurate on-resistance of transistors becomes important. Moreover, the charge transfer voltage waveforms of various charge pumps are different due to the various gate bias conditions. This implies that (2) cannot accurately estimate the output voltage. In this investigation, output voltage models for the voltage doubler [8] and the PMOS charge pump [11] are formulated based on the voltage waveforms of each pumping stage. The aspect ratio of the switching transistors in both charge pumps can be set to optimize the design.

Similar to the transistor sizes, the power efficiency of charge pumps has become an important issue in recent years due to the low power requirement. Two methods for analyzing the power efficiency are available. One is energy conservation [3] and the other one is charge balance [14]. In the energy-conservation approach, the energy that is provided by the power supply equals the energy that is delivered to the load plus the energy loss. In the charge-balance method, the charge that is transferred from the previous stage is the same as that transferred to the next stage. The power efficiency can be improved either by increasing the output voltage to increase the output power, or by using silicon on insulator (SOI) process to reduce power loss [15]. Much effort has been made in the analysis and optimization of the power efficiency of Dickson charge pump and voltage doubler [14]–[16]. In this paper, the power efficiency models for the voltage doubler and the PMOS charge pumps are derived by considering more parasitic capacitance effects.

The proposed models were verified by simulation and measurements using 0.18 \( \mu \)m CMOS technology. An optimization of the design methodology employing these models for the PMOS charge pump is also presented. A similar design strategy can also be applied to the voltage doubler or the other charge pumps.

The rest of this paper is organized as follows. The output voltage models for the voltage doubler and the proposed PMOS charge pumps are derived in Section II. Section III presents power efficiency models for both charge pumps. Section IV demonstrates the agreements between models, simulation, and measurements. On the basis of the output voltage and the power efficiency models, an optimized design strategy is presented in Section V. Conclusions are finally drawn in Section VI.

II. ANALYTICAL MODELS OF OUTPUT VOLTAGES

Before formulation of the output voltages, the operations of the proposed PMOS charge pump [11] are briefly introduced. The four-stage PMOS charge pump and its clock waveforms are shown in Fig. 2(a) and (b), respectively. The circuit has two pumping branches, the upper branch and the lower branch, which alternately transfer charges to the output \( (V_{\text{out}}) \). In Fig. 2(a), we observed each stage of the proposed PMOS charge pump is composed of a pair of pumping capacitors referred as \( C_1 \) and \( C_{i+1} \), a pair of auxiliary capacitors referred as \( C_{g1} \) and \( C_{g1+4} \), a pair of PMOS switches referred as \( M_1 \) and \( M_{i+4} \), and a pair of auxiliary transistors referred as \( M_{pi} \) and \( M_{pi+1} \). The output stage comprises two cross-connected transistors, \( M_{s1} \) and \( M_{s2} \). The pumping capacitors and the auxiliary capacitors are driven by two nonoverlapping clocks, \( \phi_1 \) and \( \phi_2 \), and two auxiliary clocks, \( \delta_1 \) and \( \delta_2 \), respectively. According to Fig. 2(b), two auxiliary clocks \( \delta_1 \) and \( \delta_2 \) can be easily created from clocks \( \phi_1 \) and \( \phi_2 \). The highest voltages at \( \delta_1 \) and \( \delta_2 \) are close to \( 2V_{\text{DD}} \).

During time \( t_1 \), clocks \( \phi_1 \) and \( \delta_1 \) are low, \( \phi_2 \) is high, and \( \delta_2 \) rises to \( 2V_{\text{DD}} \). Transistors \( M_1 \), \( M_2 \), \( M_3 \), \( M_4 \), and \( M_5 \) are turned on to transfer charges from \( V_{\text{DD}} \) to \( C_1 \), node \( B \) to \( C_1 \), node \( E \) to \( C_6 \), node \( G \) to \( C_6 \), and node \( D \) to \( C_1 \), respectively. Meanwhile, the auxiliary transistors \( M_{p2} \), \( M_{p4} \), \( M_{p5} \), and \( M_{p7} \) are turned on to keep \( M_2 \), \( M_4 \), \( M_5 \), and \( M_7 \) OFF. In a very short
period $t_2$, according to Fig. 2(b), $\phi_2$ drops to zero and $\delta_2$ drops to $V_{DD}$ at the same time, so all transistors $M_i$ are all turned off. The operations in time interval $t_3$ resemble those in $t_1$ with the roles of devices interchanged. The operation of time interval $t_4$ is identical to that of time interval $t_2$.

To derive the output voltage models, the PMOS charge pump shown in Fig. 2 is divided into the input stage, inner stages, and the output stage according to the charge transfer behaviors. The input stage is from $V_{DD}$ to node A/E, and the first to third inner stages are from A/E to B/F, B/F to C/G, and C/G to D/H, respectively. The output stage comprises two cross-connected transistors, $M_o1$ and $M_o2$. The derivation is based on the following assumptions.

1) Compared with the pumping capacitance, the small parasitic capacitance at each pumping node can be neglected.
2) Only one charge transfer branch, the upper or lower one, is considered in derivation of charge transfer characteristics.

### A. Voltage Model of Input Stage for the PMOS Charge Pump

The node voltage waveforms of transistor $M_1$ shown in Fig. 2(a) are shown in Fig. 4(a). Notably, in Fig. 2(b), $t_2$ and $t_4$ are much shorter than $t_1$ and $t_3$, so $t_1$ and $t_3$ are assumed to be equal to one half of one period ($T/2$) in the following derivation. At time interval $[nT, nT + (T/2)]$, clocks $\phi_1$ and $\delta_1$ are low, and the charges are transferred from $V_{DD}$ to $C_1$ and the drain voltage $V_d$ of transistor $M_1$ is increased from $V_{DD} - \Delta V$ to $V_{DD}$, where $\Delta V = I_o/2fC(C = C_1)$. At the same time, the voltages $V_g$ and $V_s$ are held at constant values of $-\Delta V$ and $V_{DD}$, respectively.

The current that flows through transistor $M_1$ and the pumping capacitor $C_1$ can be expressed as follows using the equation for the PMOS transistor in the triode region:

$$I = k_{p3} \left\{ [(V_s - V_g) - V_{t3}] (V_s - V_d) - \frac{1}{2} (V_s - V_d)^2 \right\} $$

where $k_{p3} = \mu_p C_{ox} W/L$ and $V_{t3}$ are the process parameters including the $W/L$ factor and the absolute value of the threshold voltage of the high-voltage PMOS transistor, respectively.

Substituting $V_s = V_{DD}$ and $V_d = -\Delta V$ into (3) yields

$$CdV_d \frac{dt}{dt} = \frac{1}{2} k_{p3} (V_{DD} - V_d) (V_{DD} + V_d + 2\Delta V - 2V_{t3}) $$

Integrating (4) with respect to $t$ and varying $V_d$ from $V_{DD} - \Delta V$ to $V_d$ yields the output voltage of the input stage of the PMOS charge pump as follows:

$$V_d = -V_{DD} + 2V_{t3} - 2\Delta V + \frac{2(V_{DD} + \Delta V - V_{t3})}{1 + |\Delta V/(2V_{DD} + \Delta V - 2V_{t3})|e^{-(k_{p3}/C)(V_{DD} + \Delta V - V_{t3})}}.$$
B. Voltage Model of Inner Stages for the PMOS Charge Pump

The corresponding node voltage waveforms of transistor $M_2$ shown in Fig. 2(a) are shown in Fig. 4(b). In the time interval $[nT + (T/2), (n+1)T)$, $\phi_2$ and $\delta_2$ are low, and the charges stored in $C_1$ are transferred to $C_2$ in a very short period. The voltage $V_d$ of transistor $M_2$ is increased from $V_{DD} - 2\Delta V$ to $V_{DD} - \Delta V$ by charging, and the source voltage $V_s$ is reduced by discharging from $V_{DD}$ to $V_{DD} - \Delta V$. Simultaneously, the voltage $V_g$ falls to $-2\Delta V$ because the clock $\delta_2$ switches to low. From Fig. 4(b), we conclude that since $V_s + V_d = 2V_{DD} - 2\Delta V$, the voltage $V_s$ can be expressed as a function of $V_d$ as

$$V_s = 2V_{DD} - 2\Delta V - V_d.$$  \hfill (6)

Substituting $V_g = -2\Delta V$ and (6) into (3) yields

$$C_dV_d \frac{dt}{dt} = 2k_{p3}(V_{DD} - \Delta V - V_d)(V_{DD} + \Delta V - V_{t3}).$$  \hfill (7)

Integrating (7) with respect to $t$ and varying $V_d$ from $V_{DD} - 2\Delta V$ to $V_d$ yields the output voltage $V_d$ of the inner stage of the PMOS charge pump as follows:

$$V_d = V_{DD} - \Delta V(1 + e^{-2(k_{p3}/C)(V_{DD} + \Delta V - V_{t3})}).$$  \hfill (8)

C. Voltage Model of Output Stage for the PMOS Charge Pump

The output stage of the proposed charge pump comprises two cross-connected transistors, $M_{o1}$ and $M_{o2}$, to output capacitor $C_L$ alternately. The corresponding node voltage waveforms of transistor $M_{o1}$ shown in Fig. 2(a) are shown in Fig. 4(c). At time $t = nT$, $\phi_2$ is high, transistor $M_{o1}$ is turned on and the charge stored in $C_1$ is transferred to $C_L$. If the output capacitance $C_L$ is large enough, the output voltage is held at $V_{DD} - \Delta V$. Then, $V_d$ may drop to $V_{DD} - 2\Delta V$ at the end of time $t = (n+1)T$ by clock $\phi_2$ switching to low. As plotted in Fig. 4(c), the source voltage $V_s$ is reduced from $V_{DD}$ to $V_{DD} - 2\Delta V$ by discharging, and the gate voltage $V_g$ falls to $-\Delta V$ at the beginning of time $t = nT$. It then rises to $0$ V by charging before $t = nT + (T/2)$. Since $V_s + V_d = 2V_{DD} - 2\Delta V$ and $V_d - V_g \cong V_{DD} - \Delta V$, both voltages $V_g$ and $V_s$ can be expressed in terms of $V_d$ as follows:

$$V_g = V_d - V_{DD} + \Delta V$$ \hfill (9)

$$V_s = 2V_{DD} - 2\Delta V - V_d.$$ \hfill (10)

Substituting (9) and (10) into (3) with $k_{p3}$ and $V_{t3}$ replaced by $k_p$ and $V_{tP}$, respectively, gives

$$C_dV_d \frac{dt}{dt} = 2k_p(V_{DD} - \Delta V - V_d)(2V_{DD} - 2\Delta V - V_d - V_{tP}).$$ \hfill (11)

Integrating (11) with respect to $t$ and varying $V_d$ from $V_{DD} - 2\Delta V$ to $V_d$ yields the drain voltage $V_d$ of the output stage of the PMOS charge pump as follows:

$$V_d = (2V_{DD} - 2\Delta V - V_{tP}) - \frac{V_{DD} - \Delta V - V_{tP}}{1 - [\Delta V/(V_{DD} - V_{tP})]e^{-2(V_{DD} - \Delta V - V_{tP})(k_p/C)t}}.$$ \hfill (12)

where $k_p = \mu_p C_{ox} W/L$ and $V_{tP}$ are the process parameters including the $W/L$ factor and the threshold voltage of the low-voltage PMOS transistor, respectively.

An $N$-stage proposed PMOS charge pump has one input stage, one output stage, and $(N-1)$ inner stages. Adding (5), (12), and $(N-1) \times (8)$ yields a complete expression for the output voltage of the PMOS charge pump as follows:

$$V_{outp} = NV_{DD} + 2V_{tP} - V_{tP} - (N + 3)\Delta V$$

$$- (N - 1)\Delta V e^{-2(k_{p3}/C)(V_{DD} + \Delta V - V_{t3})}$$

$$+ \frac{2(V_{DD} + \Delta V - V_{t3})}{1 + \left[(2(V_{DD} + \Delta V - V_{t3}))(e^{-2(k_{p3}/C)(V_{DD} + \Delta V - V_{t3})}) - 1\right]}$$

$$- \frac{V_{DD} - \Delta V - V_{tP}}{1 - \left[(2V_{DD} - \Delta V - V_{tP})e^{-2(V_{DD} - \Delta V - V_{tP})(k_{p3}/C)t}\right]}.$$ \hfill (13)

For the special case, if $t = T/2$ is very long, then all of the exponential terms approach zero. Substituting $\Delta V = V_{tP}/2$ into (13) allows $V_{outp}$ to be simplified to $V_{outp} = (N + 1)V_{DD} - \frac{NV_{tP}}{2}$, which is the same as (1) with $C_{tP} = 0$.

With the similar procedures given before, the voltage models of the input stage, inner stage, and the output stage of voltage doublers are also derived in the Appendix. The output voltage model of an $N$-stage voltage doublers can be formulated as

$$V_{outd} = \frac{(2N + \frac{5}{3})V_{DD} - (2N + 2 \frac{5}{3})\Delta V - NV_{tP} - \frac{2}{3}V_{tn}}{(N - 1)(V_{DD} - \Delta V - V_{tP})}$$

$$- \frac{(2/3)(V_{DD} - \Delta V - V_{tP})}{1 - \left[(3\Delta V/(2(V_{DD} + \Delta V - V_{tP})))e^{-2(V_{DD} + \Delta V - V_{tP})(k_{p}/C)t}\right]}$$

$$- \frac{V_{DD} - \Delta V - V_{tP}}{1 - \left[(V_{DD} - V_{tP})e^{-2(V_{DD} - \Delta V - V_{tP})(k_{p}/C)t}\right]}.$$ \hfill (14)

III. COMPACT MODELS OF POWER EFFICIENCIES

The power efficiency of a charge pump can be defined as the output power $P_o$ divided by the input power $P_i$ as

$$\eta = \frac{P_o}{P_i} = \frac{V_{out}I_o}{V_{dd}I_{dd}},$$ \hfill (15)

where $I_o$ is the output current and $I_{dd}$ is the current drawn from the power supply. Here, we assume that transistors are ideal switches and use the charge balance method to analyze the power efficiency of the voltage doubler and the PMOS charge pump. Ideal switches are assumed because, from a design perspective, the power efficiency must be maximal when the charge transfer transistors have almost zero on-resistance. Notably, the output voltage models that are derived in Section II are used to determine the transistor sizes to prevent overdesign.

Fig. 5 shows the charges distribution of the four-stage PMOS charge pump at time intervals $t_1$ and $t_2$. The charges distribution at $t_3$ and $t_4$ are similar to those of $t_1$ and $t_2$, respectively. The transistor symbols with black lines indicate that the transistors are ON, while those with gray lines mean that the transistors are OFF. The charges can be transferred only if the transistors are ON. $\Delta Q$ indicates the charges transferred to the pumping capacitor.
by power supply or clocks during \( t_1 \). \( \Delta Q_{\text{bot}} \) and \( \Delta Q_{\text{top}} \) labeled in Fig. 5(a) indicate the charge losses because of the bottom-plate and top-plate parasitic capacitances \( (C_{\text{bot}} \text{ and } C_{\text{top}}) \) of the pumping capacitors, respectively. Here, \( C_L \) is assumed to be equal to \( C_t + C_{t+4} \), so \( 2\Delta Q_{\text{top}} \) is the charge losses due to the top-plate parasitic capacitance at the output node. Similarly, the charge transferred to the auxiliary capacitor \( (C_g) \) is \( \Delta Q_g \), and the charge losses due to the bottom-plate and the top-plate parasitic capacitances \( (C_{gb} \text{ and } C_{gt}) \) of the auxiliary capacitor are \( \Delta Q_{gb} \) and \( \Delta Q_{gt} \), respectively. All of the switches, except some auxiliary transistors, are OFF in \( t_2 \), as revealed in Fig. 5(b). Hence, the charges provided by the power supply and the clocks from \( t_1 \) to \( t_4 \) can be written as

\[
\Delta Q_{i1} = \Delta Q_{i3} = 5\Delta Q + 4\Delta Q_{\text{bot}} + 10\Delta Q_{\text{top}} + 4\Delta Q_g
\]
\[
+ 4\Delta Q_{gb} + 4\Delta Q_{gt}
\]
\[
\Delta Q_{i2} = \Delta Q_{i4} = 4\Delta Q_g + 4\Delta Q_{gb} + 4\Delta Q_{gt}.
\]

(16)

(17)

The total charges provided by the power supply and the clocks in one clock cycle are \( \sum \Delta Q_{i1} \), where \( i = 1, 4 \)

\[
\Delta Q_t = 10\Delta Q + 8\Delta Q_{\text{bot}} + 20\Delta Q_{\text{top}} + 16\Delta Q_g
\]
\[
+ 16\Delta Q_{gb} + 16\Delta Q_{gt}.
\]

(18)

Since the charge pump has two branches, charges transfer to the output occurs twice in one clock cycle \( (T) \). The total current consumption can be obtained from (18) by converting charge into current using a multiplication factor of \( 1/2 \) as

\[
I_{V_{\text{DD}}} = 5I_o + 4I_{\text{bot}} + 10I_{\text{top}} + 8I_g + 8I_{gb} + 8I_{gt}.
\]

(19)

This expression can be extended to \( N \) stages as follows:

\[
I_{V_{\text{DD}}} = (N + 1)I_o + N I_{\text{bot}} + 2(N + 1)I_{\text{top}} + 2NI_g
\]
\[
+ 2NI_{gb} + 2NI_{gt}.
\]

(20)

The currents that charge or discharge the bottom-plate and the top-plate parasitic capacitors have the following relationships \( [15] \):

\[
I_{\text{bot}} = 2C_{\text{bot}}V_{\text{DD}}f
\]
\[
I_{\text{top}} = \frac{C_{\text{top}}}{C + C_{\text{top}}} I_o
\]

(21)

(22)

where \( C_{\text{bot}} \) denotes the bottom-plate parasitic capacitance of \( C_t \). Similarly, \( I_{gb} = 2C_{gb}V_{\text{DD}}f \) and \( I_{gt} = I_gC_{gt}/(C_g + C_{gt}) \) can be derived for the bottom-plate and the top-plate parasitic capacitances of the auxiliary capacitors \( C_g \), respectively, and \( I_g \) indicates the current that charges the auxiliary capacitor.

Substituting (21), (22), \( I_{gb} \), and \( I_{gt} \) into (20), the power efficiency \( \eta \) can be expressed as (23), shown at the bottom of this page.

Since the bottom-plate and the top-plate parasitic capacitances \( C_{\text{bot}} \) and \( C_{\text{top}} \) are nearly proportional to the pumping capacitance \( C \), the relations of \( C_{\text{bot}} = \alpha C \) and \( C_{\text{top}} = \beta C \) are adopted. Similarly, \( C_{gb} \) and \( C_{gt} \) are also fractions of the auxiliary capacitance \( C_g \), so that \( C_{gb} = \alpha_g C_g \) and \( C_{gt} = \beta_g C_g \). Moreover, since the pumping capacitance is more than an order of magnitude larger than the auxiliary capacitance, \( C_g = \gamma C \) can be assumed, and thus, \( I_g \equiv \gamma I_o \). Therefore, (23) can be recast as (24), shown at the bottom of this page.

\[
\eta = \frac{V_{\text{DD}} + [1/(1 + \beta)](V_{\text{outp}} - V_{\text{DD}})}{V_{\text{DD}} [(N + 1) + (2N C_{\text{bot}} V_{\text{DD}} f/I_o) + (2(N + 1)C_{\text{top}}/(C + C_{\text{top}}))] + 2N(I_g/I_o) + 4N(C_{gb} V_{\text{DD}} f/I_o) + 2N[I_g C_{gt}/(C_g + C_{gt})I_o]]}
\]

(23)

\[
\eta = \frac{V_{\text{DD}} + [1/(1 + \beta)](V_{\text{outp}} - V_{\text{DD}})}{V_{\text{DD}} [(N + 1) + (2N \alpha CV_{\text{DD}} f/I_o) + (2(N + 1)\beta/(1 + \beta))] + 2N\gamma + 4N(\alpha_g C_g V_{\text{DD}} f/I_o) + 2N[\gamma \beta_g/(1 + \beta_g)]].
\]

(24)
With the similar procedure given before, the power efficiency for the voltage doubler can also be derived as

$$\eta_d = \frac{V_{DD} + \left[ \frac{1}{1 + \beta} \right](V_{outd} - V_{DD})}{V_{DD} \left[ \frac{(N+1)}{2} + \left\{ \frac{2N\alpha CV_{DD}f}{I_o} \right\} + \left\{ \frac{2(N+1)\beta}{1 + \beta} \right\} \right]}$$

(25)

IV. SIMULATION AND MEASUREMENT RESULTS

To verify the accuracy of the proposed output voltage models, the four-stage voltage doubler and the proposed PMOS charge pumps were designed using the 0.18 µm CMOS technology with threshold voltages of 0.44, −0.495, and −0.73 V for NMOS, PMOS, and high-voltage PMOS transistor, respectively. Likewise, the process parameters $k_n$, $k_p$, and $k_{p3}$ extracted from SPICE simulations are 3.362, 0.998, and 0.872 mA/V², respectively. Both charge pumps used the same transistor sizes, clock frequency, and pumping capacitance for comparison. The pumping and output capacitances of 5 and 10 pF, respectively, were chosen for both pumps, and the auxiliary capacitors in the PMOS charge pump were 0.5 pF.

The nominal conditions of the following figures are a loading current of 50 µA, a supply voltage of 1.8 V, and a clock frequency of 10 MHz, except where otherwise specified. Figs. 6 and 7 compare the simulated output voltages, voltages obtained using the proposed voltage model, and the voltage obtained from (2) versus output current at various supply voltages for the PMOS charge pump and the voltage doubler, respectively. The proposed voltage model and (2) are mostly consistent with the simulated results at low output currents, at which the output voltages linearly decrease as the output current increases. However, for a higher loading current and a lower supply voltage, since the on-resistance of the switching device is nonlinear, the output voltages decline nonlinearly. The proposed model takes into account the accurate on-resistance, such that the errors between the simulated results and the proposed models are always less than 5%.

In Fig. 8, the measured output voltages agree with the simulated results and the results of the model for the four-stage PMOS charge pump. The differences between the measurements and the results of the model are less than 8%. Fig. 9 shows the agreement between the measurements, simulated results, and the results of the voltage model for the four-stage PMOS charge pump with various frequencies. If the parasitic capacitances at each pumping nodes are considered in (13), then the errors between the voltage models and the measurements are expected to be reduced.

Fig. 10 plots the theoretical and simulated efficiencies of both four-stage charge pumps versus frequency with a pumping capacitance of 30 pF and a loading current of 200 µA. The power efficiency is maximal at 8 MHz. The parameters $\alpha$ and $\beta$ for the voltage doubler and the PMOS charge pump, based on the extracted postlayout parasitic parameters, are 0.1 and 0.04, and 0.1 and 0.012, respectively. The parameters $\alpha_g$ and $\beta_g$ for the proposed charge pump are 0.1 and 0.08, respectively. From (24)
and (25), the voltage doubler has a higher theoretical efficiency. However, since the on-resistance of the switching devices of the PMOS charge pump is smaller, the power efficiency of the proposed charge pump is slightly higher than that of voltage doubler. Fig. 11 plots the power efficiencies of both four-stage charge pumps as functions of output load with a pumping capacitance of 30 pF. The maximum simulated efficiencies for the voltage doubler and the PMOS charge pump are 54.5% and 57.5%, respectively.

Fig. 12 plots the measured power efficiency as a function of frequency under a load of 50 μA. The measured results agree well with the simulation and the model. The measured maximum power efficiency is about 45% at 8 MHz. Fig. 13 plots the theoretical and measured power efficiencies of the four-stage PMOS charge pump as functions of output current for 12 and 10 MHz under the nominal condition. Since 5 pF pumping capacitors were used to reduce the cost of chip fabrication, the power efficiencies are lower than those shown in Fig. 11. The
maximum measured efficiency was around 45% at a loading current of 60 $\mu$A. Solid symbols indicate the errors of the power efficiency between the model and measurements.

V. DESIGN METHODOLOGY

In the design of charge pump circuits, maximum power efficiency is desired. The output voltages in (13) and (14) should approach that given by (1). To satisfy this requirement, the sizes of the transistors in the charge pump must be sufficiently large without overdesign. The exponential terms multiplied by their coefficients can be reasonably set to be 0.01 for $f = 10$ MHz and $C = 5$ pF. The aspect ratios ($W/L$) of the PMOS charge pump and the voltage doubler are shown in Fig. 14(a) and (b), respectively. The $W/L$ ratios of the voltage doubler increased exponentially with the output current. However, those of the PMOS charge pump are not varied significantly, except the output stage, which is the same as the voltage doubler.

If the exponential terms in (13) approach to zero, (24) can be rewritten as

$$\eta_{V_{DD}} = A - B\Delta V + E/\Delta V$$

where $\Delta V = I_o/2fC$ represents the optimized factor. Thus, the higher loading current leads to the higher product of pumping capacitance and clock frequency. The other parameters are

$$A = V_{DD} + \frac{N}{1 + \beta} V_{DD}$$

$$B = \frac{N}{1 + \beta}$$

$$D = N(2\gamma + 1) + 1 + \frac{2(N + 1)\beta}{1 + \beta} + 2N\gamma\beta g$$

$$E = N(\alpha + 2\alpha g\gamma)V_{DD}.$$  

These parameters can be assumed to be constant because $V_{DD}$ is usually determined by the system. The others are parasitic effects, except for the number of stages $N$, which is an integer and can be determined later.

The optimized factor $\Delta V$ can be obtained by taking the derivative of (26) with respect to $\Delta V$ and setting the derivative to zero. The resulting $\Delta V$ can be expressed as

$$\Delta V = -\frac{E}{D} \pm \sqrt{\frac{E^2}{D^2} + \frac{AE}{BD}}.$$  

Since $\Delta V$ must be positive, the positive sign in (31) must be selected.

According to Fig. 15, the optimized factor $\Delta V$ increased with the supply voltage for the PMOS charge pump. The required pumping capacitor and frequency for a given output load can be selected after the optimized factor is determined. For example, substituting an optimized factor of about 0.441 in Fig. 15 into (26) for $V_{DD} = 1.8$ V and $N = 4$ yields a maximum power efficiency $\eta$ of 46%, which agrees with the peak value in Fig. 13. Fig. 15 also indicates a small variation of the optimized factor.
with the number of stages. Interestingly, the optimized factor varies only slightly with the numbers of stages for the given parameters. Therefore, if the optimized factor is obtained by setting $N = 4$ for $N$-stage charge pumps, then the discrepancy in the maximum power efficiency is always less than 0.2% for $V_{DD} = 1.8$ V, as shown in Fig. 16.

To design the optimized power-efficient PMOS charge pump, the optimized factor $\Delta V = I_o/2f C$ was first calculated using (31) for a given $V_{DD}$ with $N = 4$. For example, $\Delta V = 0.441$ for $V_{DD} = 1.8$ V in Fig. 15. Next, according to the required output current, $f C$ is determined, and the transistor sizes are then determined using (13). Finally, the number of stages $N$ is obtained by using (1) for the required $V_{out}$. However, $N$ is usually computed as a real number. Since $N$ must be an integer, one of the two integers that are just higher and lower than the computed $N$ should be the optimized number of stages. For instance, if $V_{out} = 6$ V and the loading current is 50 $\mu$A, the sizes of the transistors in the PMOS charge pump are 10, as shown in Fig. 14(a), then $N = 3.13$ is determined. The possible choices are $N = 3$ and $N = 4$. Substituting these two integers into (1) yields two $\Delta V$ values, which are input into (26) to find the maximum power efficiency. In this example, $\Delta V = 0.3832$ and $\Delta V = 0.7374$ for $N = 3$ and $N = 4$, respectively. The corresponding values of $\eta$ are 51.84% and 46.62%. Therefore, $N = 3$ is adopted and the pumping capacitance is 6.524 pF for a loading current of 50 $\mu$A and a clock frequency of 10 MHz.

VI. CONCLUSION

Analytical output voltage models for the voltage doubler and the PMOS charge pump were formulated using dynamic charge-transferred waveforms. Since the on-resistance of the switching devices can be precisely predicted, the proposed models are more accurate than any others. The accuracy of the voltage models was verified by simulation for both pumps and measurements for the PMOS charge pump using the 0.18 $\mu$m CMOS technology. The discrepancies are less than 5% and 8% in comparison to simulation and measurements, respectively. Note that the output voltage expressions can be used to explain why the PMOS charge pump can provide higher output current without increasing the transistor sizes significantly.

Compact models of power efficiency for both charge pumps were derived by including parasitic capacitance effects. The models were also verified by simulation and measurements made by using the 0.18 $\mu$m CMOS technology. The errors between the model and measurements of the four-stage PMOS charge pump are less than 5%. Finally, a design methodology is presented, in which the output voltage model is applied to determine the transistor sizes, and the optimized factor is used to determine the pumping capacitance, the clock frequency, and the number of stages that maximize power efficiency.

APPENDIX

The similar formulation procedure discussed in Section II for the output voltages of the voltage doubler is given here for references.

A. Voltage Model of Input Stage for Voltage Doubler

The corresponding node waveforms of transistor $N_2$ shown in Fig. 1 are plotted in Fig. 17(a). When clock $\phi_1$ is low in time interval $[nT, nT + (T/2)]$, the voltages $V_s$ and $V_g$ of transistor $N_2$ are increased from $V_{DD} - \Delta V$ to $V_{DD}$ by charging and decreased by discharging from $2V_{DD}$ to $2V_{DD} - \Delta V$, respectively. The current that flows through transistor $N_2$ and the pumping capacitor $C_I$ is given by the equation for the NMOS transistor in the triode region

$$I = k_n \left\{ [(V_g - V_s) - V_{tn}] (V_d - V_s) - \frac{1}{2} (V_d - V_s)^2 \right\}$$

(A1)

where $k_n = \mu_n C_{ox} W/L$ and $V_{tn}$ are the process parameter with $W/L$ factor and the threshold voltage of the NMOS transistor, respectively. From Fig. 17(a), we conclude that since $V_s + V_g = 3V_{DD} - \Delta V$, the voltage $V_g$ can be expressed as a function of $V_s$ as

$$V_g = 3V_{DD} - \Delta V - V_s.$$  (A2)

Substituting (A2) and $V_d = V_{DD}$ into (A1) yields

$$\frac{C I dV_s}{dt} = \frac{3}{2} k_n (V_{DD} - V_s) \left( \frac{5}{3} V_{DD} - V_s - \frac{2}{3} V_{tn} - \frac{2}{3} \Delta V \right).$$

(A3)

Integrating (A3) with respect to $t$ and varying $V_s$ from $V_{DD} - \Delta V$ to $V_s$ yields the output voltage $V_s$ of the input stage of the voltage doubler as follows:

$$V_s = \frac{5}{3} V_{DD} - \frac{2}{3} V_{tn} - \frac{2}{3} \Delta V$$

$$- \frac{(2/3)}{1 - 3\Delta V/(2(V_{DD} + (\Delta V/2) - V_{tn}))} e^{-(k_n C_I)(V_{DD} - \Delta V - V_{tn})}.$$  (A4)

B. Voltage Model of Inner Stages for Voltage Doubler

Each inner stage of the voltage doubler consists of two NMOS transistors and two PMOS transistors. The charge transfer

Fig. 16. Maximum power efficiency versus stage number nearly overlapped by using the actual optimized factor and the optimized factor of $N = 4$ with $C = 5$ pF.
through the PMOS transistor of the voltage doubler is analyzed first, and the NMOS transistor is considered as an ideal switch. The reverse situation will be given later. The corresponding node voltage waveforms of transistor $P_2$ shown in Fig. I are shown in Fig. 17(b). In time interval $[nT + (T/2), (n+1)T]$, $\phi_1$ is high, transistor $P_3$ is turned on, and the charges stored in $C_2$ are transferred to $C_4$. As plotted in Fig. 17(b), the voltage $V_s$ of transistor $P_2$ is decreased by discharging from $V_{DD}$ to $V_{DD} - \Delta V$, and $V_d$ is increased from $2V_{DD} - 2\Delta V$ to $2V_{DD} - \Delta V$ by charging. Meanwhile, the voltage $V_g$ falls to $-\Delta V$ at $t = nT + (T/2)$, and then charges to 0 V before $t = (n+1)T$. From Fig. 17(b), we conclude that since $V_s + V_d = 2V_{DD} - 2\Delta V$ and $V_d - V_g = V_{DD} - \Delta V$, both voltages $V_g$ and $V_s$ can be expressed as functions of $V_d$ as follows:

\[ V_g = V_d - V_{DD} + \Delta V \quad \text{(A5)} \]

\[ V_s = 2V_{DD} - 2\Delta V - V_d. \quad \text{(A6)} \]

Substituting (A5) and (A6) into (3) with $k_{p3}$ and $V_{th3}$ replaced by $k_p$ and $V_{th}$, respectively, gives

\[ \frac{CdV_d}{dt} = 2k_p(V_{DD} - \Delta V - V_d)(2V_{DD} - 2\Delta V - V_d - V_{th}). \quad \text{(A7)} \]

Integrating (A7) with respect to $t$ and varying $V_d$ from $V_{DD} - 2\Delta V$ to $V_d$ yields the output voltage $V_d$ of the PMOS transistor of the inner stage for the voltage doubler as follows:

\[ V_d = \frac{(2V_{DD} - 2\Delta V - V_{th})}{1 - \frac{\Delta V}{V_{DD} - V_{th}}} e^{-2(V_{DD} - \Delta V - V_{th})(k_p/C_d)t}. \quad \text{(A8)} \]

If the operation of the NMOS transistor is considered, when $\phi_1$ is high and $\phi_2$ switches to low in Fig. I, transistor $N_4$ is turned on. Charge is transferred from $C_2$ to $C_1$. The voltages $V_d$ and $V_g$ of transistor $N_4$ are discharged from $V_{DD}$ to $V_{DD} - \Delta V$ and $2V_{DD} - \Delta V$ to $2V_{DD} - 2\Delta V$, respectively, and the voltage $V_s$ is increased by charging from $V_{DD} - 2\Delta V$ to $V_{DD} - \Delta V$. The corresponding charge transfer waveforms are shown in Fig. 17(c). From Fig. 17(c), we conclude that since $V_s + V_d = 2V_{DD} - 2\Delta V$ and $V_s + V_g = 3V_{DD} - 3\Delta V$, the voltages $V_d$ and $V_g$ can be expressed as functions of $V_s$ as follows:

\[ V_g = 3V_{DD} - V_s - 3\Delta V \quad \text{(A9)} \]

\[ V_d = 2V_{DD} - 2\Delta V - V_s. \quad \text{(A10)} \]

Substituting (A9) and (A10) into (A1) yields

\[ \frac{CdV_s}{dt} = 2k_n(V_{DD} - \Delta V - V_s)(2V_{DD} - 2\Delta V - V_s - V_{th}). \quad \text{(A11)} \]
Integrating (A11) with respect to \( t \), then varying \( V_s \) from \( V_{DD} - 2\Delta V \) to \( V_s \), yields the source voltage \( V_s \) of the NMOS transistor of the inner stage of the voltage doubler

\[
V_s = (2V_{DD} - 2\Delta V - V_{tn}) - \frac{V_{DD} - \Delta V - V_{tn}}{1 - \frac{V_{DD} - \Delta V - V_{tn}}{V_{DD} - V_{tn}} - \frac{\Delta V}{V_{DD} - V_{tn}}} [e^{-2(V_{DD} - \Delta V - V_{tn})(k_n/C)t}].
\]

(A12)

The differences between (A8) and (A12) are the process parameters and the threshold voltages. The equivalent process parameter \( k \) of transistors \( P_2 \) and \( N_2 \) connected in series may be equivalent to \( k_n k_p / (k_n + k_p) \). The absolute values of the threshold voltage of the PMOS and the NMOS transistors in the inner stages are assumed to be equal to simplify the formula. Substituting \( k \) into (A8), the output voltage \( V_{inner} \) of the inner stages for voltage doubler can be expressed as

\[
V_{inner} = (2V_{DD} - 2\Delta V - V_{tp}) - \frac{V_{DD} - \Delta V - V_{tp}}{1 - \frac{V_{DD} - \Delta V - V_{tp}}{V_{DD} - V_{tp}} [e^{-2(V_{DD} - \Delta V - V_{tp})(k/C)t}].
\]

(A13)

C. Voltage Model of Output Stage for Voltage Doubler

It should be noticed that the output stage of the voltage doubler is the same as that of the PMOS charge pump. An \( N \)-stage voltage doubler has one input stage, one output stage, and \( (N-1) \) inner stages. Adding (A4), \( (N-1) \times (A13) \), and (12) yields a complete expression for the output voltage of the voltage doubler as follows:

\[
V_{outd} = \left(2N + 5 \frac{2}{3}\right) V_{DD} - \left(2N + \frac{2}{3}\right) \Delta V - NV_{tp} - \frac{2}{3} V_{tn} - \frac{(N-1)(V_{DD} - \Delta V - V_{tp})}{1 - \frac{\Delta V}{V_{DD} - V_{tp}} [e^{-2(V_{DD} - \Delta V - V_{tp})(k/C)t}]} + \frac{(2/3)(V_{DD} - \Delta V - V_{tn})}{1 - \frac{3\Delta V/2}{V_{DD} + (\Delta V/2 - V_{tn})} [e^{-(V_{DD} - \Delta V - V_{tn})(k_n/C)t}]} - \frac{V_{DD} - \Delta V - V_{tp}}{1 - \frac{\Delta V}{V_{DD} - V_{tp}} [e^{-2(V_{DD} - \Delta V - V_{tp})(k_p/C)t}]}.
\]

(A14)

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Chien-Pin Hsu was born in Taiwan. He received the B.S. degree in industrial education from the National Taiwan Normal University, Taipei, Taiwan, in 1986, and the M.S. degree in electrical engineering from the National Tsing Hua University, Hsinchu, Taiwan, in 1992. He is currently working toward the Ph.D. degree in the Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan.

His current research includes the charge pump circuit design for flash memories.

Hongchin Lin received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1986, and the M.S. and Ph.D. degrees from the University of Maryland, College Park, in 1989 and 1992, respectively.

From 1992 to 1995, he was a Senior Device Engineer with the Integrated Technology Division, Advanced Micro Devices, Sunnyvale, CA. In 1995, he joined the Department of Electrical Engineering, National Chung Hsing University, Taichung, Taiwan. He has been a Full Professor since 2003. His current research interests include nonvolatile memory devices and circuits, very-large-scale integration implementation of digital communication systems, design of high-speed circuits, and systems-in-package technology. He has authored or coauthored more than 70 technical papers, including more than 20 Science Citation Index journal papers. He also holds more than 30 patents worldwide.