Chapter 4
Wafer Manufacturing
and Epitaxy Growing

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Objectives

• Give two reasons why silicon dominate
• List at least two wafer orientations
• List the basic steps from sand to wafer
• Describe the CZ and FZ methods
• Explain the purpose of epitaxial silicon
• Describe the epi-silicon deposition process.
Crystal Structures

- Amorphous
  - No repeated structure at all
- Polycrystalline
  - Some repeated structures
- Single crystal
  - One repeated structure

Amorphous Structure
Polycrystalline Structure

Grain Boundary
Grain

Single Crystal Structure
Why Silicon?

- Abundant, cheap
- Silicon dioxide is very stable, strong dielectric, and it is easy to grow in thermal process.
- Large band gap, wide operation temperature range.

<table>
<thead>
<tr>
<th>Name</th>
<th>Silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbal</td>
<td>Si</td>
</tr>
<tr>
<td>Atomic number</td>
<td>14</td>
</tr>
<tr>
<td>Atomic weight</td>
<td>28.0855</td>
</tr>
<tr>
<td>Discoverer</td>
<td>Jöns Jacob Berzelius</td>
</tr>
<tr>
<td>Discovered at</td>
<td>Sweden</td>
</tr>
<tr>
<td>Discovery date</td>
<td>1824</td>
</tr>
<tr>
<td>Origin of name</td>
<td>From the Latin word “silicus” meaning &quot;flint&quot;</td>
</tr>
<tr>
<td>Bond length in single crystal Si</td>
<td>2.352 Å</td>
</tr>
<tr>
<td>Density of solid</td>
<td>2.33 g/cm³</td>
</tr>
<tr>
<td>Molar volume</td>
<td>12.06 cm³</td>
</tr>
<tr>
<td>Velocity of sound</td>
<td>2200 m/sec</td>
</tr>
<tr>
<td>Electrical resistivity</td>
<td>100,000 μΩ-cm</td>
</tr>
<tr>
<td>Reflectivity</td>
<td>28%</td>
</tr>
<tr>
<td>Melting point</td>
<td>1414 °C</td>
</tr>
<tr>
<td>Boiling point</td>
<td>2900 °C</td>
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</table>

Source: [http://www.shef.ac.uk/chemistry/web-elements/nofr-key/Si.html](http://www.shef.ac.uk/chemistry/web-elements/nofr-key/Si.html)
Unit Cell of Single Crystal Silicon

Crystal Orientations: <100>
Crystal Orientations: $<111>$

Crystal Orientations: $<110>$
<100> Orientation Plane

Basic lattice cell

Atom

<111> Orientation Plane

Basic lattice cell

Silicon atom
Illustration of the Defects

- Impurity on substitutional site
- Silicon Atom
- Silicon Interstitial
- Vacancy or Schottky Defect
- Impurity in Interstitial Site
- Frenkel Defect

Dislocation Defects
From Sand to Wafer

- Quartz sand: silicon dioxide
- Sand to metallic grade silicon (MGS)
- React MGS powder with HCl to form TCS
- Purify TCS by vaporization and condensation
- React TCS to H$_2$ to form polysilicon (EGS)
- Melt EGS and pull single crystal ingot

From Crystal to Wafer

- Cut end, polish side, and make notch or flat
- Saw ingot into wafers
- Edge rounding, lap, wet etch, and CMP
- Laser scribe
- Epitaxy deposition
From Sand to Silicon

Heat (2000 °C)

\[ \text{SiO}_2 + \text{C} \rightarrow \text{Si} + \text{CO}_2 \]

Sand + Carbon = MGS + Carbon Dioxide

Silicon Purification I

\[ \text{Si} + \text{HCl} \rightarrow \text{TCS} \]

Condenser → Filters → Purifier → Pure TCS with 99.9999999%
Polysilicon Deposition, EGS

Heat (1100 °C)

\[ \text{SiHCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3\text{HCl} \]

TCS + Hydrogen → EGS + Hydrochloride

Silicon Purification II

Liquid TCS → \( \text{H}_2 \) gas and TCS → EGS

Process Chamber

Carrier gas bubbles
Electronic Grade Silicon

Source: http://www.fullman.com/semiconductors/_polysilicon.html

Crystal Pulling: CZ method

Quartz Crucible
Single Crystal Silicon Seed
Single Crystal silicon Ingot
Molten Silicon 1415 °C
Heating Coils
Graphite Crucible
CZ Crystal Pullers

Mitsubishi Materials Silicon

Source: http://www.fullman.com/semiconductors/_crystalgrowing.html

CZ Crystal Pulling

Source: http://www.fullman.com/semiconductors/_crystalgrowing.html
Floating Zone Method

Comparison of the Two Methods

• CZ method is more popular
  – Cheaper
  – Larger wafer size (300 mm in production)
  – Reusable materials

• Floating Zone
  – Pure silicon crystal (no crucible)
  – More expensive, smaller wafer size (150 mm)
  – Mainly for power devices.
Ingot Polishing, Flat, or Notch

Flat, 150 mm and smaller  
Notch, 200 mm and larger

Wafer Sawing

Orientation  
Notch  
Saw Blade  
Coolant  
Crystal Ingot  
Ingot Movement  
Diamond Coating
Parameters of Silicon Wafer

<table>
<thead>
<tr>
<th>Wafer Size (mm)</th>
<th>Thickness (µm)</th>
<th>Area (cm²)</th>
<th>Weight (grams)</th>
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<tbody>
<tr>
<td>50.8 (2 in)</td>
<td>279</td>
<td>20.26</td>
<td>1.32</td>
</tr>
<tr>
<td>76.2 (3 in)</td>
<td>381</td>
<td>45.61</td>
<td>4.05</td>
</tr>
<tr>
<td>100</td>
<td>525</td>
<td>78.65</td>
<td>9.67</td>
</tr>
<tr>
<td>125</td>
<td>625</td>
<td>112.72</td>
<td>17.87</td>
</tr>
<tr>
<td>150</td>
<td>675</td>
<td>176.72</td>
<td>27.82</td>
</tr>
<tr>
<td>200</td>
<td>725</td>
<td>314.16</td>
<td>52.98</td>
</tr>
<tr>
<td>300</td>
<td>775</td>
<td>706.21</td>
<td>127.62</td>
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</tbody>
</table>

Wafer Edge Rounding

Wafer Before Edge Rounding

Wafer After Edge Rounding
Wafer Lapping

- Rough polished
- conventional, abrasive, slurry-lapping
- To remove majority of surface damage
- To create a flat surface

Wet Etch

- Remove defects from wafer surface
- 4:1:3 mixture of HNO₃ (79 wt% in H₂O), HF (49 wt% in H₂O), and pure CH₃COOH.
- Chemical reaction:

  \[ 3 \text{Si} + 4 \text{HNO}_3 + 6 \text{HF} \rightarrow 3 \text{H}_2\text{SiF}_6 + 4 \text{NO} + 8 \text{H}_2\text{O} \]
Chemical Mechanical Polishing

200 mm Wafer Thickness and Surface Roughness Changes

- After Wafer Sawing: 76 µm, 914 µm
- After Edge Rounding: 76 µm, 914 µm
- After Lapping: 12.5 µm, 814 µm
- After Etch: <2.5 µm, 750 µm
- After CMP: Virtually Defect Free, 725 µm
Epitaxy Grow

- Definition
- Purposes
- Epitaxy Reactors
- Epitaxy Process

Epitaxy: Definition

- Greek origin
- *epi*: upon
- *taxy*: orderly, arranged

- Epitaxial layer is a single crystal layer on a single crystal substrate.
Epitaxy: Purpose

- Barrier layer for bipolar transistor
  - Reduce collector resistance while keep high breakdown voltage.
  - Only available with epitaxy layer.
- Improve device performance for CMOS and DRAM because much lower oxygen, carbon concentration than the wafer crystal.

Epitaxy Application, Bipolar Transistor
Epitaxy Application: CMOS

Silicon Source Gases

Silane \quad \text{SiH}_4
Dichlorosilane \quad \text{DCS} \quad \text{SiH}_2\text{Cl}_2
Trichlorosilane \quad \text{TCS} \quad \text{SiHCl}_3
Tetrachlorosilane \quad \text{SiCl}_4
Dopant Source Gases

- Diborane \( B_2H_6 \)
- Phosphine \( PH_3 \)
- Arsine \( AsH_3 \)

DCS Epitaxy Grow, Arsenic Doping

\[
\text{Heat (1100 °C)} \\
\text{SiH}_2\text{Cl}_2 \rightarrow \text{Si} + 2\text{HCl} \\
\text{DCS} \quad \text{Epi} \quad \text{Hydrochloride}
\]

\[
\text{Heat (1100 °C)} \\
\text{AsH}_3 \rightarrow \text{As} + 3/2 \text{H}_2
\]
Schematic of DCS Epi Grow and Arsenic Doping Process

Epitaxial Silicon Growth Rate Trends
Barrel Reactor

Vertical Reactor

Reactants and byproducts
Epitaxy Process, Batch System

- Hydrogen purge, temperature ramp up
- HCl clean
- Epitaxial layer grow
- Hydrogen purge, temperature cool down
- Nitrogen purge
- Open Chamber, wafer unloading, reloading
Single Wafer Reactor

• Sealed chamber, hydrogen ambient
• Capable for multiple chambers on a mainframe
• Large wafer size (to 300 mm)
• Better uniformity control
Epitaxy Process, Single Wafer System

- Hydrogen purge, clean, temperature ramp up
- Epitaxial layer grow
- Hydrogen purge, heating power off
- Wafer unloading, reloading
- In-situ HCl clean,

Why Hydrogen Purge

- Most systems use nitrogen as purge gas
- Nitrogen is a very stable abundant
- At > 1000 °C, N₂ can react with silicon
- SiN on wafer surface affects epi deposition
- H₂ is used for epitaxy chamber purge
- Clean wafer surface by hydrides formation
Properties of Hydrogen

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
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<tbody>
<tr>
<td>Name</td>
<td>Hydrogen</td>
</tr>
<tr>
<td>Symbol</td>
<td>H</td>
</tr>
<tr>
<td>Atomic number</td>
<td>1</td>
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<tr>
<td>Atomic weight</td>
<td>1.00794</td>
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<tr>
<td>Discoverer</td>
<td>Henry Cavendish</td>
</tr>
<tr>
<td>Discovered at</td>
<td>England</td>
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<td>Discovery date</td>
<td>1766</td>
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<tr>
<td>Origin of name</td>
<td>From the Greek words &quot;hydro&quot; and &quot;genes&quot; meaning &quot;water&quot; and &quot;generator&quot;</td>
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<tr>
<td>Molar volume</td>
<td>11.42 cm$^3$</td>
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<td>Velocity of sound</td>
<td>1270 m/sec</td>
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<td>Refractive index</td>
<td>1.000132</td>
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<tr>
<td>Melting point</td>
<td>-258.99 °C</td>
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<tr>
<td>Boiling point</td>
<td>-252.72 °C</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>0.1805 W m$^{-1}$ K$^{-1}$</td>
</tr>
</tbody>
</table>

Defects in Epitaxy Layer

- Stacking Fault from Surface Nucleation
- Stacking Fault form Substrate Stacking Fault
- Dislocation
- Impurity Particle
- Hillock
- Epi Layer
- Substrate

After S.M. Zse’s VLSI Technology
Future Trends

- Larger wafer size
- Single wafer epitaxial grow
- Low temperature epitaxy
- Ultra high vacuum (UHV, to \(10^{-9}\) Torr)
- Selective epitaxy

Summary

- Silicon is abundant, cheap and has strong, stable and easy grown oxide.
- \(<100>\) and \(<111>\)
- CZ and floating zone, CZ is more popular
- Sawing, edging, lapping, etching and CMP
Summary

- Epitaxy: single crystal on single crystal
- Needed for bipolar and high performance CMOS, DRAM.
- Silane, DCS, TCS as silicon precursors
- $\text{B}_2\text{H}_6$ as P-type dopant
- $\text{PH}_3$ and $\text{AsH}_3$ as N-type dopants
- Batch and single wafer systems